Reference Manual
P853,854



Data
Systems

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1 SYSTEM ASPECTS

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1.1 INTRODUCTION

The P853 minicomputer system utilizes the CP1A Central Processor Unit (CPU), which is the successor of the P851M-CPU.

The P854 minicomputer system utilizes the P857E/B Central Processor Unit (CPU), which combines the advantages of the P857M-CPU with the smaller physical size of the Eurocard.

The P857E employs Microprocessor technology to perform 3 CPU functions:

- Arithmetic Logic Unit, in the format of 4 x 4-bit slices to form the 16-bit word.
- Memory Address Sequensor, in the format of 4 x 4-bit slices to form the 16-bit memory address.
- Micro-Program Sequensor which has control over most CPU functions and their execution.

The P857E uses the P857 instruction set plus an extra three groups:

- Bit String Handling.
- Address Loading.
- Character String Handling.

The system input/output and control is with the Unified Product Line (UPL) Bus which interconnects all system units. The P857E may be connected with other devices in the P800 family via the UPL Bus; these devices are:

- GPBS (P851) Control Units.
- UPL Control Units and Memories.
- GPB (P856 and P857) Control Units using the Translator Card (TUGP).

The principle facilities available with the P854 are as follows:

- 16 hardware registers.
- V24 interface for operators peripheral.
- V24 interface for Control Panel.
- Power Failure/ Automatic Restart.
- Battery Back-Up after Power Failure.
- Real Time Clock.
- 2 IOP Channels (16 sub-channels).
- 32 parallel interrupts of which 4 are internal to the CPU.
- Up to 61 serial encoded interrupts.
- Hardware Bootstrap Loading with facility to load from one of 16 external devices.
- One of two serial Control Panels: HHCP - displays a hexadecimal address or data, FRCP - displays hexadecimal address and data simultaneously.
- Logical addressing for up to 32k words, 16 bits (CPU function).
- Physical addressing for up to 8M words, 24 bits (MMU Function).
- Memory Protection on a Page basis (MMU Function).
- Stop On Preset Address for up to 512k words, 20 bits (SOPA Function)

The principle components showing their connection to the P854 are shown in Figure 1.1.

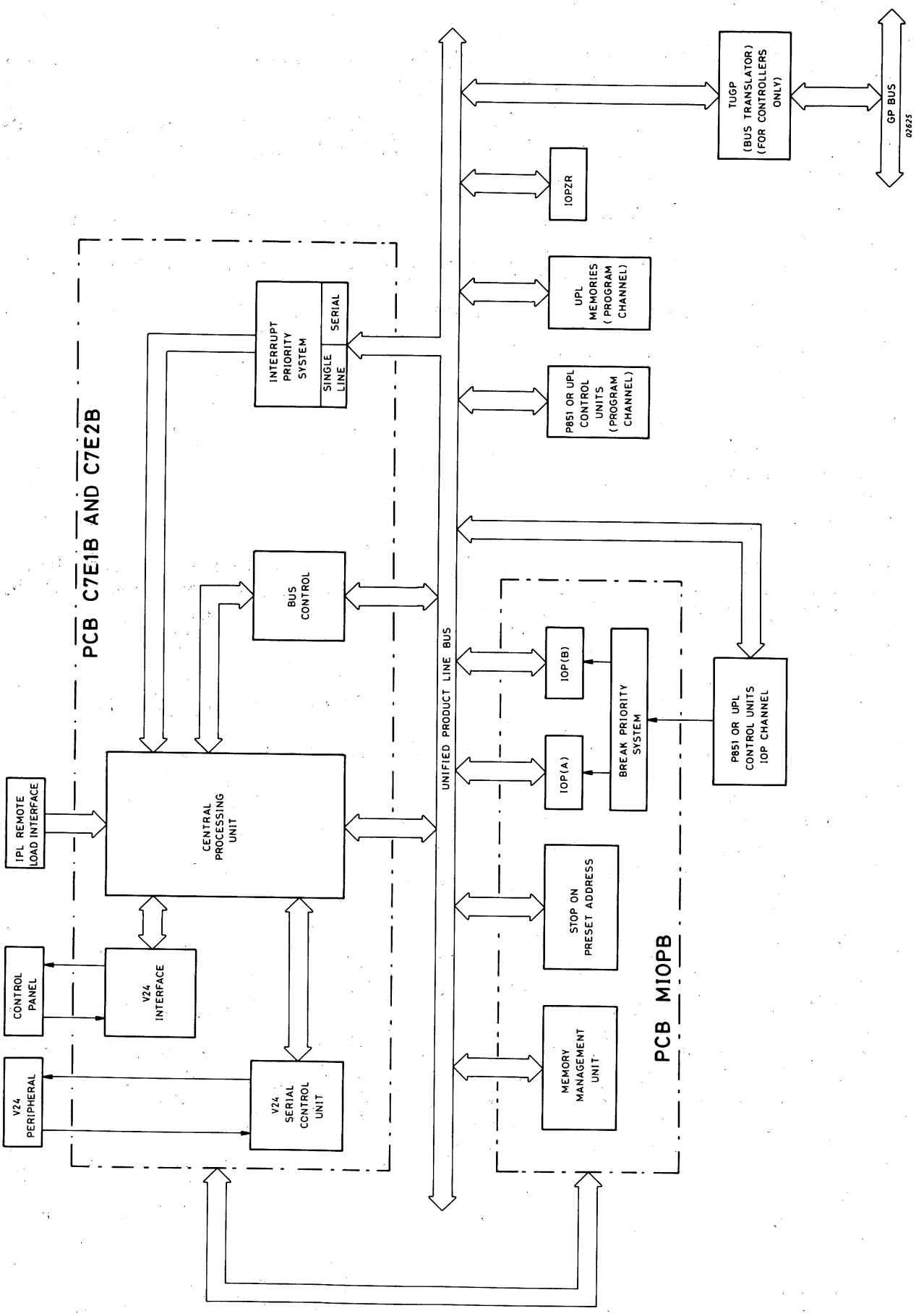


Figure 1.1 P854 MAIN SYSTEM COMPONENTS

1.2 UNIFIED PRODUCT LINE BUS

In the following description N, behind a signal name, stands for "Active Low". The signals and lines, associated with the Bus functions are.

Bus Allocation Signals

BUSRN A signal bus request which is sent to the bus controller in the CPU by a master which requires control of the bus to effect an exchange.

BYSN A signal Bus Busy which is shared by all masters. It is set to "0" by the master which has been given control of the bus so that the exchange can commence without interruption.

MSN A signal Master Selected which is transmitted to all other masters by the master which has become master of the bus to block all activity of the priority selection chain. The signal is released when the master is ready for the next priority transaction.

ERQN Enable Request is sent by the Bus controller and received by masters working with the second level of priority. ERQN is set to 0 when there is no request, no current allocation, no master selected, no current exchange on the bus.

OKO A signal generated by the bus controller. It is sent to the master having the highest priority (determined by hard wiring in the priority selection chain).

OKI A master which receives signal OKO regards the signal as OKI. It then retransmits a further OKO to the next master in the priority chain. The first master to receive OKI (set to "1" and to retransmit OKO reset to "Ø") is next master of the bus.

Bus Address Lines

MADØØ - MAD15, MADEØØ-MADEØ7

These lines carry the memory address, register address, peripheral address or the requested control unit function. They are qualified by a timing signal from a master.

1. Memory Exchange (qualified by TMRN)
   MADØØ through MAD14: these lines carry the 15-bit memory address required to access up to 32k 16-bit words of memory.
   MAD15: this line is only significant in character operations. It carries the least significant bit of the memory address and indicates whether the right hand character (MAD15 = 1) or the left hand character (MAD15 = Ø) of a word is addressed.
   MADE00-through MADEØ7: these lines extend the memory addressing to 8M 16 bit words.
2. External Register (qualified by TMEN)
   MADØ8 through MAD15: these lines give the 8-bit address of an external register.
   MADØ4: this line is used to indicate a Read (MADØ4 = 1) or Write (MADØ4 = Ø) operation.
3. Peripheral Control Unit Exchange (qualified by TMPN)
   MAD1Ø through MAD15: these lines carry the 6-bit device address required to access up to 64 control units.
   MADØ4 = direction of the exchange of Ø to control unit
   1 to master.
   MADØ8 = indicates whether a data exchange, command or status exchange.
   MADØ9 = this line is a function line reserved for special control units.
   MADØ3 = this line is used to indicate whether the current word or character exchange is the last exchange. If 1: last exchange.

Bus Data Lines

BIOØØN - BIO15N

16 input/output lines used to transfer data between units.

Data and Command Exchange Signals

Timing Signals

TMRN This signal is raised by a master and is used to validate the data and address and to control the timing of the exchange with memory.

TMPN This signal is raised by a master and is used to validate the control data and address and to control the timing of an exchange with peripheral control unit.

TMEN This signal is raised by a master and is used to validate the data and address and to control the timing of an exchange between a master and a unit containing an external register.

TSMN This signal is raised by a slave as answer to TMRN, TMPN or TMEN and validates the data during an input operation or to signal the termination of an exchange.

Miscellaneous Signals

CLEARN This signal is sent from the CPU to all units connected to the Bus and initiates a general reset of these units.

WRITE This signal is raised by a master to indicate that the exchange is "Write to Memory". If not present a "Read from memory" is indicated.

CHA This signal is sent from a master to memory to specify that the requested exchange is to be carried out in character mode. If Ø the change is in word mode.

ACN This signal is sent by a control unit to indicate that it accepts a request from the CPU to carry out a designated function.

BAWOFN This signal is raised to inform that battery power is (was) switched off.

PWFN This signal is raised during the power on or power off or power failure sequence and is used within the system to ensure an orderly run down of operations without loss of data.

RSLN This signal is raised during the power on or power restoration sequence and is used within the system to ensure an orderly commencement or resumption of operation without loss of data.

IRN Ø,1 This signal is raised by the control unit to inform the CPU that a data transfer or status transfer is required.

BRN Ø,1 This signal is raised by the control unit and is sent to the I/O Processor to request a data transfer.

BCI BUS Coded Interrupt (serial)
This interrupt is sent by a control unit with Interrupt Handler Chip Code: 1 start bit, 6 source bits (interrupt level), 6 destination bits and 2 spare bits.

INCL Interrupt Clock. Sent by CPU to all CU's for synchronisation of BCI.

Time-out

For a normal data transfer TMRN, TMEN and TMPN are sent from the CPU to initiate the transfer.
TSMN is the reply of the slave.
If no TSMN signal is received within 6.4 microsec. the CPU generates an external signal TSMN which frees the bus.

Relation with Power-on/Power-off

After POWER-ON a master is not authorized to request the bus until PWFN is high. When PWFN is going low, the masters must limit their exchanges in order to give to the CPU enough time to execute the power failure routine.

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
1C01	+12V	1B01	ERQN	1A01	-12V
1C02	+5VM	1B02	BUSRN	1A02	+5VM
1C03	BCI	1B03	MSN	1A03	INCL
1C04	*	1B04	ØV	1A04	*
1C05	*	1B05	BSYN	1A05	*
1C06	ØV	1B06	OKO	1A06	ØV
1C07	PWFN	1B07 **	OKI	1A07	RSLN
1C08	CLEARN	1B08	RTCN	1A08	ACN
1C09	ØV	1B09 *	BAWOFN	1A09	ØV
1C10	TMPN	1B10 ***	STOPN	1A10	TSMN
1C11	TMEN	1B11	ØV	1A11	TMRN
1C12	ØV	1B12	MADEØ	1A12	ØV
1C13	MADØØ	1B13	MADE1	1A13	MADØ1
1C14	MADØ2	1B14	ØV	1A14	MADØ3
1C15	MADØ4	1B15	MADE2	1A15	MADØ5
1C16	MADØ6	1B16	MADE3	1A16	MADØ7
1C17	MADØ8	1B17	MADE4	1A17	MADØ9
1C18	MAD1Ø	1B18	MADE5	1A18	MAD11
1C19	MAD12	1B19	MADE6	1A19	MAD13
1C20	MAD14	1B20	MADE7	1A20	MAD15
1C21	CHA	1B21	ØV	1A21	WRITE
1C22	ØV	1B22	*	1A22	Ø
1C23	BIOØ8N	1B23	*	1A23	BIOØØN
1C24	BIOØ9N	1B24	*	1A24	BIOØ1N
1C25	BIO1ØN	1B25	*	1A25	BIOØ2N
1C26	BIO11N	1B26	ØV	1A26	BIOØ3N
1C27	BIO12N	1B27	*	1A27	BIOØ4N
1C28	BIO13N	1B28	*	1A28	BIOØ5N
1C29	BIO14N	1B29	*	1A29	BIOØ6N
1C30	BIO15N	1B30	*	1A30	BIOØ7N
1C31	+12VM	1B31	+5VL	1A31	+12VM
1C32	+5VL	1B32	+5VL	1A32	+5VL

* These signals are not bussed on the backpanel.
** This point is not used at the CPU level.
OKO is connected with OKI from the next connector of the backpanel.
*** Not used in P800, however signals may still be connected.

Table 1.1 UPL BUS

1.3 TYPICAL BUS ASPECTS GP - UPL.

Bus timing: difference of memory access (write)

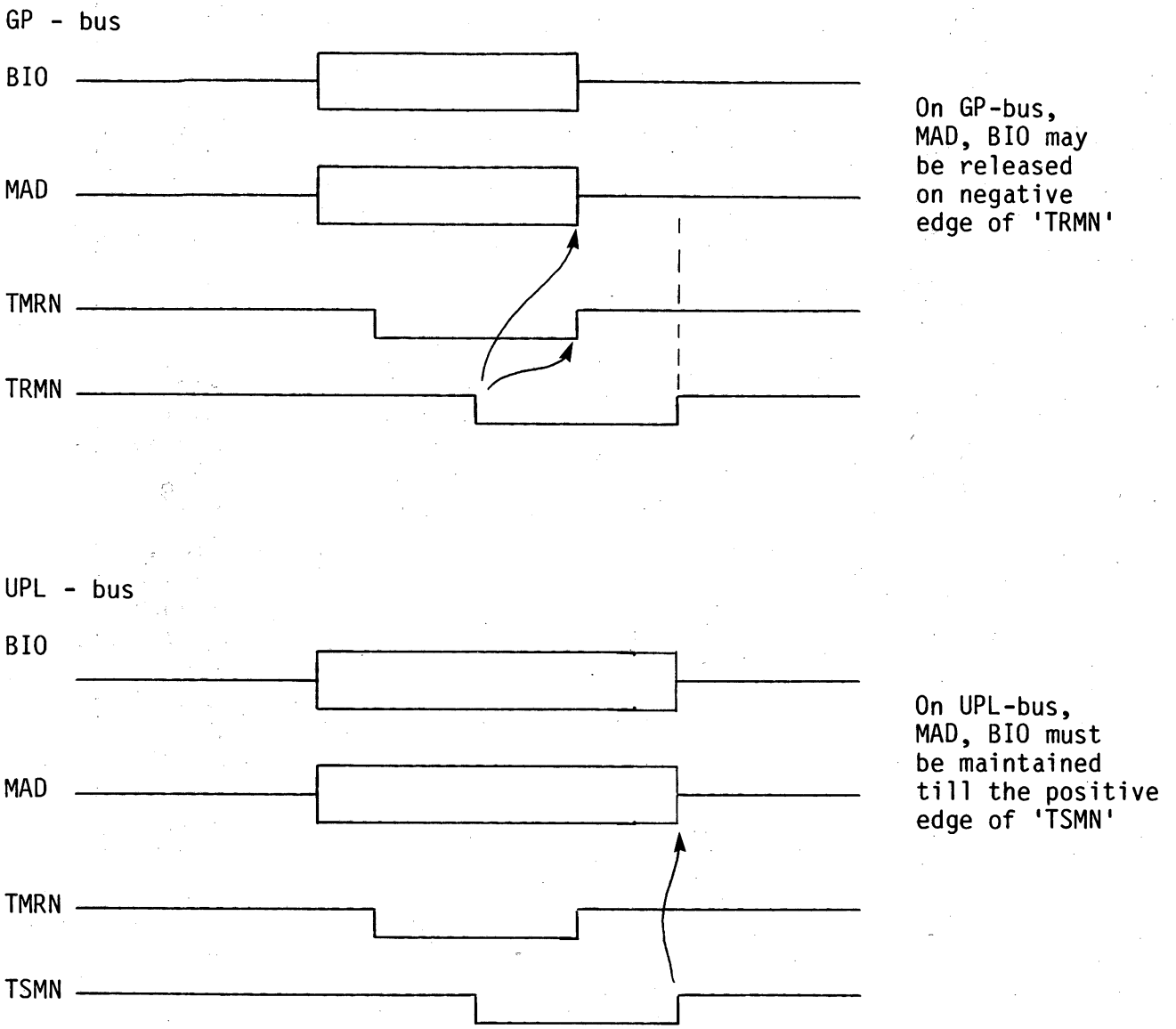


Figure 1.2 GP - UPL BUS TIMING

1.4 UPL BUS ALLOCATION

- Bus priority logic will select the master which requests the bus. In case of more requests, only the master with highest priority will access the bus.
- Master may be switched to second class of priority. In that case bus access can only be done if no requests are available, nor the bus is busy. This is indicated by ERQN.
- The CPU may only use the bus if no other masters do a bus request.

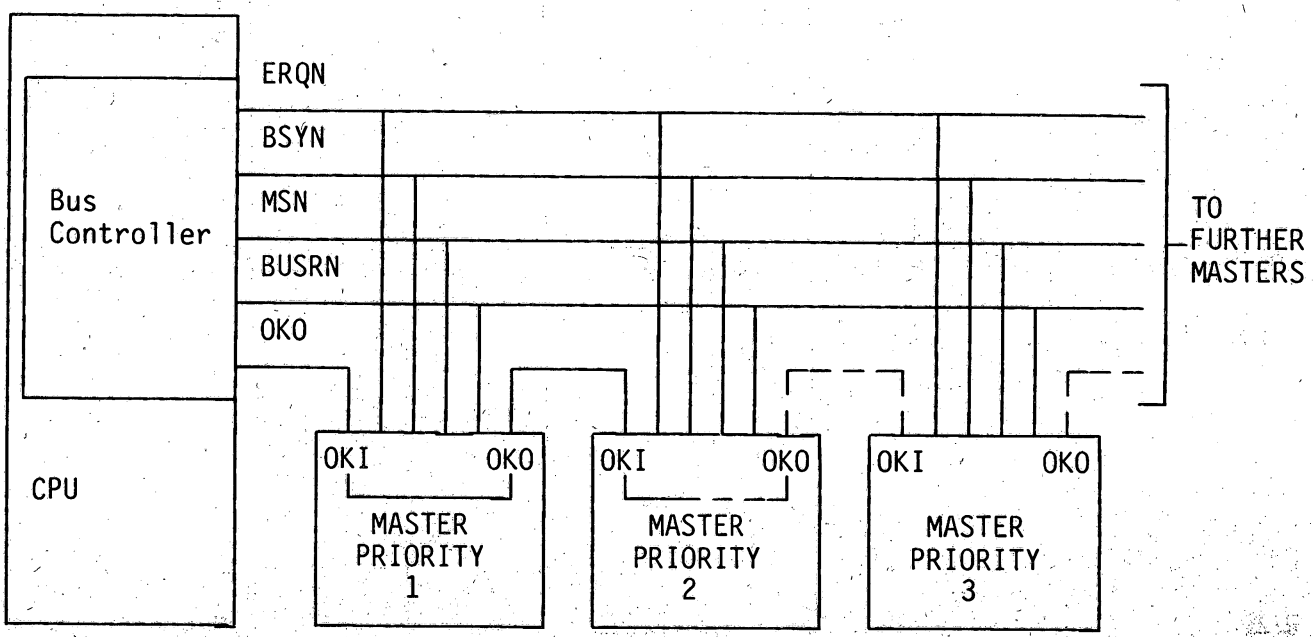


Figure 1.3 UPL BUS PRIORITY CONTROL

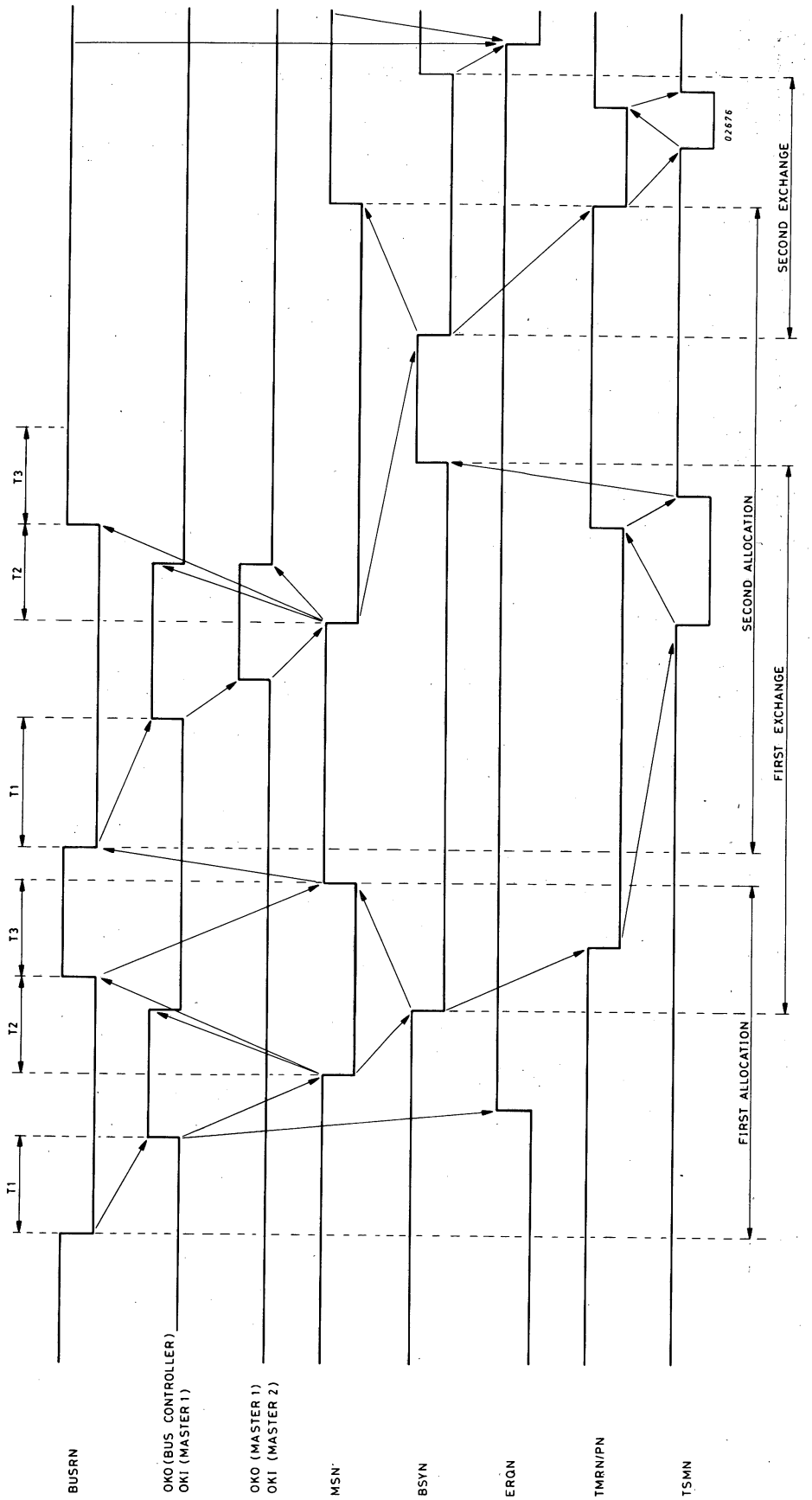
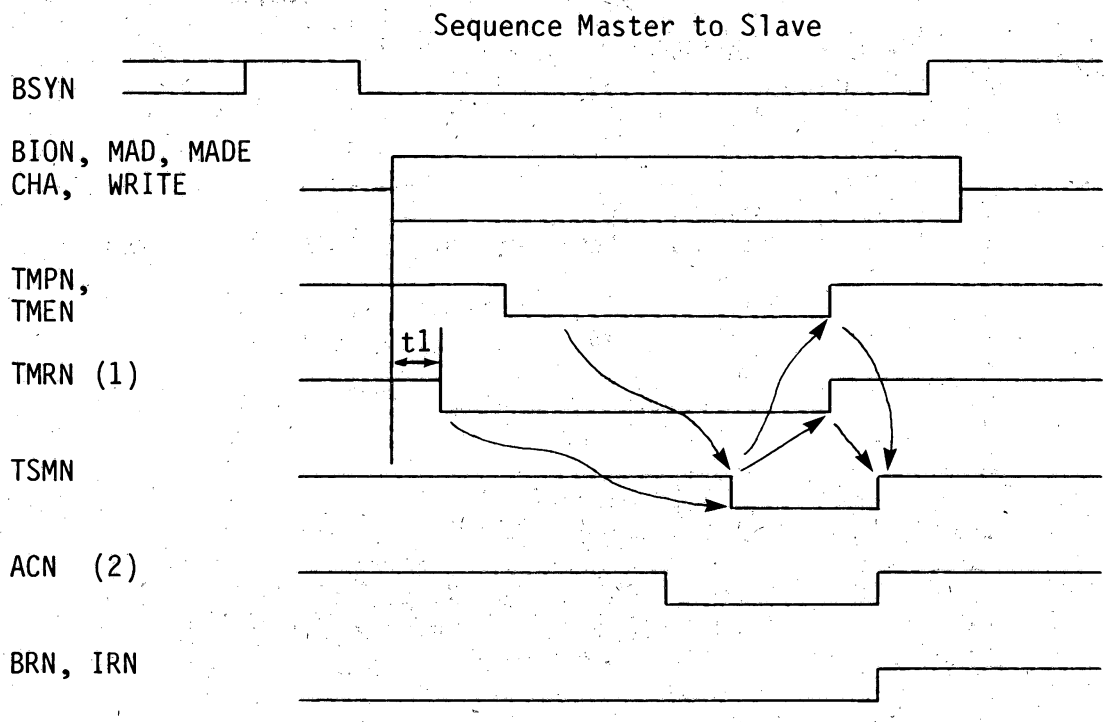


Figure 1.4 EXAMPLE OF 2 BUS ALLOCATIONS



Remarks:
1. New Masters will be able to generate TMRN with t1 = 50ns to be able to work with P851 memories, new memories consider t1 = 25ns.
2. New Masters which work with P851 control units must take into account that ACN signal can be defined 95ns after TSMN = Ø.

Figure 1.5a MASTER TO SLAVE TIMING

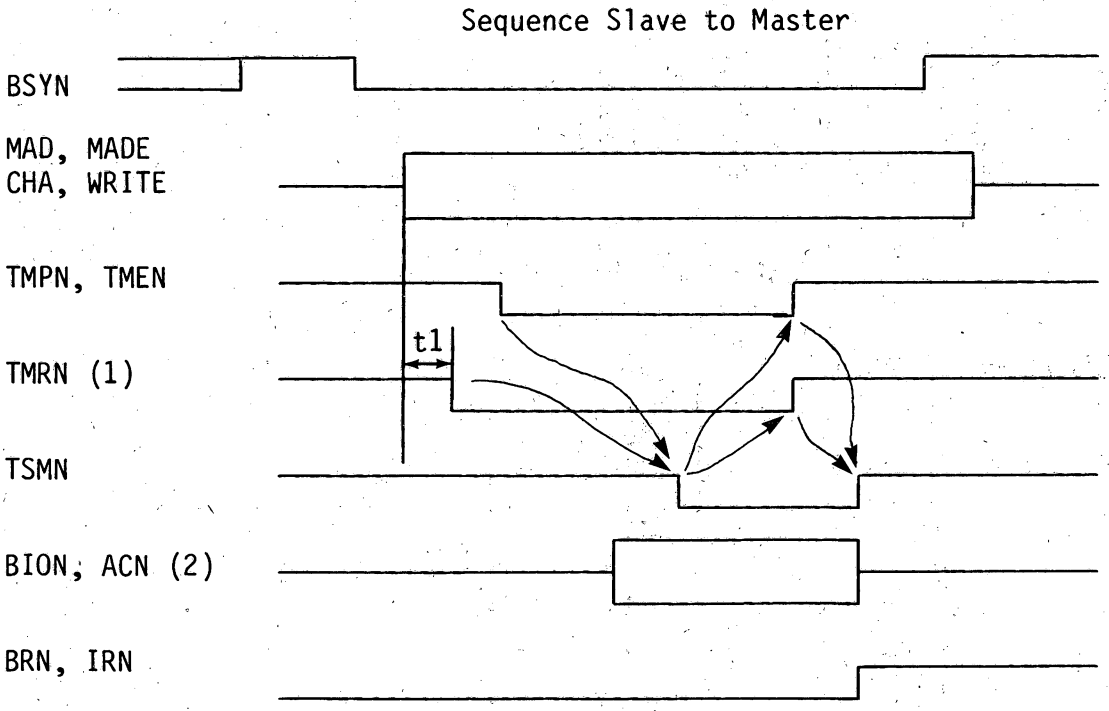


Figure 1.5b SLAVE TO MASTER TIMING

1.6 RECOMMENDED STANDARD INTERRUPTS

	LEVEL HEX	LEVEL DEC	INTERR. CONTROL ADDRESS HEX		SOURCE
INTERNAL (FIXED)	0	0	0		PF/AR
	1	1	2		LKM or Stackoverflow i.e. (A15) less than /100
	2	2	4		RTC
	3	3	6	*	FPP (P854: Control Panel)
EXTERN	4	4	8		Spare (Temporary: memory error)
	5	5	A		Spare
	6	6	C		Operator Console
	7	7	E	*	Control Panel
	8	8	10		DTC
	9	9	12	*	DTC (P854: PTR)
	A	10	14	*	DTC (P854: PTP)
	B	11	16		DTC On programmed channel
	C	12	18	*	DTC (P854: Disc X1215/16)
	D	13	1A	*	DTC (P854: Line Printer X1415/25)
	E	14	1C	*	DTC (P854: Disc floppy)
	F	15	1E	*	PTR
	10	16	20		Disc CDC (ad/16)
	11	17	22	*	Disc X1215 (ad/02)
	12	18	24	*	Disc floppy (ad/03)
	13	19	26	*	MT
	14	20	28		TK
	15	21	2A		CR
	16	22	2C	*	PTP
	17	23	2E	*	LP
	18	24	30		Disc X1216 (ad/01)
	19	25	32		Disc CDC (ad/17)
	1A	26	34		DTC
	1B	27	36		DTC
	1C	28	38		DTC On IOP
	1D	29	3A		DTC
	1E	30	3C	*	DTC (P854: MT)
	1F	31	3E		DTC

Table 1.2 INTERRUPTS

* Note: Not standard on P854.

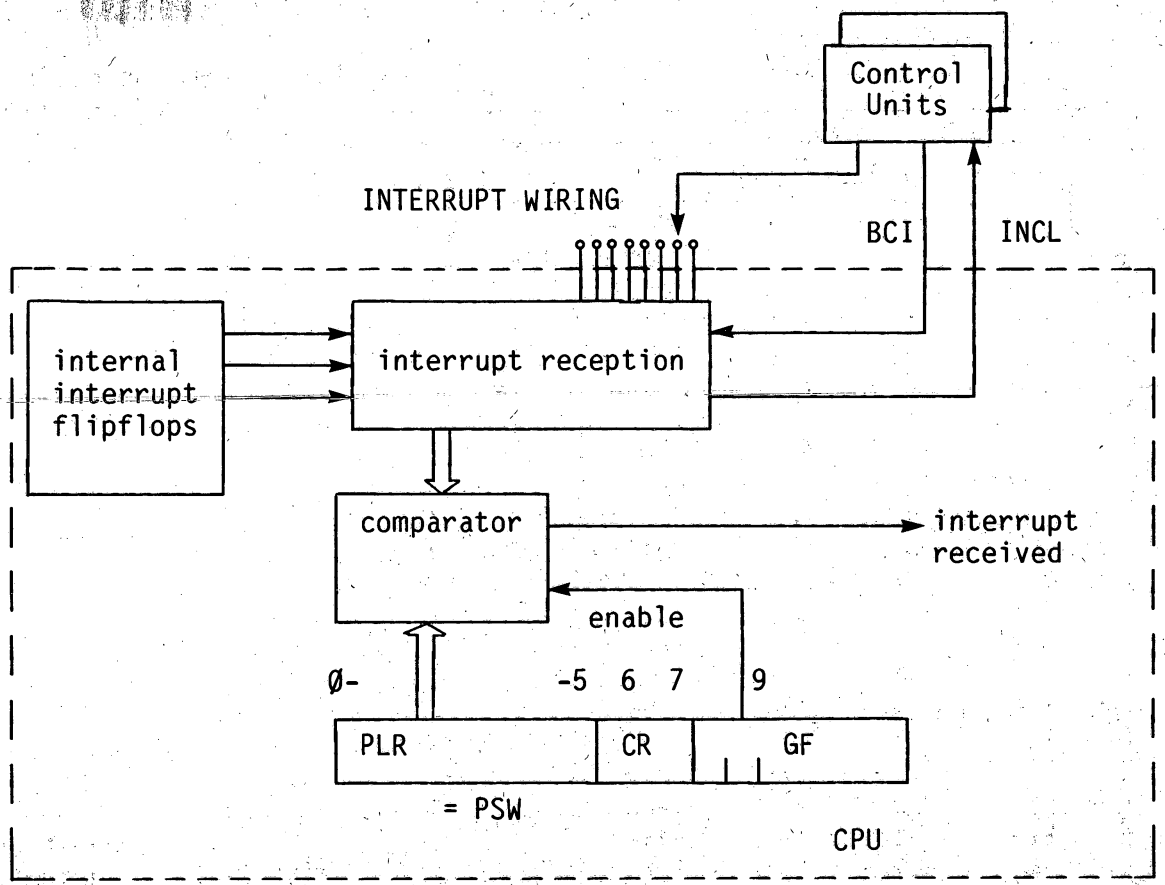
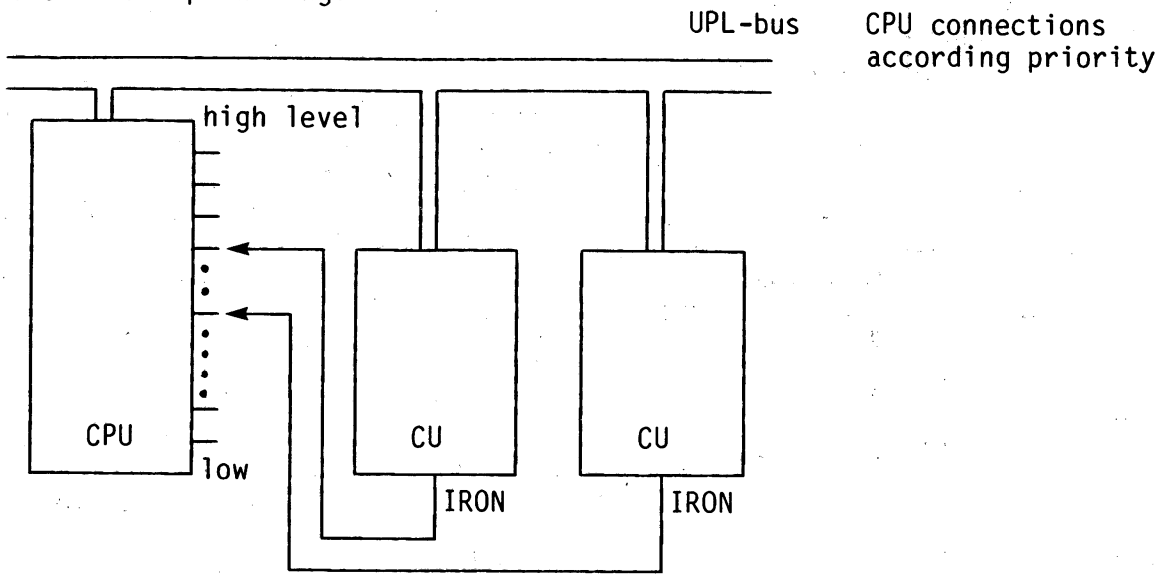


Figure 1.6 INTERRUPT SYSTEM P853/4

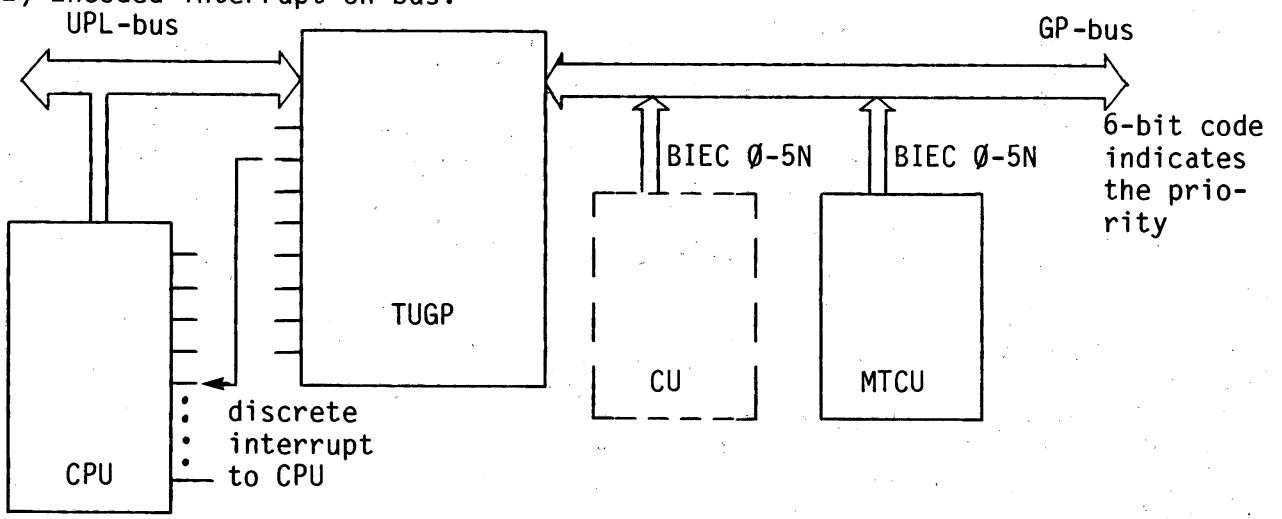
Interrupt Acceptance:
- Store P (return address) ┐
- Store PSW (save condition register) ├ STACK
- Update A15 (for possible next interrupt) ┘
- Inhibit for further interrupts
- PLR updated
- P loaded with the start address of the interrupt routine
- User to system mode

Interrupt Transport Modes

1) Discrete interrupt wiring:



2) Encoded interrupt on bus:



3) Binary coded interrupts on serial line:

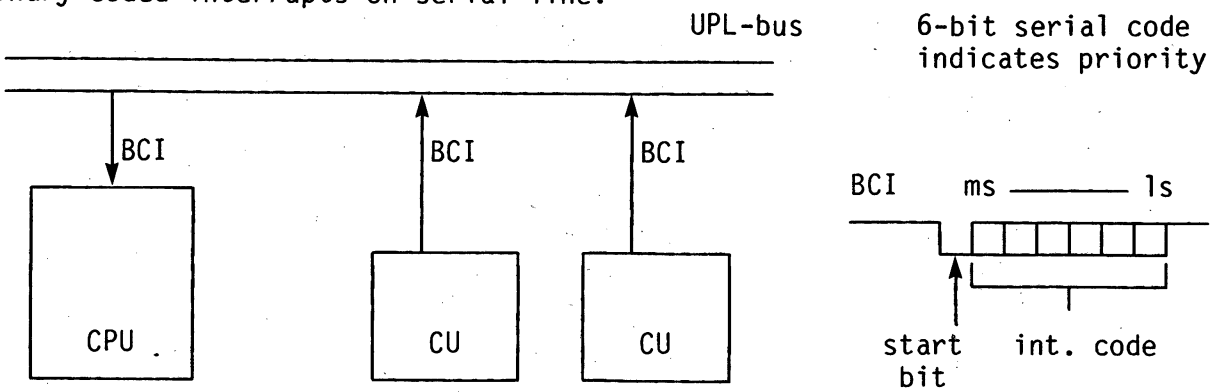


Figure 1.7 INTERRUPT TRANSPORT MODES

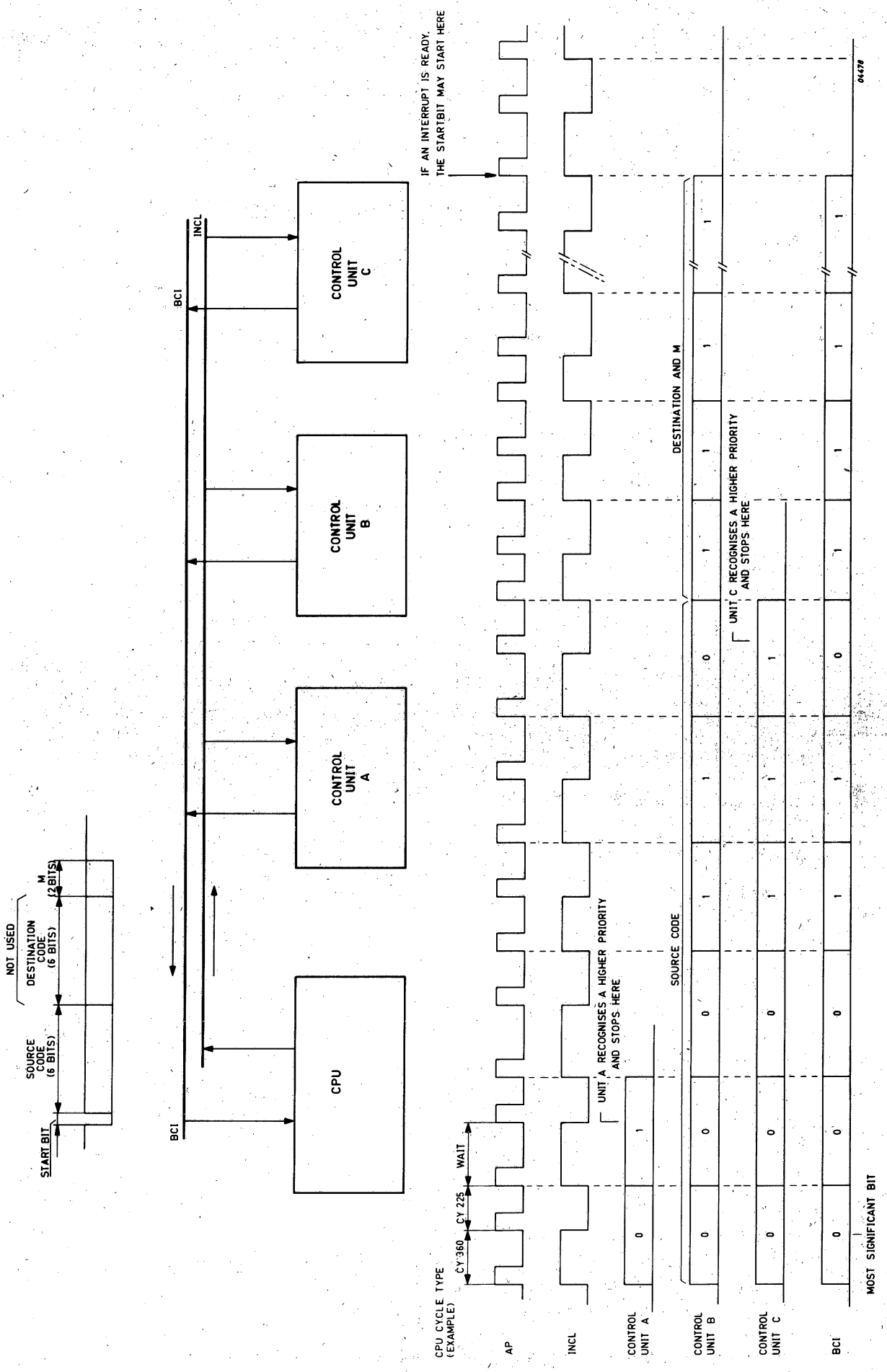


Figure 1.8 SERIAL INTERRUPTS - PRINCIPLE OF OPERATION

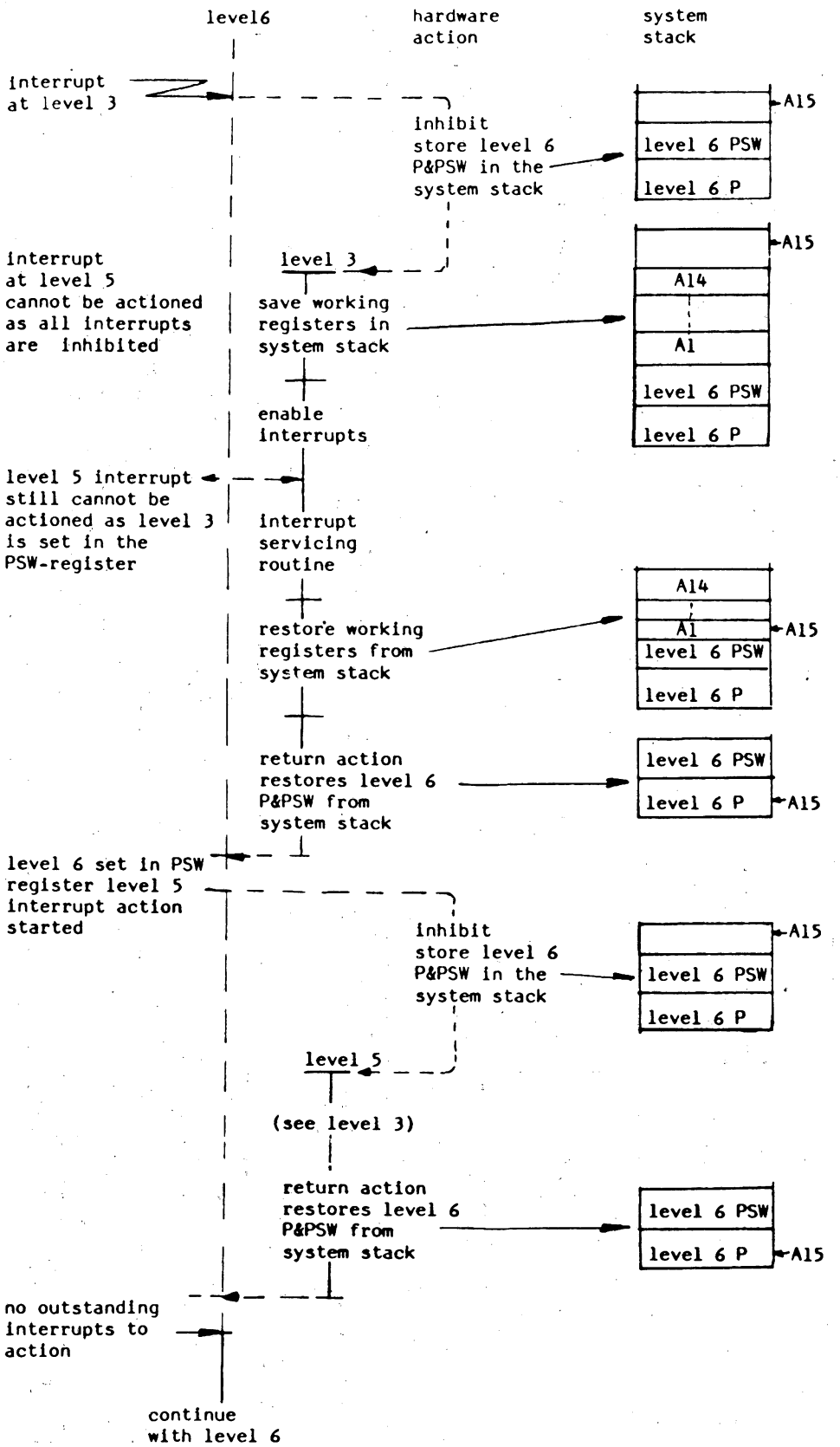


Figure 1.9 DIAGRAM OF INTERRUPT SEQUENCE

Control Unit modes
Example:

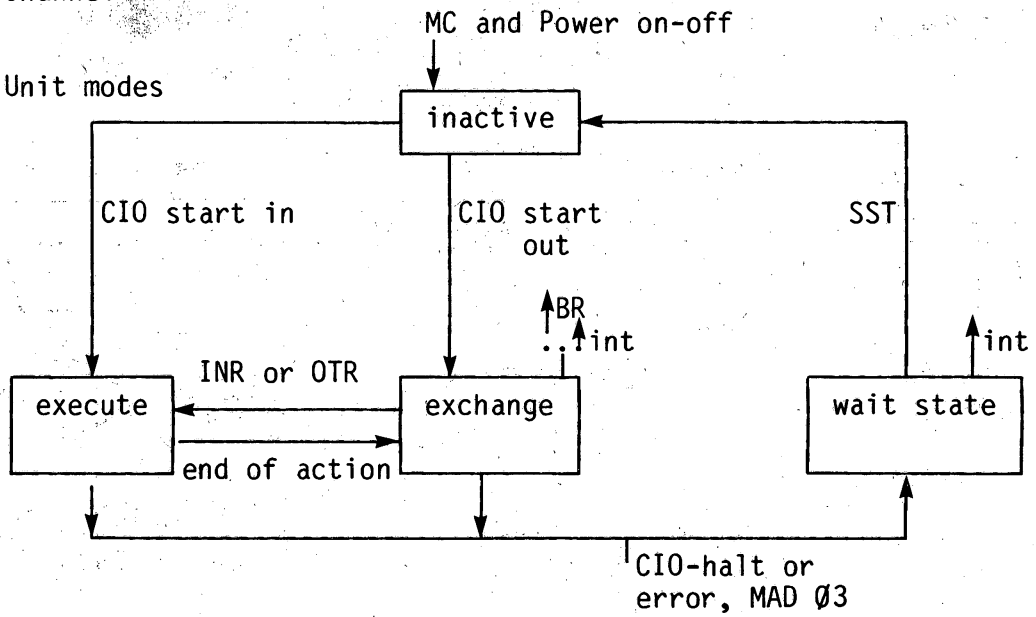
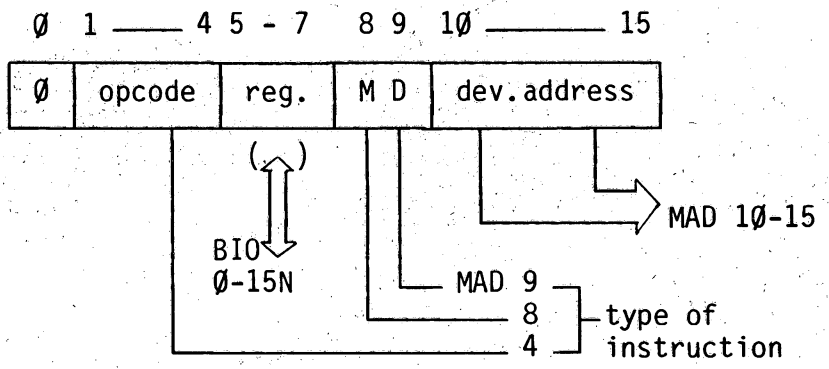


Figure 1.10 CONTROL UNIT MODES

I/O Instruction Format



Instruction		4	8	9	
MAD Lines	Ø3	Ø4	Ø8	Ø9	Accepted in mode
CIO start	Ø	Ø	1	1	Inactive
CIO stop	Ø	Ø	1	Ø	Always
INR (Input Transfer)	Ø	1	Ø	Ø	Exchange
OTR (Output Transfer)	Ø	Ø	Ø	Ø	Exchange
TST (Test Status)	Ø	1	1	Ø	Always
SST (Send Status)	Ø	1	1	1	Wait state
INR (last) IOP	1	1	Ø	Ø	Exchange
OTR (last) IOP	1	Ø	Ø	Ø	Exchange

CR reflects acceptance by TSMN and ACN:
Ø Ø = accepted
Ø 1 = not accepted
1 1 = Dev. addr. not recognised

Figure 1.11 IO INSTRUCTIONS

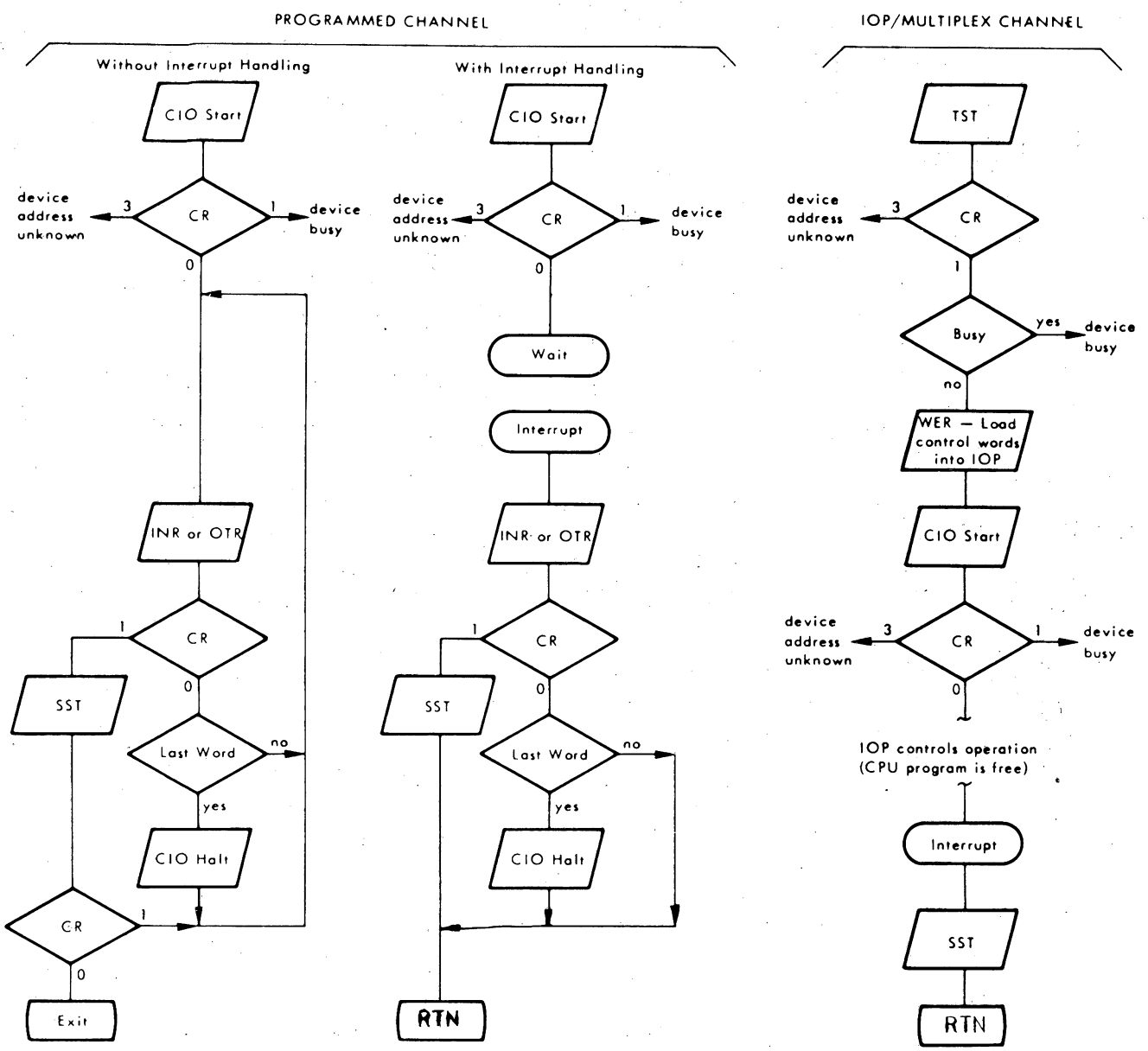


Figure 1.12 CHANNEL PROGRAMMING SEQUENCE

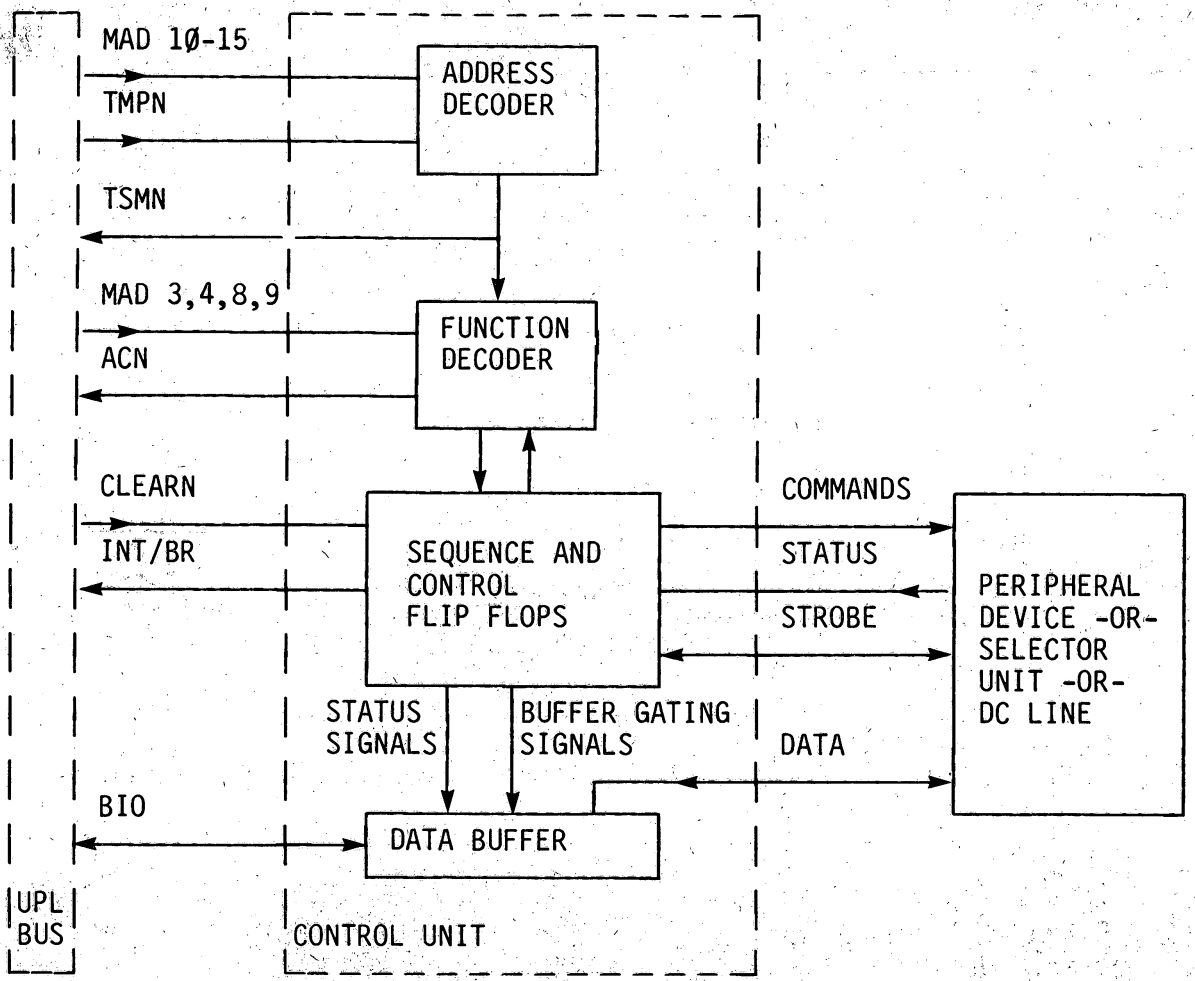
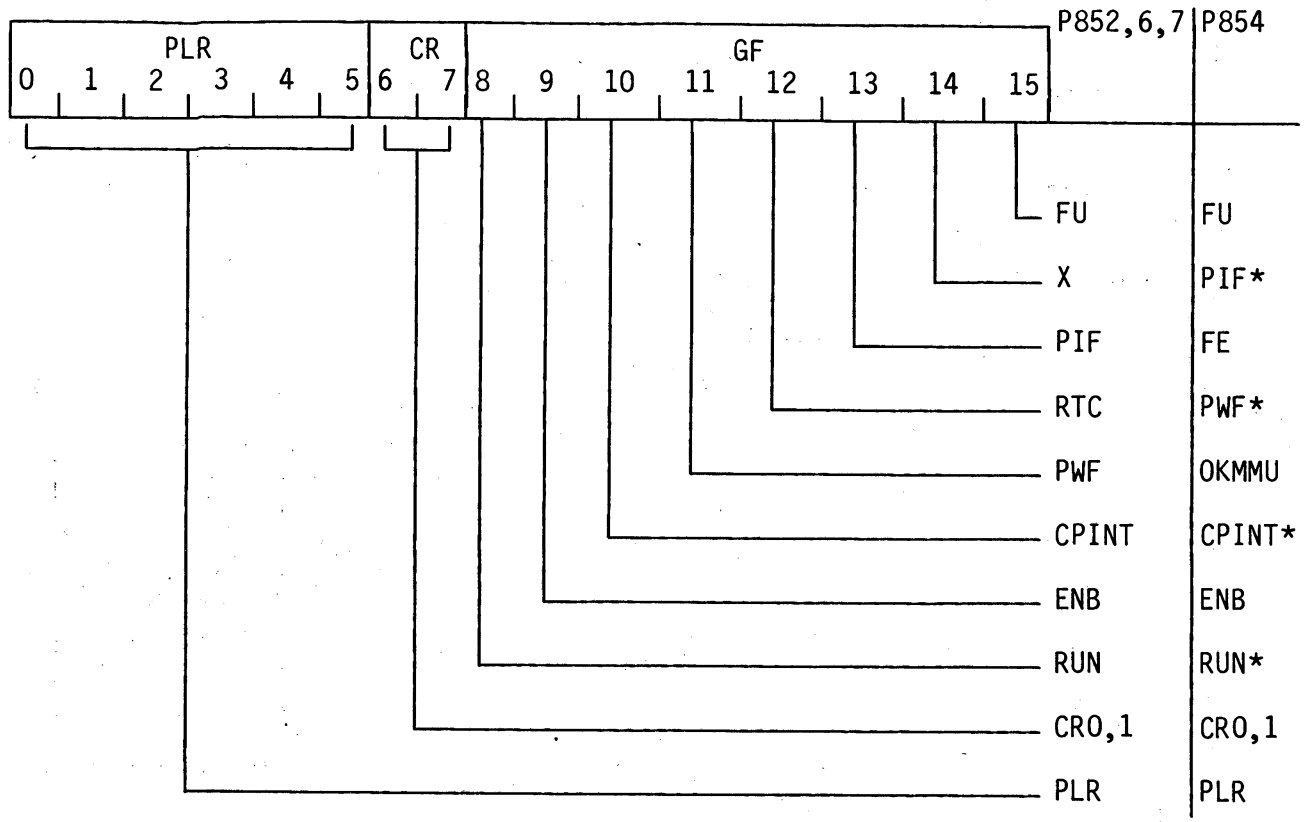


Figure 1.13 BLOCKDIAGRAM OF TYPICAL CONTROL UNIT

1.9 PROGRAM STATUS WORD



FE : Extended System Mode
FU : User Mode
RTC : Real Time Clock
PWF : Power Failure Interrupt
CPint : Control Panel Interrupt

ENB : Interrupt ENable
RUN : CPU in RUN Mode
CR : Condition Register
PLR : Program Level Register
PIF : Program Interrupt, Stack Overflow**

* These bits are not displayable (blanked in microprogram).

CRO,1:

CRO CR1	ARITHMETIC	COMPARE	I/O
00	Zero	Equal	Accepted
01	Positive	Greater	Not Accepted
10	Negative	Less	--
11	Overflow	--	Device Address Unknown

** Stackoverflow if (A15) smaller than /100.

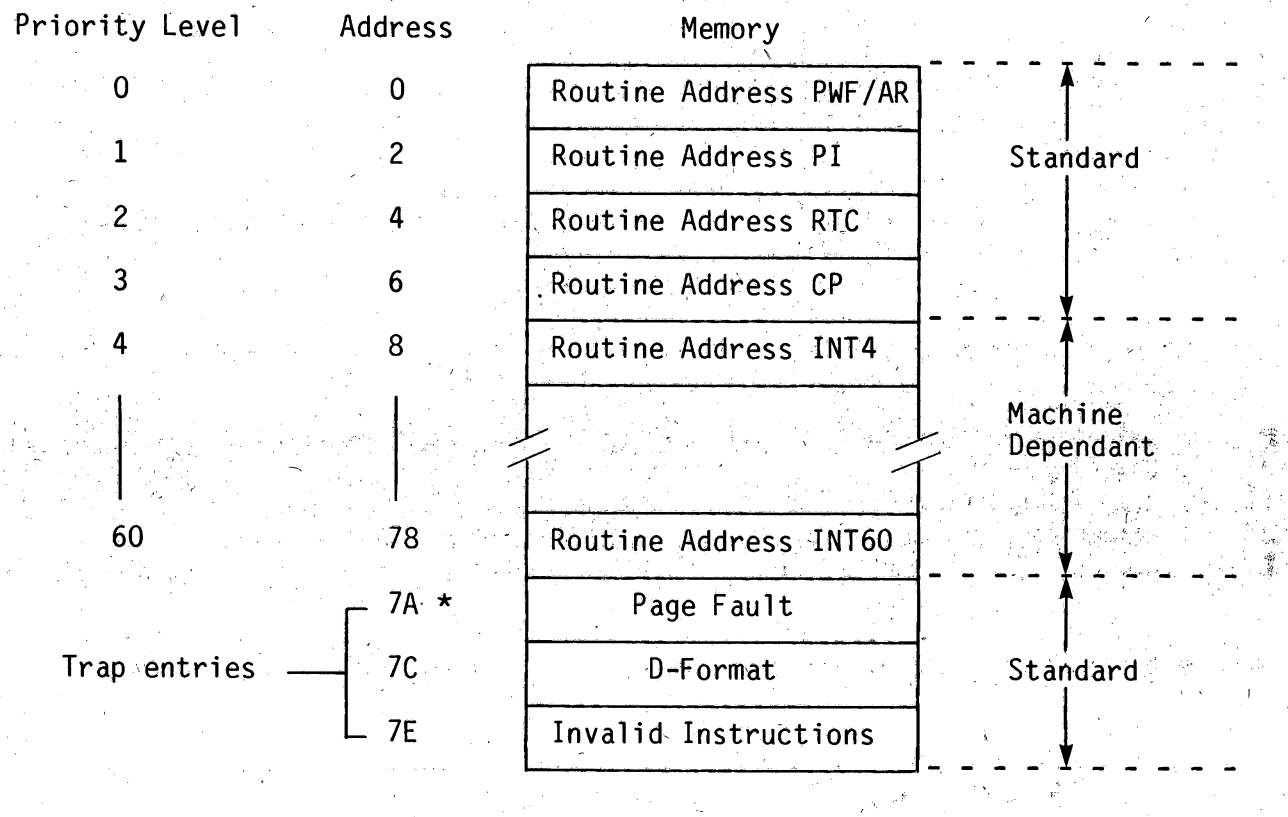
Figure 1.14 PROGRAM STATUS WORD OLD/NEW

1.10 TRAPS

In case the CPU detects either an unknown instruction code or a priviledged instruction in USER mode, the CPU will jump to the TRAP routine.
Actions executed by the CPU are slightly different from an interrupt:

- store P (here: address of the 'wrong' instruction) ┐
- store PSW (save condition register) ┘ STACK
- update A15 (for possible interrupt)
- INHibit for interrupts
- USER to SYSTEM mode
- P loaded with the start address of the TRAP routine.

Memory Layout of Interrupt and Trap Table:



* Not used in P853

Table 1.3 INTERRUPT/TRAP ENTRIES

Missing contents

(See 87x p. 1-24)

1.11 INITIAL PROGRAM LOADER (FIGURE 1.15)

The Initial Program Loader (IPL) is responsible for system initiation by enabling the eventual loading of an Object Program. For purposes of this description the IPL Sequence to load from a Sequential Device is described in 3 parts:

. Bootstrap
. Low Core IPL
. High Core IPL

BOOTSTRAP

The Bootstrap is contained in the Bootstrap ROM in the CPU in a format 1k x 4bits. The CPU assembles this format into 256 x 16-bit words which are loaded into Memory starting from 000. The CPU loads the IPL parameters (keyed in on Control Panel) into Register A15. The Bootstrap enables the loading of the Low Core IPL, from the peripheral addressed in A15.

LOW CORE IPL

The Low Core IPL has 3 principal functions:

. Calculates the size of Memory and subtracts 400 characters to find the High Core start address.
. Loads High Core IPL.
. Starts High Core IPL.

HIGH CORE IPL

The High Core IPL has 3 principal functions:

. The IDENT name of the program to be printed out on the ASR.
. Loads the Object Program starting from address 000.

Rx, vca, VK

1.12 REMOTE IPL

The last 16 words of the Bootstrap (addresses 240-255(1EO to 1FF) inclusive) contain parameters for up to 16 remote devices. The system enables operation in one of two modes:

. Address is selected by card links OPSON-3N (see Note).
. Remote Device sends its own address, no links selected.

The parameter from the selected address will be loaded into A15.

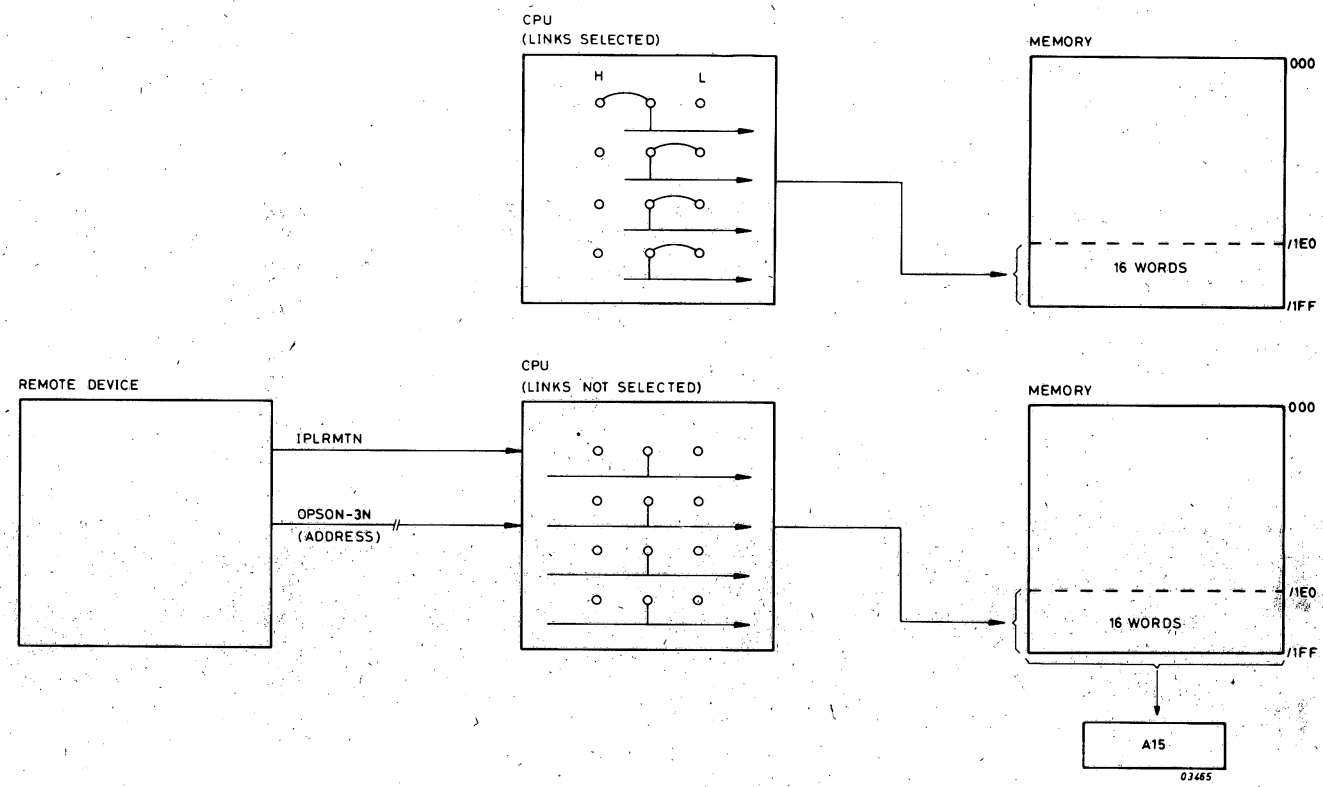


Figure 1.16 REMOTE IPL

Note:

The same hardware is used for AUTOMATIC IPL.
AUTOMATIC IPL is done after POWER-ON in LOCK-mode, only if the memory contents was not maintained by BATTERY supply (AUTOMATIC RESTART of the program is done when memory contents was maintained).

1.13 STANDARD DEVICE ADDRESSES

Device connected to:
Single Device Controllers

Console Typewriter	/10 (FIXED)*
PTR	/20
PTP	/30
CR	/06
LP	/07

Device connected to:
Multiple Device Controllers

X1215 Disc	Drive 0 cartridge	/02
	fixed	/22
	Drive 1 cartridge	/12
	fixed	/32
X1216 Disc	Drive 0 cartridge	/01
	fixed	/21
	Drive 1 cartridge	/11
	fixed	/31
Flexible Disc	Drive 0	/03
	Drive 1	/13
	Drive 2	/23
	Drive 3	/33
Magnetic Tape	Drive 0	/04
	Drive 1	/14
	Drive 2	/24
	Drive 3	/34
Cassette Tape	Drive 0	/05
	Drive 1	/15
	Drive 2	/25

Bigdisc	First Contr.	Second Contr.
	Drive 0 /16	Drive 0/17
	Drive 1 /36	Drive 1/37

* Note: DEVICE ADDRESS /10 only and always to be used for integrated Control Unit on CPU board (P854).

Table 1.4 STANDARD DEVICE ADDRESSES

```
00000                          IDENT    BOOBIG                82-05-12
00001                  *
00002                  *     BOOBIG SUPPORT NEW BIG DISC CONTROLLERS  BIGD2 AND FOLLOWING
00003                  *     CDC BIG DISC CONTROL UNIT
00004                  *
00005                  *
00006                  *        PROM     04063
00007                  *
00008                  * BOOTSTRAP  256*16 BITS
00009                  *            CONTENTS THE DISC AND SEQUENTIAL BOOTSTRAP
00010                  *                     ROM  AND SEQUENTIAL BOOTSTRAP
00011                  *
00012                  *            ALLOWS MOREOVER IPL FROM   MINI FIXED DISK X1250
00013                  *                                       FLOPPY DISK 1MB
00014                  *                                       IPLRZ CARD
00015                  *                                       REMOTE IPL ( ALCUZ , HLCUZ )
00016                  *                                       FIXED HEAD DISK DDC
00017                  *
00018                  *           AND ALSO BY USE OF ONE OF THE LAST 64 WORDS OF BOOTSTRAP
00019                  *               AS VALUE OF REGISTER A15
00020                  *                                       AUTOMATIC IPL
00021                  *                                       AUTOMATIC RE-IPL (BATTERY OFF)
00022                  *
00023                  *
00024                          EJECT
00025                  *       THE CONFIGURATION OF REGISTER A15 IS AS FOLLOWS :
00026                  *
00027                  *       BITS
00028                  *
00029                  *       0=1                    INDICATES THE CU READING 16 BITS WORDS
00030                  *                              WHEN IT IS CONNECTED ON PROGRAMMED CHANNEL
00031                  *                              (FOR EX   FLOPPY DISK )
00032                  *
00033                  *       1=1                    DISK ON IOP OR PROGRAMMED CHANNEL
00034                  *       THEN  3=1              PROGRAMMED CHANNEL
00035                  *             3=0              IO PROCESSOR
00036                  *             2=1              MOVING HEADS
00037                  *             2=0              FIXED HEADS
00038                  *
00039                  *       1=0                    OTHER CASES
00040                  *       THEN  2=1              ROM IPL OR DMA
00041                  *             THEN   3=1       ROM IPL
00042                  *                              3=0 ; 0=1 ; 9=1  DMA UPL WITH CIO IPL
00043                  *                              3=0 ; 0=1 ; 9=0  FREE
00044                  *                              3=0 ; 0=0 ; 9=0  BIGD2
00045                  *                              3=0 ; 0=0 ; 9=1  NEW CU BIG DISC
00046                  *                                               NOT YET SPECIFIED
00047                  *
00048                  *             2=0              SEQUENTIAL DEVICES OR CDC DISK
00049                  *
00050                  *             2=0              SEQUENTIAL DEVICES
00051                  *                    3=1       PROGRAMMED CHANNEL
00052                  *                    3=0       IO PROCESSOR
00053                  *
00054                  *       9                      NOT SIGNIFICANT FOR BOOTSTRAP
00055                                                  BUT MUST BE SET FOR MOVING-HEAD DISKS
00056                                                  WITH ABSOLUTE SEEK
00057                                                  USING IPL OF X1215/1210 DISK
00058                  *
00059                  *       4 TO 7                 BIO LINES FOR CIO START
00060                  *                 -  0111              FOR K7
00061                  *                 -  1010              FOR MT
00062                  *                 -  0001              FOR BIG DISC WITH CIO IPL
00063                  *                 -  0000              SECTOR # CONTAINING IPL
00064                  *                                      FOR FLOPPY 1/4 MB
00065                  *                                            FHD
00066                  *                                            X1250
00067                  *                                            FLOPPY 1 MB
00068                  *                      - INTERLACE = SECTOR #   CONTAINING IPL
00069                  *                                    FOR X1250 /X1216
00070                  *                                    - 0000
00071                  *                      - 0000        FOR PAPER TAPE
00072                  *                                    FOR IPLRZ
00073                  *                      - BITS 4,5,6 = SECTOR # OF IPL      *
00074                  *                        BIT 7 = 0     MOVABLE PART        * FOR BIGD2
00075                  *                              7 = 1   FIXED PART          *
00076                  *
00077                  *
00078                  *     8=1                      MULTI DEVICE CONTROLLER
00079                  *     8=2                      SINGLE DEVICE CONTROLLER
00080                  *     10 TO 15                 DEVICE ADDRESS
00081                  *
```

```
00082                          EJECT
00083                  *
00084                  *       DESCRIPTION
00085                  *
00086                  *       NEWB10 LOADS THE IPL ( OR THE FIRST RECORD OF IPL )
00087                  *              AT ADDRESS IPLADD
00088                  *       THEN STARTS IT
00089                  *       LOADING ADDRESS + 4 GIVEN TO THE IPL IN A14
00090                  *       FOR DISC LIKE DEVICE THE RECORD IS SECTOR # (PHYSICAL SECTOR #
00091                  *       SPECIFIED BY MEANS OF BIO LINES )
00092                  *                              THE LENGTH IS LENGTH OF A X1215 SECTOR (205 WORDS)
00093                  *                                           OR LENGTH OF A FLOPPY SECTOR (64 WORDS)
00094                  *
00095                  *                                                    ( OR 128 WORDS )
00096                  *       FOR SEQUENTIAL DEVICES LENGTH IS IPLLEN CHARACTERS
00097                  *                                    LEADING CHARACTERS ARE IGNORED
00098                  *
00099                  *       FOR CDC DISK THE IPL SECTOR IS READ ON LOCATION 0
00100                  *                BRANCH TO IPL BEGINNING IS PERFORMED IN THE
00101                  *                FOLLOWING WAY : WHEN LOADING THE IPL INTO
00102                  *                MEMORY, THE BOOTSTRAP LOOPS AT ADDRESSES /7A-/7C
00103                  *                BUT AT THE SAME LOCATIONS THE IPL CONTAINS A BRANCH
00104                  *                TO ADDRESS /0000, WHICH WILL OVERWRITE THE BOOTSTRAP
00105                  *                LOOP.
00106                  *
00107                  *       FOR ROM IPL THE NEWBOO BRANCHS TO THE FIRST NOT NULL ROM
00108                  *                LOCATION AFTER /202
00109                  *
00110                  *       FOR DMA UPL SPECIAL BLOCKS ARE ALREADY PROVIDED , A SPECIAL
00111                  *                SEQUENCE PERFORMS CIO IPL AND STARTS LOADED IPL
00112                  *                AT ADDRESS SPECIFIED AT PREMARK TIME.
00113                  *                DIRECTLY ADDRESSABLE : IMPLAN
00114                  *                (ACTUALLY THE ADDRESS GIVEN AT PREMARK IS THAT
00115                  *                OF THE LAST LOCATION DIRECTLY ADDRESSABLE :
00116                  *                E.G. FOR 32K MEMORY, 'IMPLAN' = /FFFE )
00117                  *                IPL IS STARTED DIRECTLY AT LOADING ADDRESS.
00118                  *
00119                  *
00120                  *
00121                  *       THAT VERSION OF BOOTSTRAP IS COMPATIBLE WITH EXISTING IPL
00122                  *       SO       - IPLADD = LOADING ADDRESS OF IPL = /80
00123                  *                - IPLLEN = LENGTH OF A RECORD FOR = /50
00124                  *                           SEQUENTIAL DEVICES
00125                  *                - SOME PART OF CODING USE BY SOME IPL MUST BE
00126                  *                  AT THE SAME PLACE
00127                  *
00128                  IPLADD   EQU      /80                  LOADING ADDRESS OF IPL
00129                  IPLLEN   EQU      /50                  LENGTH OF A RECORD FOR
00130                                                          SEQUENTIAL DEVICES
00131                  *
00132                  *
00133                           EJECT
00134                           AORG     0
00135                  BOOT     EQU      *
00136  0000  5700  F             RF       BOOT00
00137                           EJECT
00138                  *
00139                  *       SOME IPL ( FOR K7 , PTR , FLOPPY 1/4 MB )
00140                  *       USE A PART OF BOOTSRAP TO LOAD FURTHER RECORDS OF IPL
00141                  *       TO BE COMPATIBLE WITH THEM
00142                  *       SOME INSTRUCTIONS MUST BE AT THE SAME ADDRESS AS IN PREVIOUS
00143                  *       BOOTSTRAPS
00144                  *                AT /3E       LDKL  A5,/80CD
00145                  *                AT /42       WER   A5,0
00146                  *                AT /5A       RF(4) INR10
00147                  *
00148                  *       MOREOVER THE LOADING ADDRESS OF IPL MUST BE /80
00149                  *       SO THE PART OF BOOTSRAP WHICH LOADS THE IPL
00150                  *       MUST BE LOADED BEFORE /80
00151                  *
00152                  *       REGISTERS
00153                  *
00154                  *       (A1)   =  REGISTER OF CIO START
00155                  *       (A2)   =  INR INST. ADDRESS
00156                  *       (A3)   =  CIO INST. ADDRESS
00157                  *       (A4)   =  SST INST. ADDRESS
00158                  *       (A5)   =  REMAINING # OF CHARACTERS (WORDS) TO BE READ ( PC )
00159                  *                 OR FIRST MULTIPLEX WORD ( IOP )
00160                  *       (A6       CURRENT ADDRESS OF CHARACTER (WORD) TO BE READ ( PC )
00161                  *                 OR SECOND MULTIPLEX WORD ( IOP )
00162                  *       (A7)   =  REGISTER OF INR OR SST
00163                  *       (A8)   =  START ADDRESS OF IPL
00164                  *       (A9)   =  FLAG USED IN PC. TO IGNORE LEADING CHARACTERS
00165                  *       (A10)  =  NOT USED
00166                  *       (A11)  =  NOT USED
00167                  *       (A12)  =  LOADING ADDRESS OF UPL PART OF BOOTSTRAP
00168                  *                 OR LOADING ADDRESS OF IPL BIG DISC WITHOUT CIO IPL
00169                  *       (A13)     USED IF UPL
00170                  *       (A14)     NOT USED
00171                  *       (A15)     INPUT REGISTER OF BOOTSTRAP
00172                  *
00173                  *
00174                  *
00175                  SSTCP    EQU      *                    SST FOR PROGRAMMED CHANNEL
00176  0002  F031              EXR*     A4                   LOOP  SST / INR
```

```
00177  0004  5400  F           RF(4)    INR
00178                  TSTSTA   EQU      *
00179  0006  A720              ANKL     A7,/4207
       0008  4207
00180                                                    13 =DATA FAULT
00181                                                    14 =THROUGHPUT ERROR
00182                                                    15 =NOT OPERABLE
00183  000A  5400  F           RF(4)    NEWIO
00184                                                 THEN START BOOTSTRAP AGAIN
00185                                                 FROM THE VERY BEGINNING.
00186                  BRANCH   EQU      *
00187  000C  8F02              ABR      A8                    BRANCH TO IPL
00188                  *
00189                  *
00190                  *
00191                  *
00192                  *        IO BLOCK OF COMMANDS FOR BIGD2 CONTROL UNIT
00193                  *
00194  000E  E000      BIGD20   DATA     /E000                 SEEK TO ZERO
00195  0010  0800      BIGD21   DATA     /800                  BIT 4 = 1 TO GET INTERRUPT
00196                                                          BITS 5 TO  10 = SECTOR #
00197                                                          BITS 11 TO 15  = HEAD #
00198  0012  00CD      BIGD22   DATA     /CD                   TOTAL LENGTH
00199  0014  00CD      BIGD23   DATA     /CD                   PARTIAL LENGTH
00200  0016  0000      BIGD24   DATA     0                     BUFFER ADDRESS MOST SIGNIF. BITS
00201  0018  0000      BIGD25   DATA     0                     BUFFER ADDRESS LEAST SIGNIF. BITS
00202                  *
00203                  *        IO BLOCK OF COMMANDS FOR FURTHER BIG DISC CONTROL UNIT
00204                  *
00205  001A                    RES      5
00206                  TSTA     EQU      *
00207  0024  A720              ANKL     A7,/4207              IF STATUS CORRECT
       0026  4207
00208  0028  5000  F           RF(0)    CIOSTA                   EXECUTE CIO START
00209                  NEWIO    EQU      *
00210  002A  871E              LDR      A7,A15
00211  002C  3FC1              SLC      A7,1                  DISK ?
00212  002E  5600  F           RF(6)    SEQUEN                NO : SEQUENTIAL OR CDC
00213                  *
00214                  *
00215                  *
00216                           AORG     /30
00217                  DISK     EQU      *                     DISK ON IOP OR PC
00218  0030  3FC1              SLC      A7,1                  MOVING HEADS ?
00219  0032  5600  F           RF(6)    NOSEEK                NO                              3A
00220  0034  0103              LDK      A1,3                  YES : PERFORM A CIO             3C
00221  0036  41C0      CIO      CIO      A1,1,0                SEEK TO CYLINDER 0
00222                  *
00223                  *  PREPARE NEXT IO ON DISK
00224                  *
00225                  NOSEEK   EQU      *
00226  0038  811E              LDR      A1,A15                GET                             40
00227  003A  3966              SRL      A1,6                  SECTOR #                        42
00228  003C  213C              ANK      A1,/3C                IN A1                           44
00229  003E  8520              LDKL     A5,/80CD              READ  205 (/CD) WORDS           46
       0040  80CD
00230                  *
00231                  * EXECUTE WER INSTRUCTIONS , WHATEVER THE CHANNEL IS
00232                  *
00233                  SEQUEN   EQU      *
00234                  WER1     EQU      *
00235  0042  7500              WER      A5,0                  INIT LENGTH OF THE BUFFER       4A
00236                  WER2     EQU      *
00237  0044  7601              WER      A6,1                  INIT LOADING ADDRESS            4C
00238                  DMACDC   EQU      *
00239  0046  F031              EXR*     A4          SST       TEST STATUS BEFORE CIO START    4E
00240  0048  5826              RB(0)    TSTA
00241                  CIOSTA   EQU      *
00242  004A  F02D              EXR*     A3          CIO                                       50
00243  004C  5C08              RB(4)    DMACDC                52
00244  004E  871E              LDR      A7,A15                                                54
00245  0050  3F43              SLL      A7,3                                                  56
00246  0052  5600  F           RF(6)    SST                   MULTIPLEX
00247                  *
00248                  *   PROGRAMMED CHANNEL
00249                  *
00250                  *        IF A9=A5 IGNORE LEADING CHARACTERS
00251                  INR      EQU      *
00252  0054  4F00              INR      A7,0,0      READ ONE CHAR                             5C
00253  0056  5C56              RB(4)    SSTCP       EXECUTE SST                               5E
00254  0058  E994              CWR      A9,A5       LEADING  CHAR ?                           60
00255  005A  5400  F           RF(4)    INR10       NO                                        62
00256  005C  871C              LDR      A7,A7       CHECK IF NULL                             64
00257  005E  580C              RB(0)    INR         YES : IGNORE                              66
00258                  *
00259                  INR10    EQU      *
00260  0060  879E              LDR      A15,A15     TEST IF CU 16 BITS ON PC.                 68
00261  0062  5600  F           RF(6)    STORE       NO : 8+8                                  6A
00262                  *
00263  0064  8739              STR      A7,A6       STORE WORD                                6C
00264  0066  1601              ADK      A6,1        INCREMENT CHARACTER ADDR                  6E
00265                  STORE    EQU      *
```

```
00266  0068  E739          SCR     A7,A6       STORE CHARACTER                    70
00267  006A  1601          ADK     A6,1        NEXT  CHARACTER ADDR               72
00268  006C  1D01          SUK     A5,1        COUNT DONE ?                       74
00269  006E  5C1C          RB(4)   INR         NO                                 76
00270                *                          YES :CIO HALT
00271  0070  0700          LDK     A7,0
00272  0072  4780    HIO   CIO     A7,0,0
00273  0074  5700  F       RF      SST
00274                *
00275                *       FOR IPL FROM CDC LOOP UNTIL SST ACCEPTED AT @ /7A
00276                *
00277  0076                RES     2
00278                       AORG    /7A
00279                SST    EQU     *
00280  007A  4FC0          SST     A7,0                LOOP UNTIL SST ACCEPTED
00281  007C  5C04          RB(4)   *-2
00282  007E  5F7A          RB      TSTSTA              TEST STATUS
00283                *
00284                *       /80     ADDRESS OF AWORD FOR UPL RESTART
00285                *
00286  0080  0000  F         DATA    HARD
00287                BOOT00  EQU     *
00288  0082  8720            LDKL    A7,/AAAA            PATTERN TO BE CHECKED
       0084  AAAA
00289  0086  84A0            LDKL    A12,/F800           STACK
       0088  F800
00290                B00010  EQU     *
00291  008A  8733            STR     A7,A12
00292  008C  EF32            CWR*    A7,A12
00293  008E  5000  F         RF(0)   B00020
00294  0090  9CA0            SUKL    A12,/1000
       0092  1000
00295  0094  5F0C            RB      B00010
00296                B00020  EQU     *                   MOVE BOOT UPL TO HIGH-CORE
00297  0096  8120            LDKL     A1,BASE+0           BEGIN OF BOOT
       0098  0000  F
00298  009A  8212            LDR     A2,A12
00299  009C  8320            LDKL    A3,LIMIT-BASE       LENGTH OF BOOT
       009E  0000  F
00300                B0030   EQU     *
00301  00A0  8424            LDR*    A4,A1
00302  00A2  8429            STR     A4,A2
00303  00A4  1202            ADK     A2,2
00304  00A6  1102            ADK     A1,2
00305  00A8  1B02            SUK     A3,2
00306  00AA  590C            RB(1)   B0030
00307                *
00308                *  BASE REGISTERS INITIALIZATION
00309                *
00310                INIT10  EQU     *
00311  00AC  0254            LDK     A2,INR              (A2) = INR @
00312  00AE  0336            LDK     A3,CIO              (A3) = CIO @
00313  00B0  047A            LDK     A4,SST              (A4) = SST @
00314                *
00315                *  GET DEVICE ADDRESS TO INITIALIZE THE  I/O COMMANDS
00316                *
00317  00B2  861E            LDR     A6,A15      A6 = KEYS VALUE                    6
00318  00B4  263F            ANK     A6,/3F      KEEP JUST DEVICE ADDRESS           8
00319  00B6  AE29            ORRS    A6,A2       INIT INR INST WITH DA              A
00320  00B8  AE2D            ORRS    A6,A3            CIO                           C
00321  00BA  AE41            ORS     A6,HIO                HIO
       00BC  0072
00322                *
00323                * GET CONTROLLER TYPE AND ADDRESS.
00324                *
00325  00BE  871E            LDR     A7,A15      MULTIPLE OR SINGLE                 12
00326  00C0  3FC8            SLC     A7,8        DEVICE CONTROLLER ?                14
00327  00C2  5600  F         RF(6)   INIT20      IF SINGLE BRANCH                   16
00328  00C4  260F            ANK     A6,/F       KEEP THE DEVICE CONTROLLER ADDRESS 18
00329                *
00330                * INITIALIZE THE WER INSTRUCTIONS AND SST ONE.
00331                *
00332                INIT20  EQU     *
00333  00C6  AE31            ORRS    A6,A4               SST INSTRUCTION            1A
00334  00C8  3E41            SLL     A6,1                CHANNEL AND SUBCHANNEL VALUES 1C
00335  00CA  AE41            ORS     A6,WER1             IN WER
       00CC  0042
00336  00CE  AE41            ORS     A6,WER2             INSTRUCTIONS
       00D0  0044
00337  00D2  811C            LDR     A1,A7               LOAD A1 WITH BIO CONTENTS  22
00338  00D4  0550            LDK     A5,IPLLEN           (A5) = LENGTH TO BE LOADED
00339  00D6  8194            LDR     A9,A5               USED FOR LEADING CHARACTERS
00340  00D8  8620            LDKL    A6,IPLADD           LOADING ADDRESS OF IPL
       00DA  0080
00341  00DC  8098            LDR     A8,A6
00342  00DE  90A0            ADKL    A8,4                (A8)  = START ADDRESS OF IPL
       00E0  0004
00343  00E2  8698            LDR     A14,A6              (A14) = LOADING AADDRESS OF IPL
00344                *
00345                * CHECK DEVICE TYPE
00346                *
```

```
00347  00E4  3FE7            SRC     A7,7                IS IT DISK ON IOP OR PC ?          2A
00348  00E6  5AB8            RB(2)   DISK                YES                                2C
00349  00E8  3FC1            SLC     A7,1                ROM IPL OR DMA UPL ?
00350  00EA  5EAA            RB(6)   SEQUEN              NO: INIT WER                       30
00351  00EC  3FC1            SLC     A7,1                YES : ROM IPL ?
00352  00EE  5200  F         RF(2)   ROMIPL              YES
00353  00F0  3FE3            SRC     A7,3                BIG DISC ?
00354  00F2  5600  F         RF(6)   BIGDIS              YES
00355  00F4  8112            LDR     A1,A12              NO : BRANCH TO BOOT UPL
00356  00F6  1100  F         ADK     A1,DMAUPL-BASE      IN HIGH-CORE
00357  00F8  8F04            ABR     A1                  (A12) = LOADING ADDRESS
00358                        EJECT
00359                 BIGDIS  EQU     *
00360                 *
00361                 *       2 TYPES OF BIG DISC CONTROL UNIT WITHOUT CIO IPL
00362                 *               - BIGD2
00363                 *               - OTHER NOT YET SPECIFIED
00364                 *
00365  00FA  3FC9            SLC     A7,9                BIGD2 ?  (BIT 9 = 0 )
00366  00FC  5200  F         RF(2)   BIGNEW              NO
00367                 BIGD2   EQU     *
00368                 *
00369                 *       FOR CU BIGD2 2 TYPES OF DRIVES
00370                 *               SMD         1 PART    AMOVIBLE       BIT  7 = 0
00371                 *
00372                 *               CMD         2 PARTS   1 FIXED        BIT  7 = 1
00373                 *                                     1 AMOVIBLE     BIT  7 = 0
00374                 *
00375                 *               BITS  4,5,6  GIVE SECTOR NUMBER
00376                 *
00377  00FE  3FC3            SLC     A7,3                PUT SECTOR #   BITS 4,5,6
00378  0100  27F0            ANK     A7,/F0                  VOLUME #   BIT  7
00379  0102  AF41            ORS     A7,BIGD21           IN  BLOCK OF COMMANDS
       0104  0010
00380                                                        BITS  8 9 10 11
00381  0106  010E            LDK     A1,BIGD20           (A1) = ADDRESS OF BLOCK OF
00382                                                          COMMANDS
00383  0108  5FC4            RB      DMACDC              START LOADING
00384                 *
00385                 *       SEQUENCE  FOR NEW CONTROLLER BIG DISC
00386                 *
00387                 BIGNEW  EQU     *
00388  010A  5F0E            RB      BIGD2
00389                 *
00390                         EJECT
00391                 ROMIPL  EQU     *
00392                 *
00393                 *  FETCH FOR THE FIRST LOCATION ROM , NOT NULL ,FROM ADD /202
00394                 *  AND  BRANCH TO IT
00395                 *
00396  010C  8620            LDKL    A6,/200
       010E  0200
00397                 LOOP    EQU     *
00398  0110  1602            ADK     A6,2
00399  0112  8618            LDR     A6,A6                LOOP IF NO ROM
00400  0114  5802            RB(0)   *
00401  0116  8238            LDR*    A2,A6           TAKE CONTENTS OF CURRENT LOCATION      90
00402  0118  580A            RB(0)   LOOP                ROM CONTENT =0 NOT SIGNIFICANT VALUE  92
00403  011A  9039            IMR     A6                  TRY TO MODIFY THE CURR MEMORY      94
00404  011C  EA38            CWR*    A2,A6           TEST IF STORE WAS SUCCESSFULL          96
00405  011E  8818            ABR(0)  A6              NO  THE LOCATION CONTENTS NOT CHANGED  98
00406                                                      BRANCH TO IT                       9A
00407  0120  8239            STR     A2,A6               RESTORE PREVIOUS CONTENTS          9C
00408  0122  5F14            RB      LOOP                GO TO TEST NEXT LOCATION           9E
00409                         EJECT
00410                 *
00411                 *     DMA UPL
00412                 *
00413                 HARD    EQU     /100
00414                 *       BIT 0 AT LOCAATION /100 MUST BE 0
00415                 BASE    EQU     *
00416                 CSD     EQU     *
00417  0124  0000            DATA    0                   CID ADDRESS  0  ,  1
00418  0126  0000            DATA    0                   CID ADDRESS  2  ,  INTD = ****
00419  0128  0000            DATA    0           INTS = ****     ,  0                       A4
00420                 CID     EQU     *
00421  012A  0000            DATA    0                   IOD ADD OUT  0  ,  1
00422  012C  0000            DATA    0                   IOD ADD OUT  2  ,  IOD ADD IN 0
00423  012E  0000            DATA    0                   IOD ADD IN  1  ,  2
00424  0130  0000  ITSPEC    DATA    0           INT SPEC        ,  RDN IN                  AC
00425  0132  0000            DATA    0           PAI CODE        ,  0                       AE
00426                 IOD     EQU     *
00427  0134  0082            DATA    /82                 RDN OUT      , COM= /82 (IPL)
00428  0136  0000  LOGSTA    DATA    0                   LOGICAL STATUS
00429  0138  0000  PHYSTA    DATA    0           PHYSICAL STATUS                            B4
00430  013A  0000            DATA    0                   IO AREA LENGTH
00431  013C  0000            DATA    0                                                      B8
00432  013E  0000  MEDCAR    DATA    0                   MEDIUM CHARACTERS ,  *
00433  0140  0000            DATA    0           **              ,  IO AREA ADD  0          BC
00434  0142  0000  IOAREA    DATA    0                   IO AREA ADD  1  ,  2
00435  0144  0000            DATA    0           REL SECT #   0  ,  1                      C0
00436  0146  0000  RSN       DATA    0           REL SECT #   2  ,  **                     C2
```

```
00437  0148  0000                DATA    0,0,0,0,0,0
       014A  0000
       014C  0000
       014E  0000
       0150  0000
       0152  0000
00438                    IODEND  EQU     *
00439                    DMAUPL  EQU     *
00440                    *
00441                    *       INIT CSD BLOCK WITH CID ADDRESS
00442                    *       AND CID BLOCK WITH IOD ADDRESS
00443                    *       THE ADDRESS FOR UPL IS ON 3 OCTADS
00444                    *       PUT IN A13 CSD BLOCK ADDRESS TRANSMITTED TO IPL
00445                    *
00446  0154  E592                ECR     A13,A12
00447  0156  E5D3                SC      A13,CSD+1-BASE,A12
       0158  0001
00448  015A  0106                LDK     A1,CID-BASE
00449  015C  E153                SC      A1,CSD+2-BASE,A12
       015E  0002
00450  0160  E5D3                SC      A13,CID+1-BASE,A12
       0162  0007
00451  0164  0110                LDK     A1,IOD-BASE
00452  0166  E153                SC      A1,CID+2-BASE,A12
       0168  0008
00453  016A  8592                LDR     A13,A12
00454  016C  E5D2                LC      A13,CSD+2-BASE,A12
       016E  0002
00455  0170  0100                LDK     A1,CSD-BASE             PUT CSD BLOCK ADDRESS
00456  0172  9112                ADR     A1,A12
00457  0174  8220                LDKL    A2,HARD                 AND HARD BLOCK @
       0176  0100
00458  0178  B941                MS      2,/80                   INTO LOCATION /80 AND /82
       017A  0080
00459  017C  E11E                ECR     A1,A15
00460  017E  8204                LDR     A2,A1
00461  0180  210F                ANK     A1,/F                   BITS  4,5,6,7  OF A15
00462  0182  3944                SLL     A1,4                    ARE BITS  0,1,2,3 OF
00463  0184  E153                SC      A1,MEDCAR-BASE,A12      MEDIUM CHARACTERS
       0186  001A
00464  0188  3A6E                SRL     A2,14                   BITS 8, 9 OF A15 ARE RELATIVE
00465  018A  3A48                SLL     A2,8                    DEVICE NUMBER
00466  018C  2A82                ORK     A2,/82                  IPL COMMAND CODE
00467  018E  8253                ST      A2,IOD-BASE,A12         --> IOD
       0190  0010
00468  0192  821E                LDR     A2,A15                                                  D6
00469  0194  223F                ANK     A2,/3F                  PUT DMA UPL ADDRESS             D8
00470  0196  AA53                ORS     A2,CIOUPL-BASE,A12
       0198  0000  F
00471  019A  A053                CM      ITSPEC-BASE,A12         CLEAR INTERRUPTS FIELD
       019C  000C
00472  019E  41C0       CIOUPL   CIO     A1,1,0                  CIO IPL
00473                    TSTIT    EQU     *
00474  01A0  E652                LC      A6,ITSPEC-BASE,A12      LOOP UNTIL
       01A2  000C
00475  01A4  2620                ANK     A6,/20                  END OF IO
00476  01A6  5808                RB(0)   TSTIT
00477  01A8  8152                LD      A1,PHYSTA-BASE,A12      TEST STATUS  PHYSTA
       01AA  0014
00478  01AC  A952                OR      A1,LOGSTA-BASE,A12            AND    LOGSTA
       01AE  0012
00479  01B0  5C5E                RB(4)   DMAUPL                  IF ONE OF THESE BITS SET
00480  01B2  8F52                ABI     IOAREA-BASE,A12         BRANCH TO LOAD ADDRESS
       01B4  001E
00481                    *       EJECT
00482                    *
00483                    *     16 WORDS ARE RESERVED AT END OF BOOTSTRAP
00484                    *     THEIR CONTENTS ARE LOADED AT IPL IN REGISTER A15
00485                    *     TO CHOOSE THE VALUE, THE HARDWARE USES AS INDEX
00486                    *        (WORD 0 IS THE LAST ONE AT LOCATION /1FE)
00487                    *        (WORD 15 IS THE FIRST ONE AT LOCATION /1E0)
00488                    *        THE VALUE OF A WHEEL WITH INDEXES FROM 0 TO /F
00489                    *
00490                    *                 OR STRAPS WITH INDEXES FROM  0 TO   7    3 STRAPS
00491                    *                                         OR   0 TO / F    4 STRAPS
00492                    *
00493                    *
00494                    *     THIS WAY OF LOADING A15 IS USED WHEN IPL IS NOT DONE
00495                    *     FROM A CONTROL PANEL
00496                    *                              - AUTOMATIC IPL
00497                    *                              - AUTOMATIC RE-IPL  (BATTERY OFF)
00498                    *                              - REMOTE IPL
00499                    *
00500                          AORG    /1E0
00501  01E0  FFFF              DATA    /FFFF     DMA UPL                                  15
00502  01E2  2116              DATA    /2116               CMD FIXED PART                 14
00503  01E4  65E2              DATA    /65E2               X1215 FIXED DISC INTERFACE 5   13
00504  01E6  2056              DATA    /2056               NEW CU BIG DISC EUROBOARD      12
00505  01E8  2016              DATA    /2016               CMD CARTRIDGE OR SMD           11
00506  01EA  0116              DATA    /0116     CDC                    0                10
00507  01EC  400A              DATA    /400A               FHD DISC                        9
00508  01EE  103F              DATA    /103F     IPLRZ                                    8
00509  01F0  0785              DATA    /0785     K7          IOP        0                 7
00510  01F2  3000              DATA    /3000     ROM IPL                                  6
00511  01F4  150D              DATA    /150D     REMOTE IPL                               5
00512  01F6  63C2              DATA    /63C2     X1215     3 CARTRIDGE      0             4
00513  01F8  60C1              DATA    /60C1                 X1250 DISC                   3
00514  01FA  6083              DATA    /6083     FLOPPY 1MB               0             2
00515  01FC  4083              DATA    /4083               FLOPPY IOP 1/4 MB              1
00516  01FE  1020              DATA    /1020               PTR                            0
00517                    LIMIT   END     BOOT
```

```
          SYMBOL TABLE

  IPLADD  0080  A   IPLLEN  0050  A   BOOT    0000  A   BOOT00  0082  A
  SSTCP   0002  A   INR     0054  A   TSTSTA  0006  A   NEWIO   002A  A
  BRANCH  000C  A   BIGD20  000E  A   BIGD21  0010  A   BIGD22  0012  A
  BIGD23  0014  A   BIGD24  0016  A   BIGD25  0018  A   TSTA    0024  A
  CIOSTA  004A  A   SEQUEN  0042  A   DISK    0030  A   NOSEEK  0038  A
  CIO     0036  A   WER1    0042  A   WER2    0044  A   DMACDC  0046  A
  SST     007A  A   INR10   0060  A   STORE   0068  A   HIO     0072  A
  HARD    0100  A   BOO010  008A  A   BOO020  0096  A   BASE    0124  A
  LIMIT   0200  A   BOO30   00A0  A   INIT10  00AC  A   INIT20  00C6  A
  ROMIPL  010C  A   BIGDIS  00FA  A   DMAUPL  0154  A   BIGNEW  010A  A
  BIGD2   00FE  A   LOOP    0110  A   CSD     0124  A   CID     012A  A
  ITSPEC  0130  A   IOD     0134  A   LOGSTA  0136  A   PHYSTA  0138  A
  MEDCAR  013E  A   IOAREA  0142  A   RSN     0146  A   IODEND  0154  A
  CIOUPL  019E  A   TSTIT   01A0  A

          ASS.ERR.    00000
:EOF

EXIT CODE= /00
SKP
```

1.15 DATA TRANSFER PROCEDURES

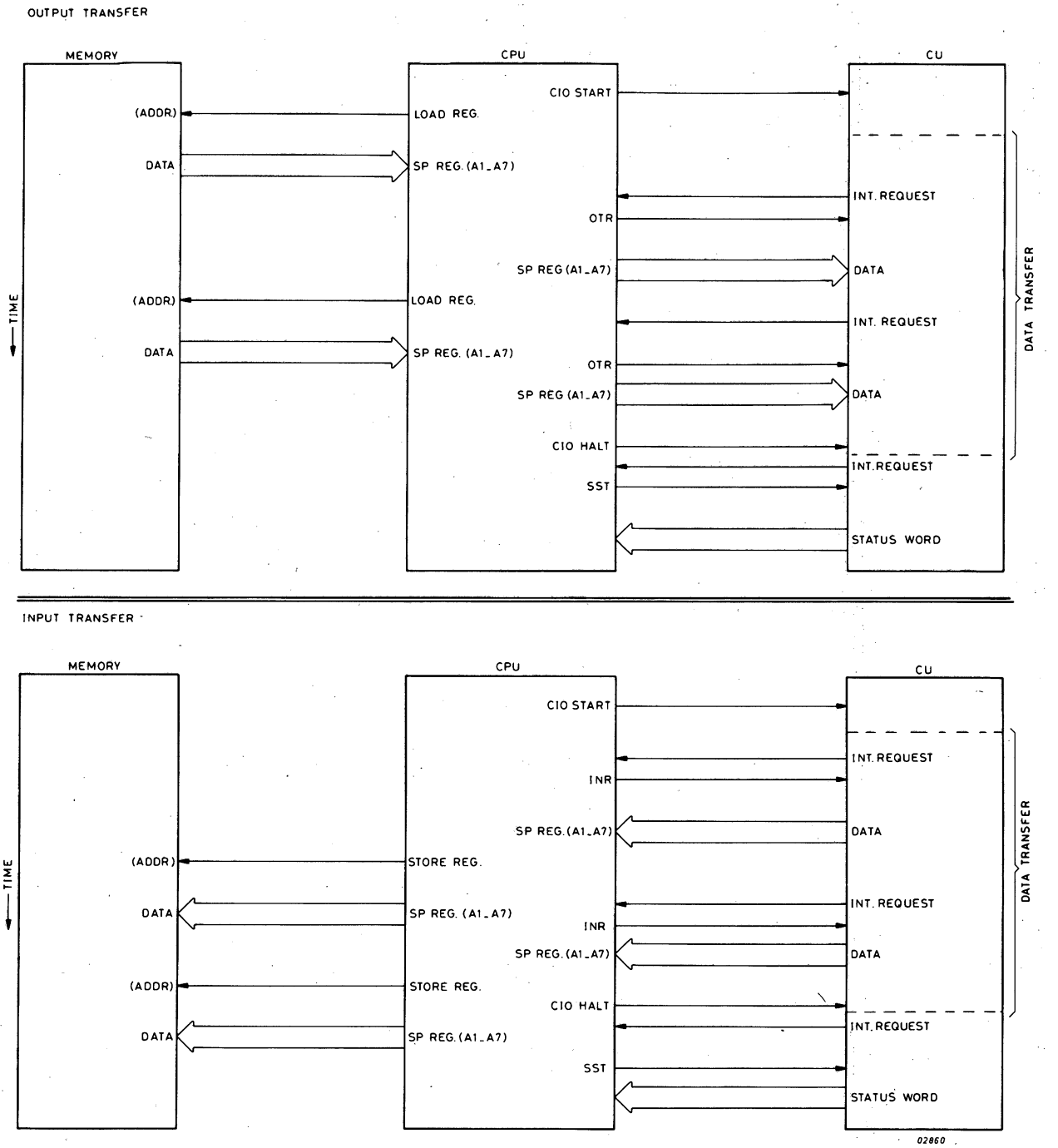
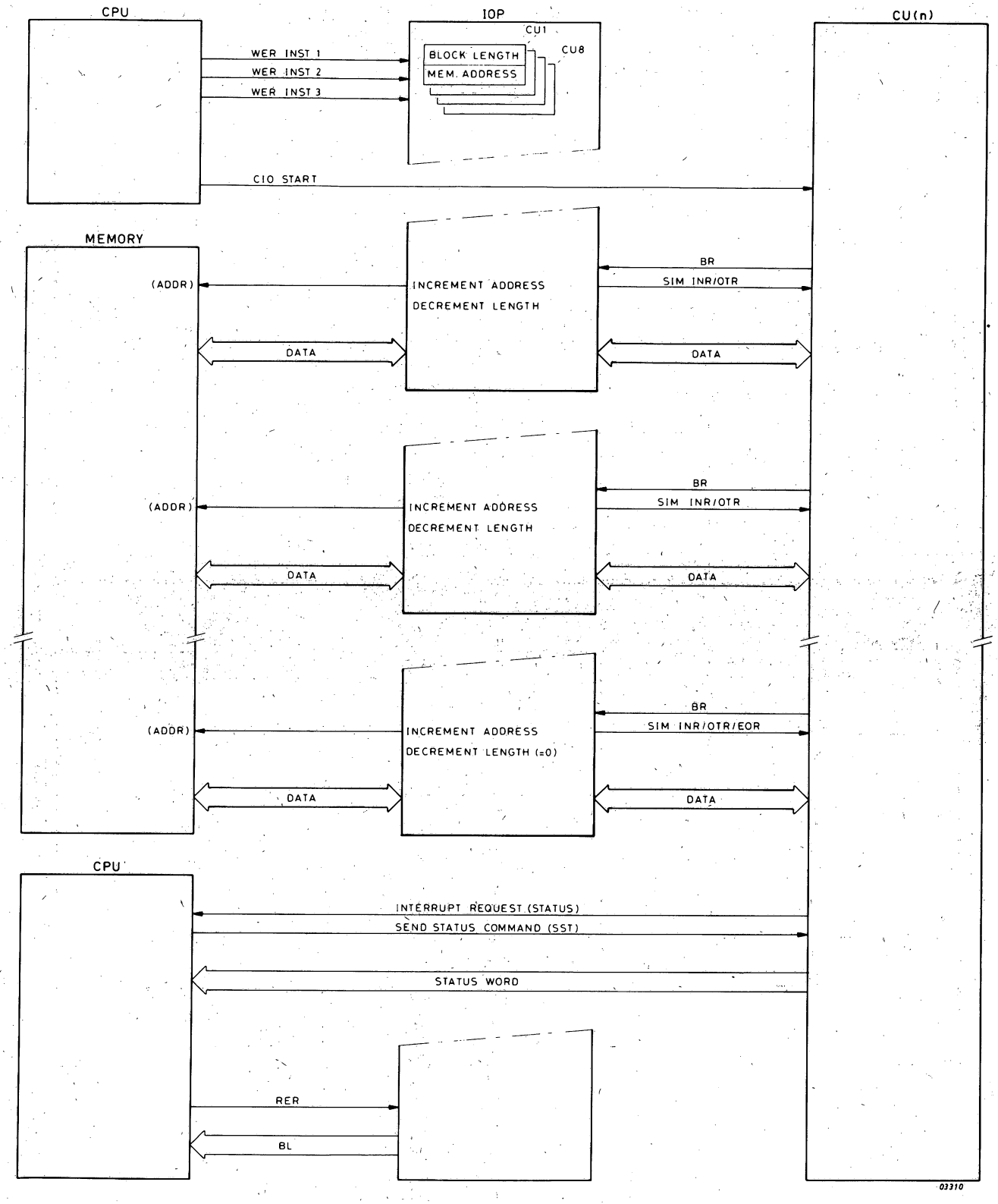


Figure 1.17 INPUT AND OUTPUT PROGRAMMED CHANNEL TRANSFERS



Note: WER 1,2 and 3 must be executed in this order.

Figure 1.18 IOP CHANNEL TRANSFERS

DIRECT MEMORY ACCESS CHANNEL

The DMA Channel enables a high speed control unit to make direct exchanges with memory. The following figure shows the sequence of events for a DMA transfer. The principle of operation is the same as for the IOP but as only one device is used the IOP/CU function is incorporated in the DMACU.

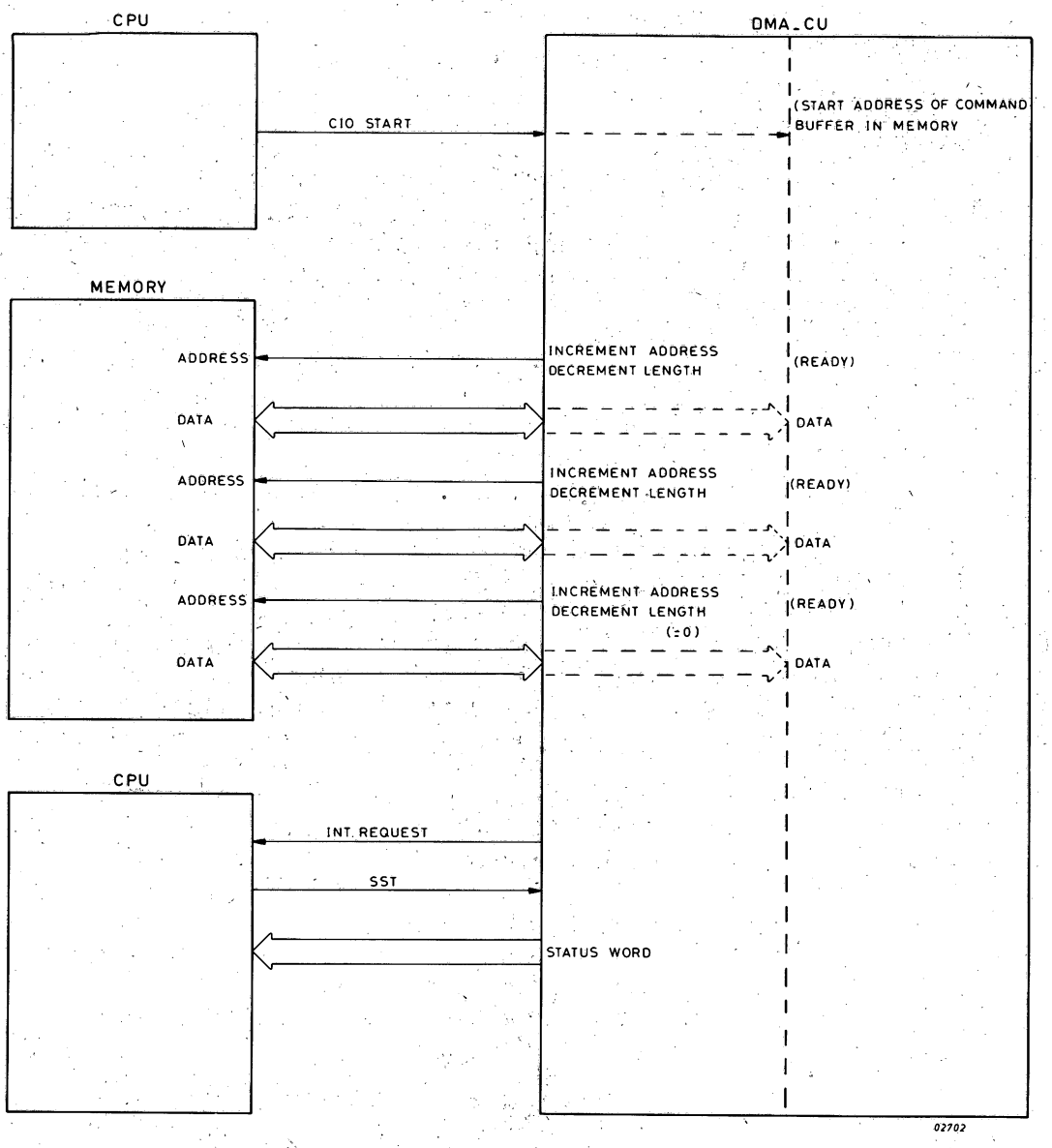


Figure 1.19 DIRECT MEMORY ACCESS CHANNEL TRANSFER

1.16 BASIC SYSTEM TYPES

BASIC SYSTEMS

In the P800 series "Basic Systems" have been defined.
A basic system consists of:

- a mounting box (rack) with a certain number of slots in which memory cards and control units can be inserted
- an integrated power supply unit
- a control panel and/or control panel interface
- a CPU-card- or cardset

The basic systems as described below do not contain any memory except for P853-257. However, for reasons of system responsibility no systems without memory can be delivered, unless a special arrangement with the customer has been made. In some cases a basic system is equipped with a battery pack and logic for power supply during power failure and with a filter option.
Mounting gear for standard 19" cabinets is supplied with all basic systems.

TYPE NUMBER	DESCRIPTION
P853-200	P853 Basic System with 5 free general purpose slots, incl. control panel interface hand held control panel
P853-257	P853 Basic System with 5 free general purpose slots incl. 32K 16-bit words of memory, access time 0.58us, and control panel interface for hand held control panel.
P853-300	P853 Basic System with 11 free general purpose slots, incl. control panel interface for hand held control panel
P853-357	P853 Basic System with 11 free general purpose slots, incl. 32K 16-bit words of memory, access time 0.58 us, and control panel interface for hand held control panel. models: P853-xxx/11 incl. filter P853-xxx/41 incl. filter and battery
P854-300	P854 Basic System with 9 free general purpose slots, incl. control panel interface for either hand held control panel or extended digital control panel. A ventilation unit is mandatory if the system is mounted in a cabinet, otherwise it is strongly recommended. models: P854-300/41 not equipped for slave-memories, incl. filter board and battery P854-300/51 not equipped for slave-memories, incl. filter board and 2 batteries P854-302/41 equipped for 2 slave-memories, incl. filter board and battery P854-302/51 equipped for 2 slave-memories, incl. filter and 2 batteries P854-304/41 equipped for 4 slave-memories, incl. filter and battery P854-304/51 equipped for 4 slave-memories, incl. filter board and 2 batteries
P854-400	P854 Basic Systen with 20 free general purposes slots incl. power supplies PSUB and PSUM, battery back-up, filter board ventilation unit and control panel interface for either hand held control panel or extended digital control panel. models: P854-400 not equipped for slave-memories P854-404 equipped for 4 slave-memories P854-408 equipped for 8 slave-memories

BASIC SYSTEM COMPONENTS

	P851	P853 -x00	P853 -x57	P854
Racks: Eurorack	-100			
6U6G rack	-200			
6U6U rack		-200	-257	
RU12 rack		-300	-357	-300
RU22 rack				-400
CPU's: CPSZ-card	x			
CP1L-card		x		
CP1A-card			x	
C7E1-, C7E2-, MIOP-card (P857E-cards)				x

1.17 BASIC SYSTEM POWER CHARACTERISTICS

Type Number	Free slots	Mounting Code	power available (in Amp) logic- +5V	logic- +12V	logic- -12V	memory- +5V	memory- +12V
P851-100	12	rack 6U	12.2	2.0	1.2	1.2	.9
P851-200	5	rack 6U	11.2	1.0	.5	1.5	.9
P853-200	5	rack 6U	11.8	1.5	.5	1.5	.9
P853-200	5	rack 6U	11.2	1.4	.5	.8	.4
P853-300	11	rack 6U	25.8	3.0	1.0	1.5	.9
P853-357	11	rack 6U	25.2	2.9	1.0	.8	.4
P854-300	9	rack 6U	19.2	2.9	1.0	1.5	.9
P854-400	20	rack RU22	31.2	1.4	1.0	2.5	1.4

Remark: The number of U(nits) denotes the height of the rack.
Standard 19" cabinets exist with a height of either 33U or 24U. Of all equipment to be mounted in the cabinet, mentioned in this catalogue, the height in units is given. Loose panels with heights of 1U, 3U, 5U, or 7U are available to close the cabinet.
1U is 1.75 (44.45).
The RU22 Rack is standard 6U, but including ventilation units and Control Panel this is 10U.

2 CABINETS

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	2.7	EXTENSION CABINET DISTRIBUTION PANEL	2-9
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2.1 INTRODUCTION BASIC AND EXTENSION CABINETS

The Basic cabinet comprises a 19" rack with a usable depth of 700mm (27.5 inches) and a mounting height of 36 standard units enclosed by side panels and a rear door (the extension cabinets have the same characteristics except they have no side panels).

A mounting kit is required for cabinets that have moving head disc units fitted. It comprises a new rear door containing a ventilation unit, and a pedestal to be fitted at the front of the cabinet (see figure 2.1).

2.2 MOUNTING DEVICES

The different mounting devices include:

. Telescopic slides for the Magnetic Tape Formatter and moving head disc drives.
. Mounting Hinges for the Magnetic Tape Transport.
. Fixed slides.

Some units such as the card Mounting Box are fitted directly to the rack by screws.

2.3 FRONT PANELS

Front panels of either 1, 3, 5 or 7 rack units are available to fill the spaces not used (or cover items like equipment shelves) in the cabinet.

2.4 VENTILATION UNITS

Convection cooling is sufficient if the total heat dissipation of the equipment in the cabinet is less than 700 kcal/h (800 watts). Above this level forced air circulation by one of the following ventilation units is necessary. Both units are similar except for the number of fans and the unit needs 1U space in the cabinet. The heat dissipation capabilities of the units are:

- P849-040 between 700 and 1030 kcal/h (800 to 1200 watts)
- P849-041 between 1030 and 1300 kcal/h (1200 to 1500 watts)

Figure 2.2 shows the two Ventilator Units.

2.5 POWER DISTRIBUTION PANELS

Two types of distribution panels are available to suit different power consumption levels. Both panels are 2U high and have a mains filter, mains isolation switch, neon indicator, fuse and terminal block. The current carrying capacities are:

- P849-042 10 amperes
- P849-043 25 amperes

The panels and their circuits are shown in the figures 2.3 to 2.7.

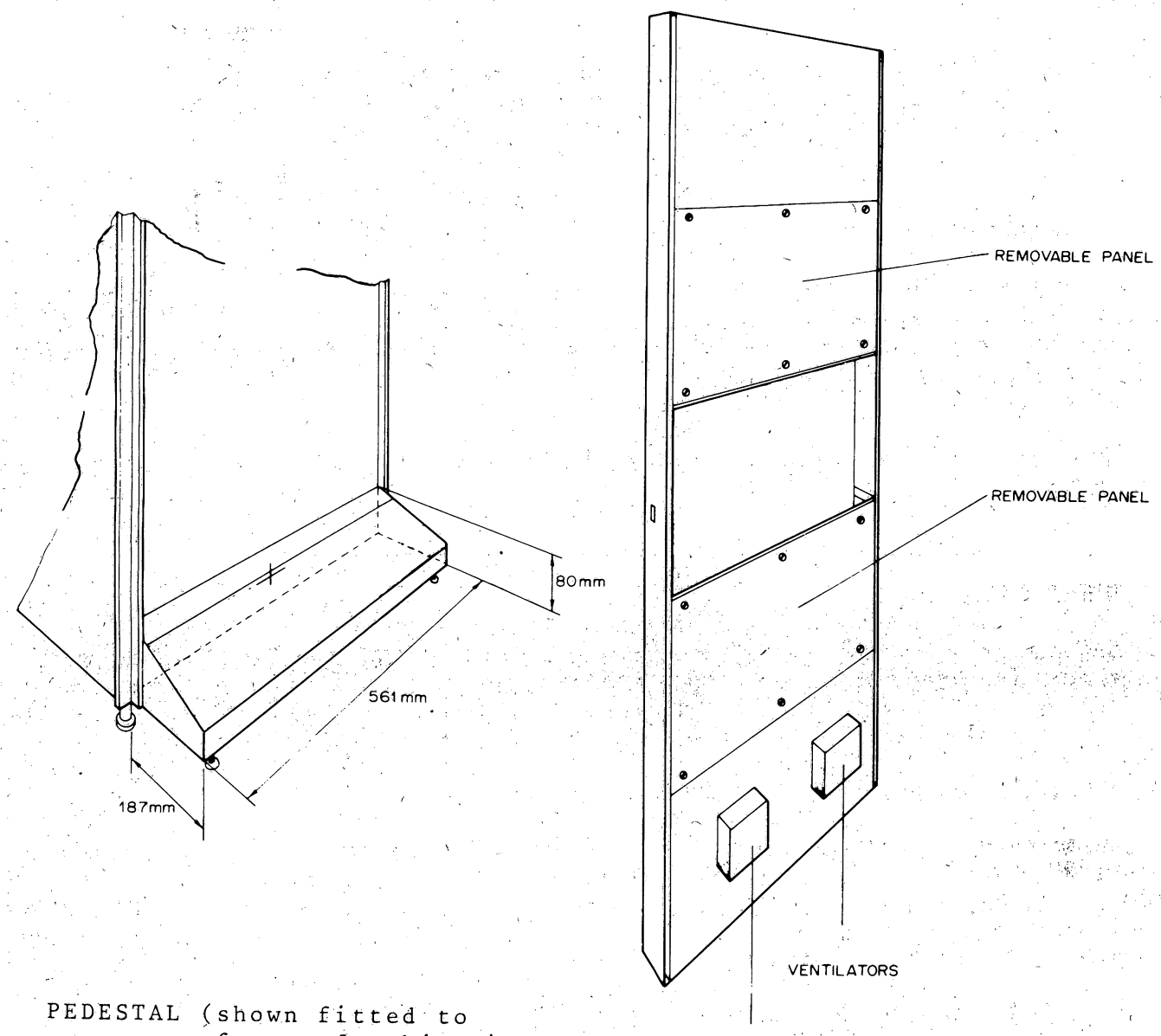
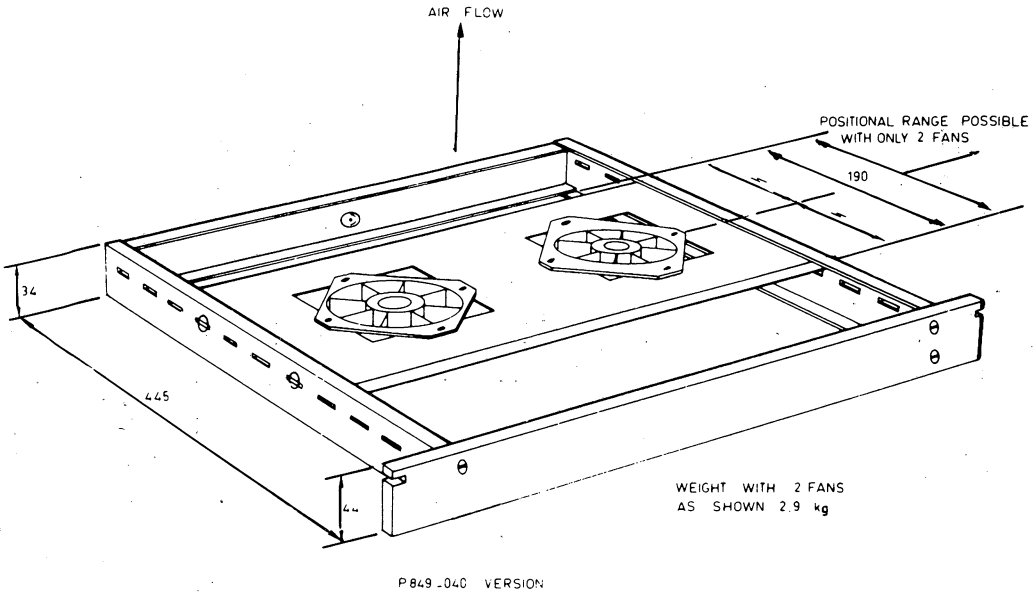
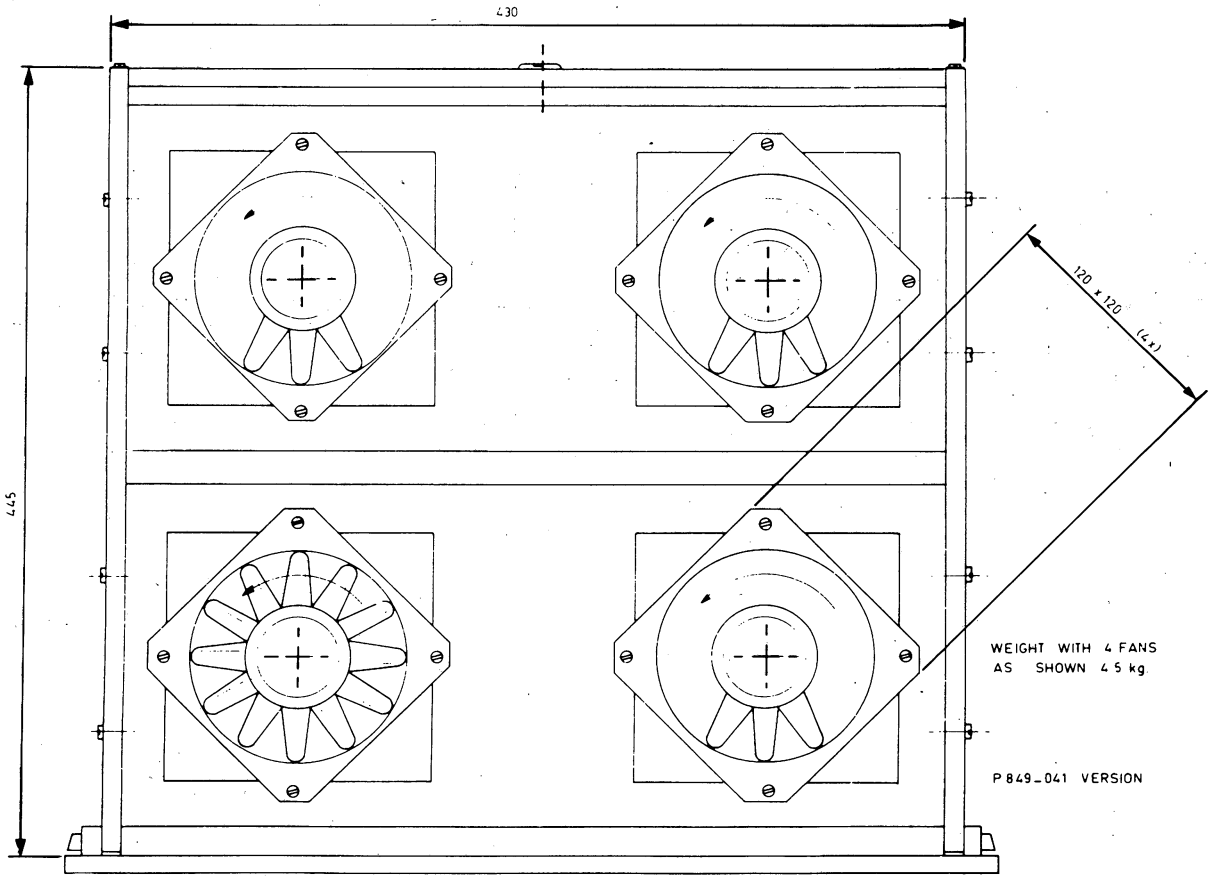


Figure 2.1 MOUNTING KIT (P849-039)





All dimensions are in mm

VENTILATOR UNITS ARE SUPPLIED WITH FIXED SLIDES

Figure 2.2 VENTILATOR UNITS

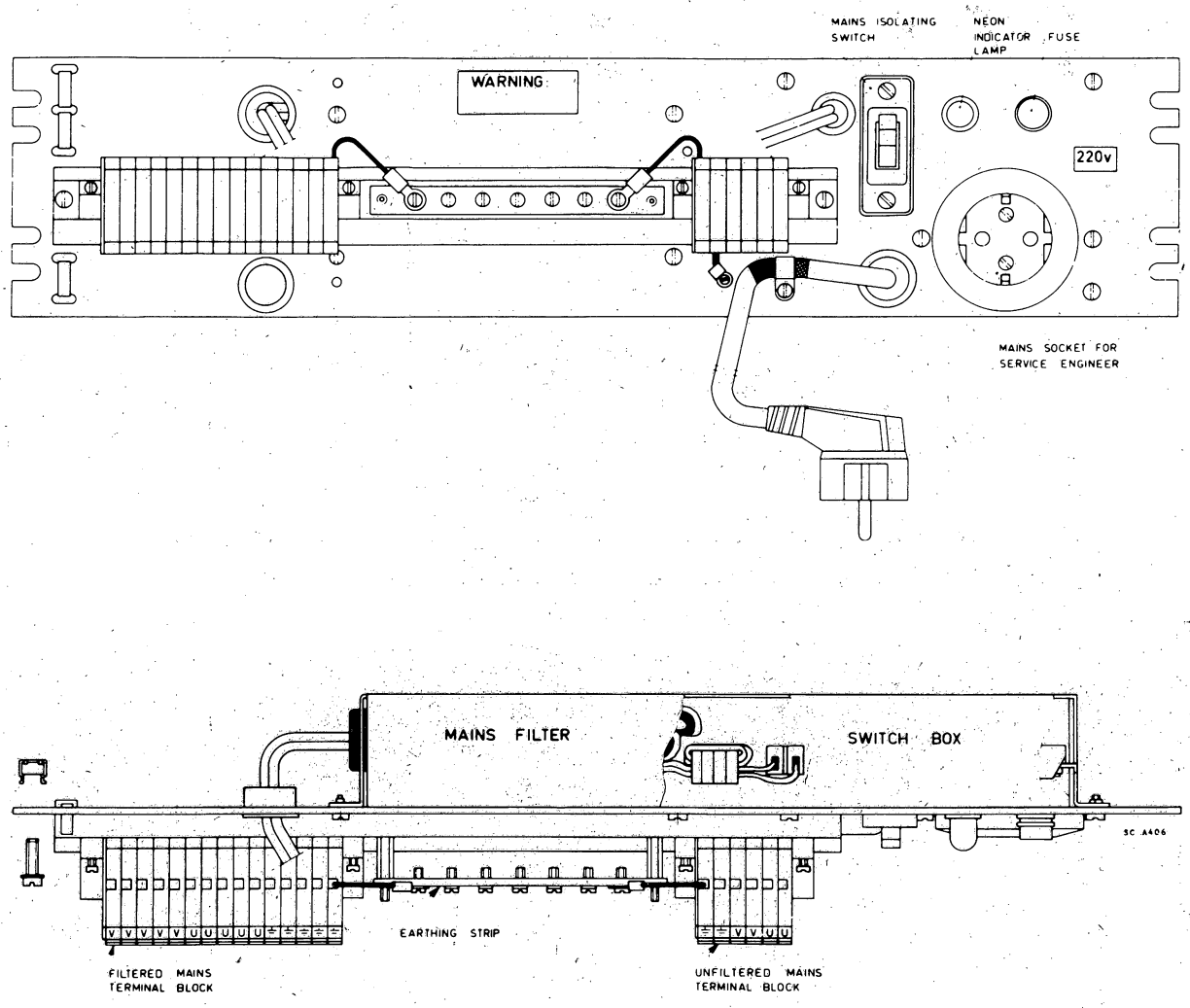


Figure 2.3 10 AMPERE DISTRIBUTION PANEL

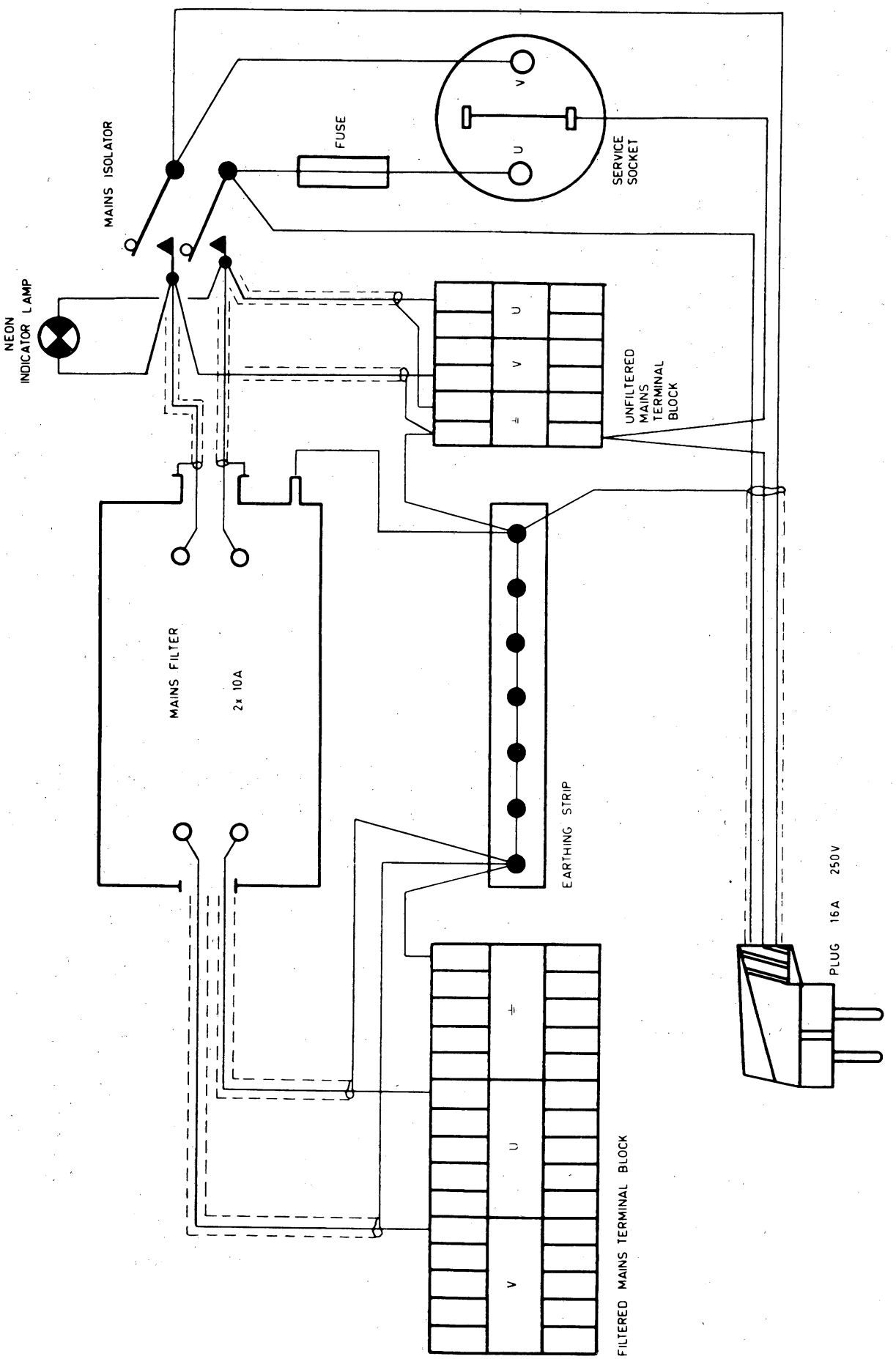


Figure 2.4 10 AMPERE DISTRIBUTION PANEL, CIRCUIT

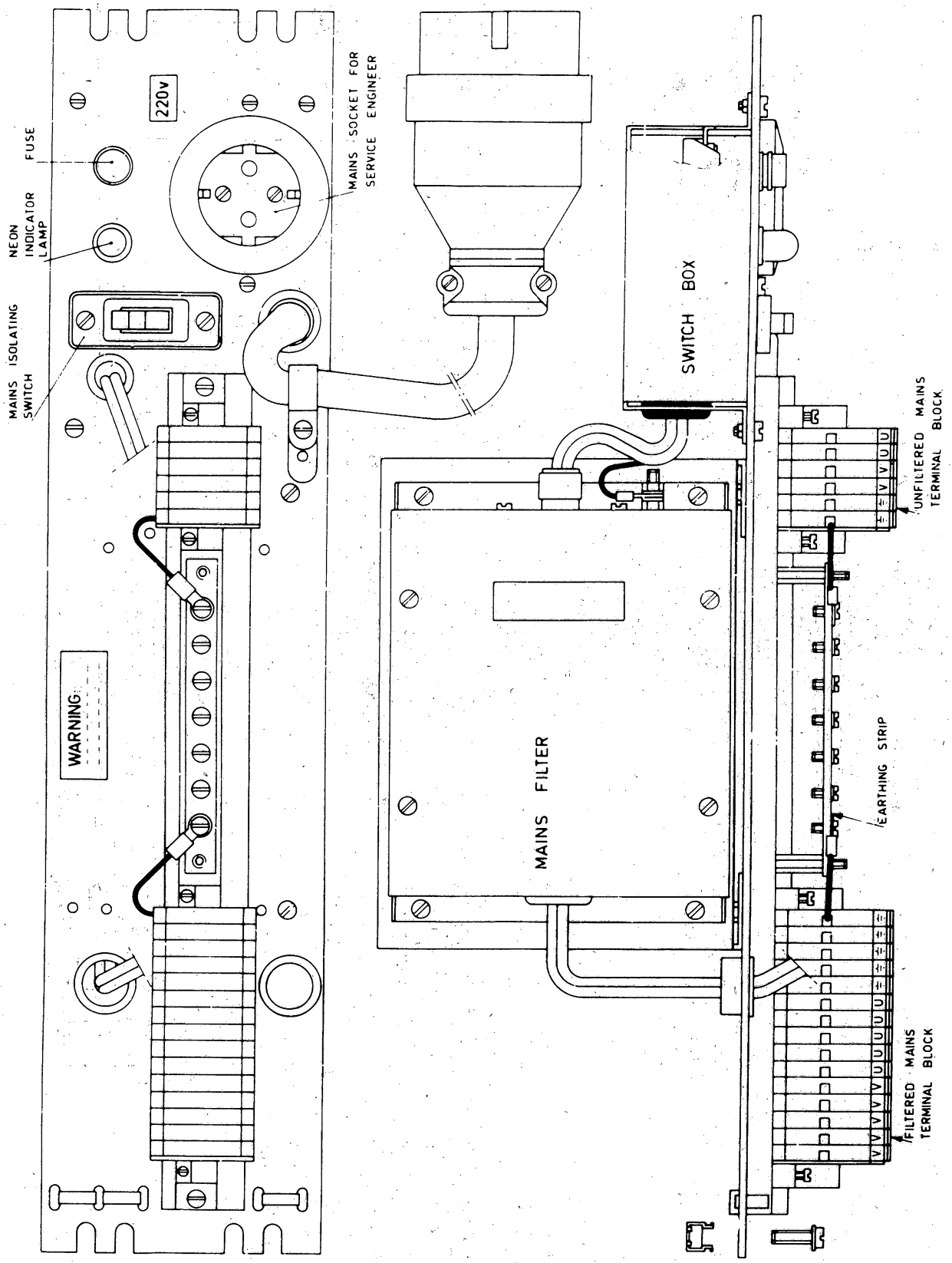


Figure 2.5 25 AMPERE DISTRIBUTION PANEL

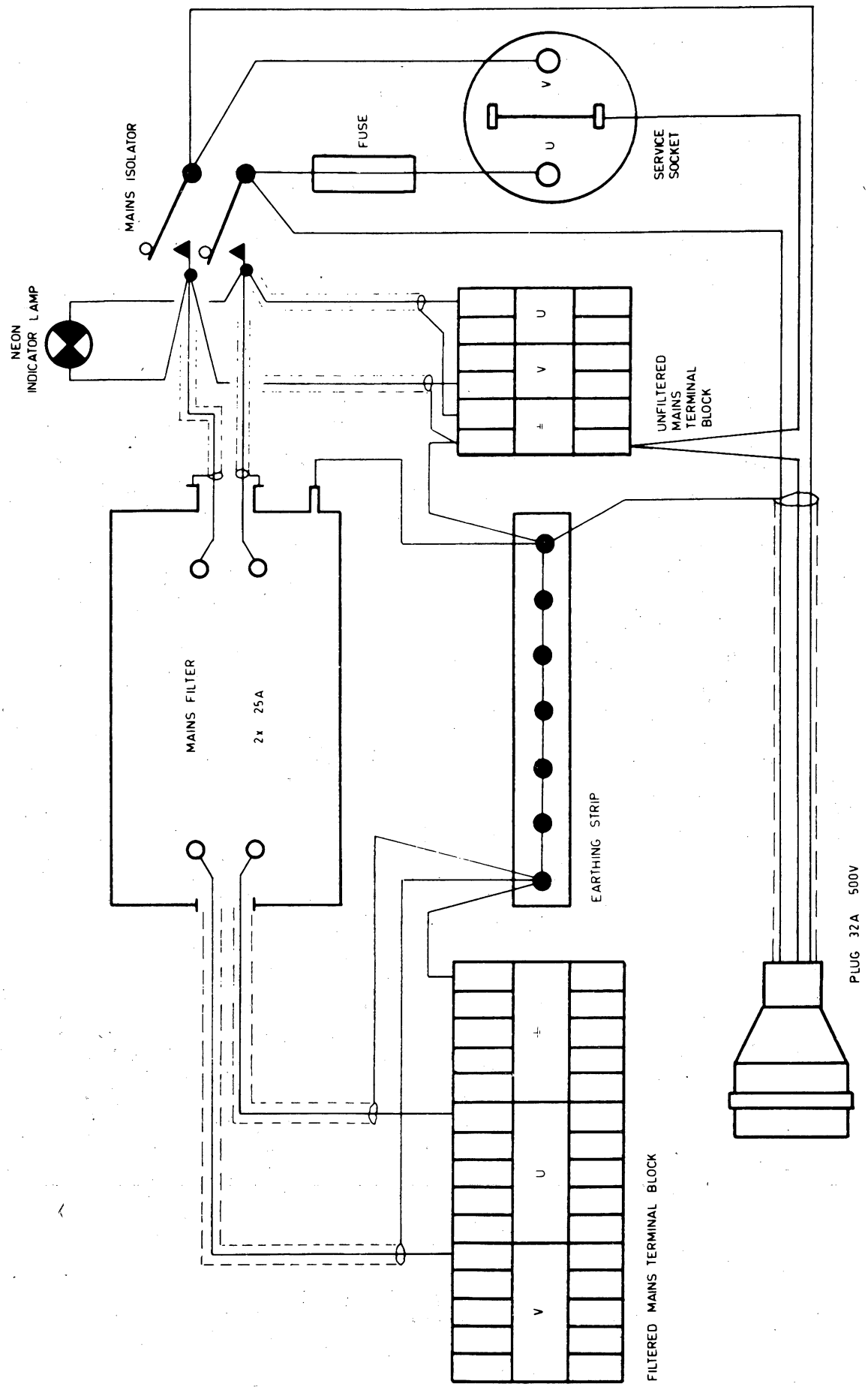


Figure 2.6 25 AMPERE DISTRIBUTION PANEL, CIRCUIT

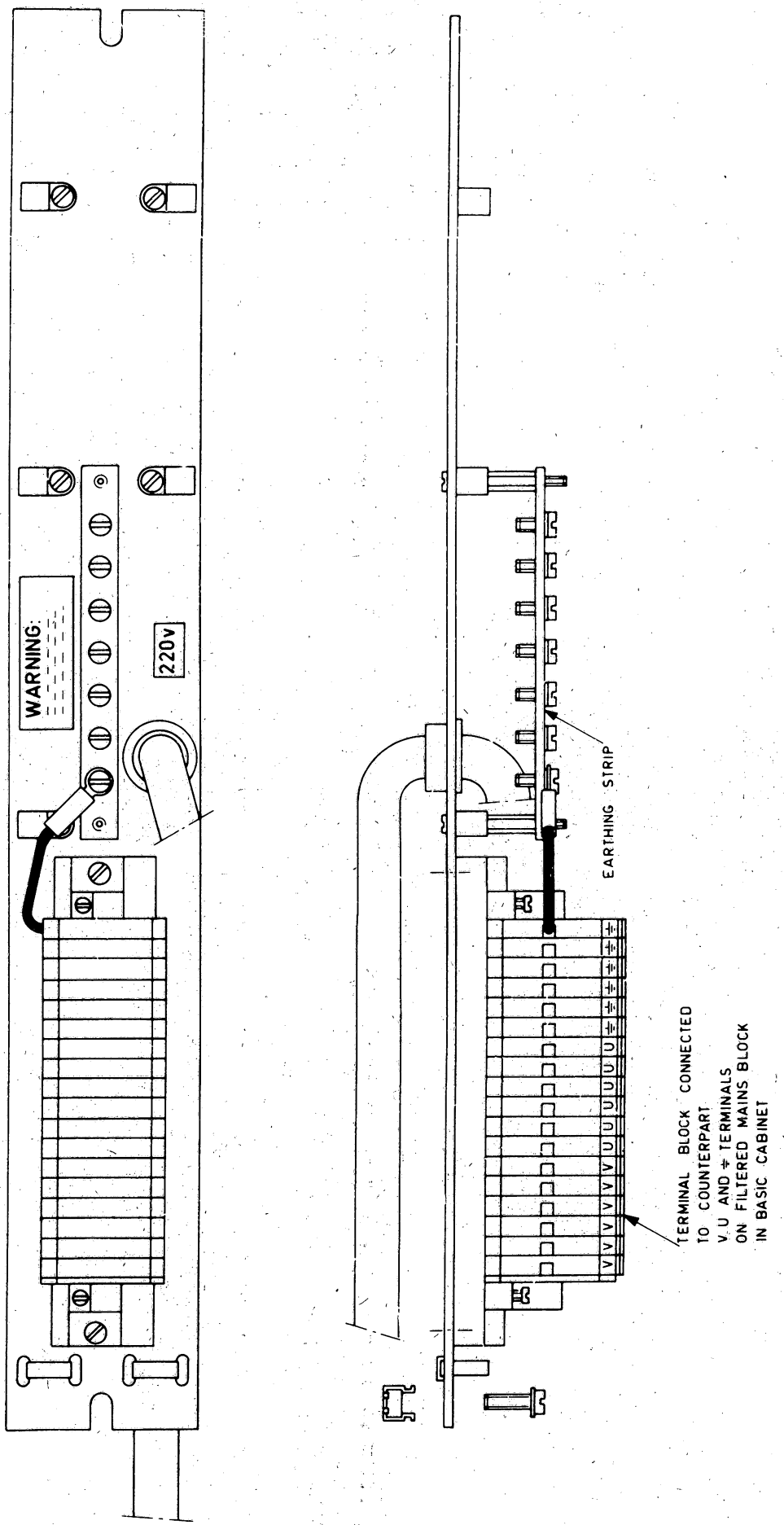


Figure 2.7 EXTENSION CABINET DISTRIBUTION PANEL

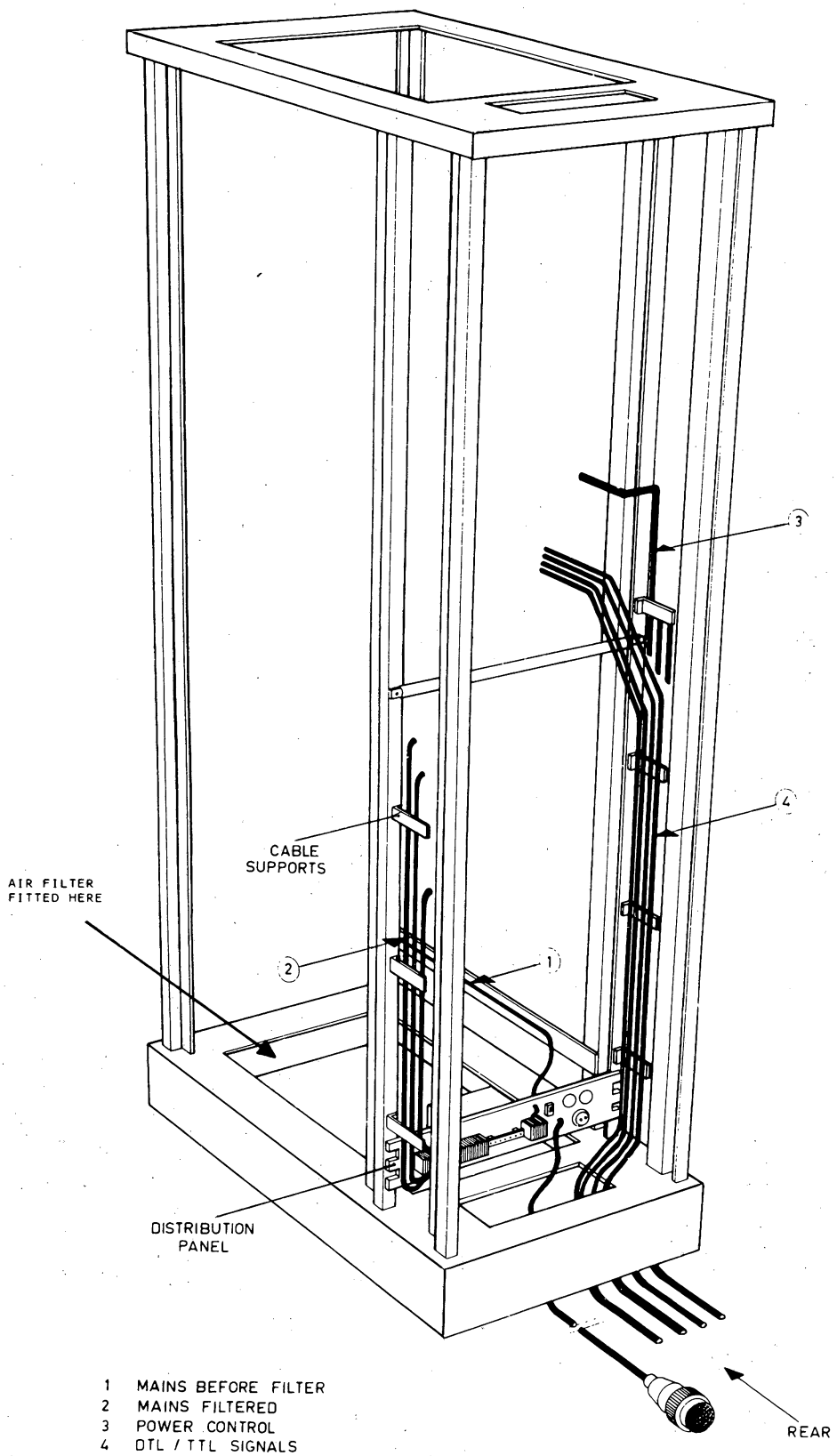


Figure 2.8 EXAMPLE OF CABINET WIRING

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3.1 6U6/6U12 RACKS

3.1.1 PERFORMANCE DATA POWER SUPPLY

- REGULATED D.C. SUPPLIES (LOGIC AND MEMORY)

voltage	load variation static	load variation dynamic	mains variation	current	ripple and noise	ambient temp.range
+5V ±0.25V	20% to 100%	±10%	±10%	up to 12A	1% (0Hz to 30MHz)	0° to 50°C
+10V ±1V	,,	,,	,,	up to 0.6A	,,	,,
+12V ±0.6V	,,	,,	,,	up to 2A	,,	,,
-12V ±0.6V	,,	,,	,,	up to 0.5A	,,	,,

- OVERCURRENT PROTECTION

+ 5V: With +12V and -12V supplies loaded, the current limit is typically 15A.
+12V: Adjustable between nominal load current and 4A* (only allowed after repair in a workshop).
-12V: Adjustable between nominal load current and 4A* (only allowed after repair in a workshop).

* typically 3.8A

- OVERVOLTAGE PROTECTION

+5V: Limited to between +5.5V and +7.5V (6.8V nom.).
+12V: Limited to between +13.5V and +18V (15V nom.).
-12V: Limited to between -13.5V and -18V (-15V nom.).

- UNREGULATED D.C. SUPPLIES

VIN2	+20V	±2V
+18V AUX	+18V	±1.8V

MAINS SUPPLY

198V to 264 single-phase with neutral and safety earth or two-phases and safety earth, 48Hz to 63Hz, or
99V to 132V single-phase with neutral and safety earth or two-phases and safety earth, 48Hz to 63Hz.

3.1.2 PERFORMANCE DATA BATTERY OPTION CARD

INPUTS (from basic power supply)

VIN2 +20V ±2V
+18V AUX +18V ±1.8V

- REGULATED D.C. OUTPUTS (MEMORY ONLY)

voltage	current	load variation static	load variation dynamic	mains variation	ripple and noise	ambient temp.range
+5VM	+0.25V 1A max.	20% to 100%	±10%	±10%	less than or equal to 1% OHz to 30MHz	0° to 50°C
-12VM	+0.6V 1A max.	,,	,,	,,	,,	,,

- OVERCURRENT PROTECTION

+5V: Set to 1.5A.
+12V: Set to 1.5A.

- OVERVOLTAGE PROTECTION

+5V: Limited to between 5.5V and 7.5V (6.8V nom.).
+12V: Limited to between 13.5V and 18V (15V nom.).

Note: Battery charging time (fully exhausted to fully charged) is about 48 hours.
Battery voltage is 14.4V nom. at 2Ah.

LOGIC SIGNALS

	signal	low-level	high-level	current
	PWFN	0V to 0.5V	greater than 2.5V	48mA
*1	RSLN	0V to 0.5V	greater than 2.5V	48mA
*2	BAWOFN	0V to 0.5V	greater than 2.5V	48mA
*3	RTCN	0V to 0.5V	greater than 2.5V	48mA

*1 When a mains voltage is not presvent RSLN is at a true logical 0, i.e. earth potential.
*2 When BAWOFN is not used it is strapped to ground.
*3 Waveform period = mains supply period.
low-level interval = 1us $^{+200ns}_{-300ns}$

3.2 PHYSICAL DESCRIPTION 6U6/6U12 RACKS

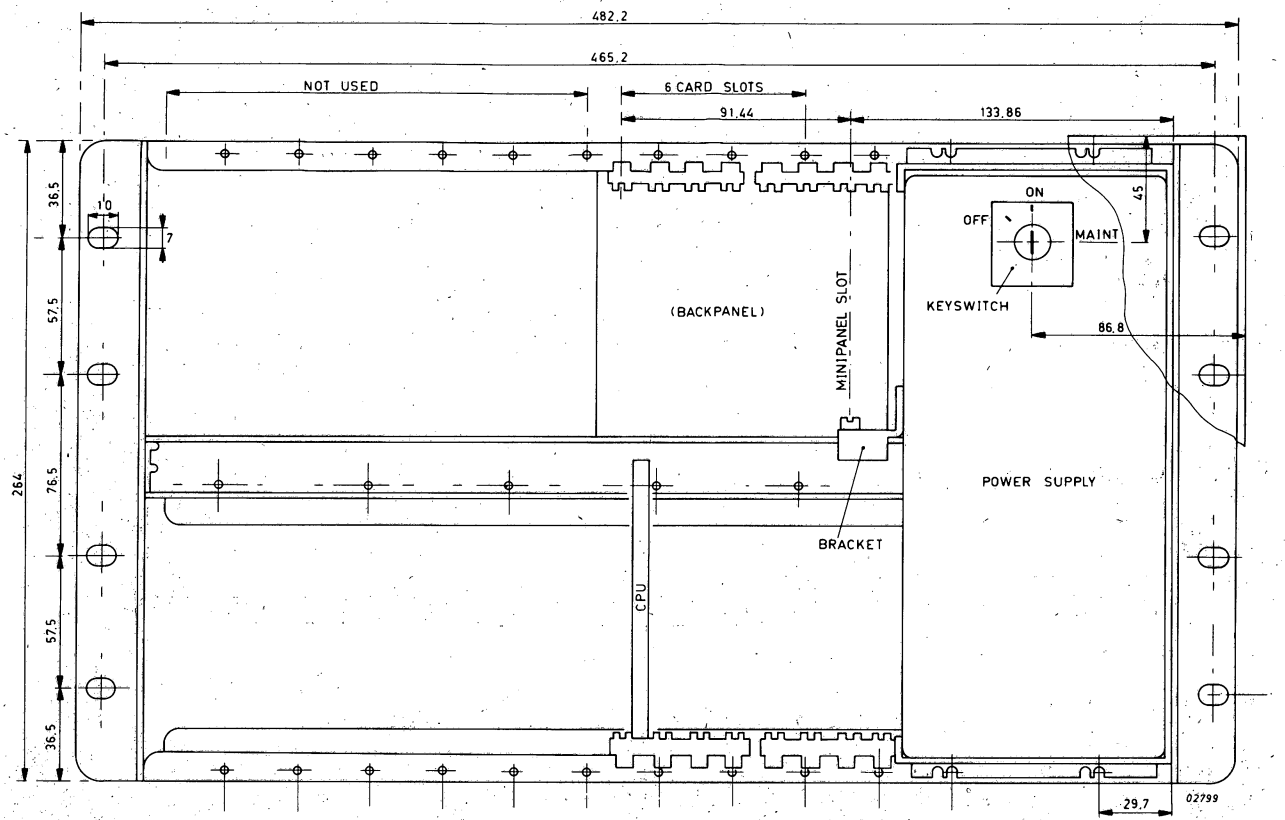


Figure 3.1 FRONT VIEW OF 6U6 RACK

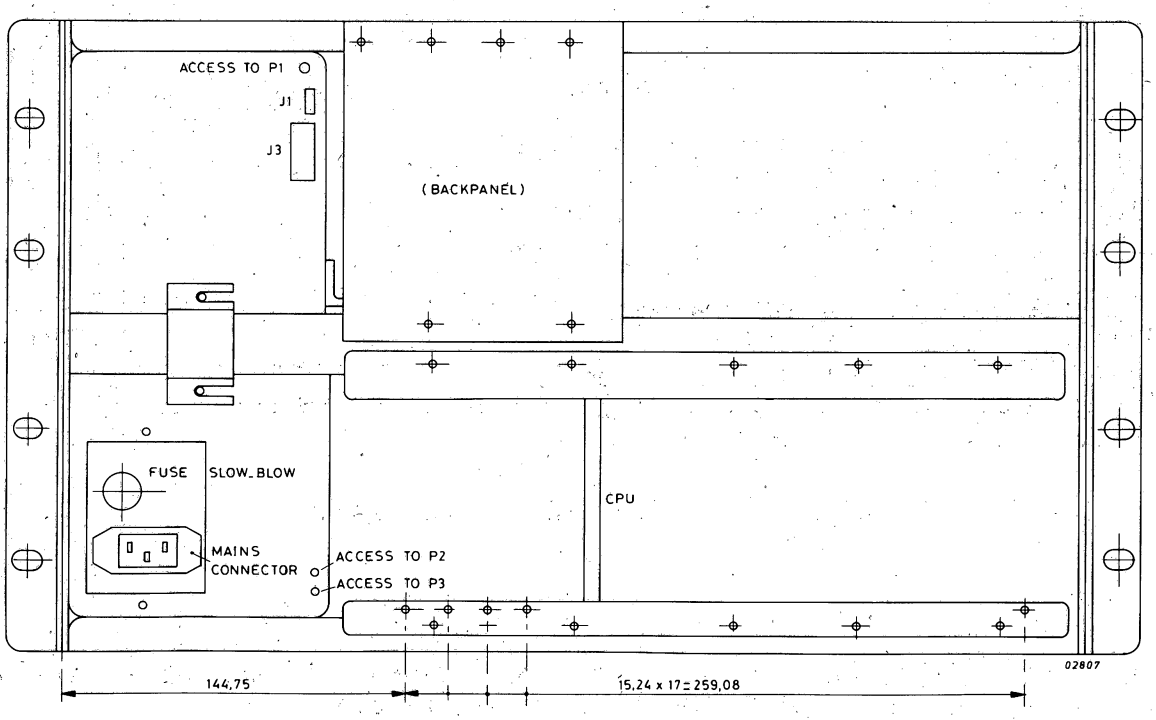


Figure 3.2 REAR VIEW OF 6U6 RACK

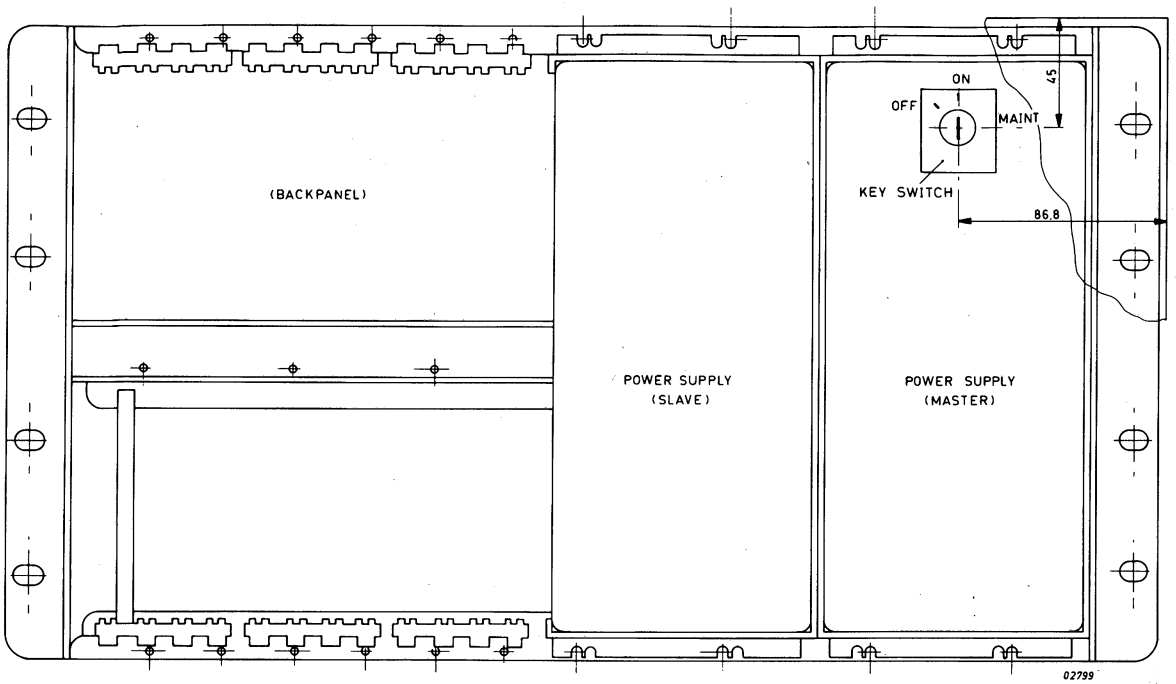


Figure 3.3 FRONT VIEW OF 6U12 RACK

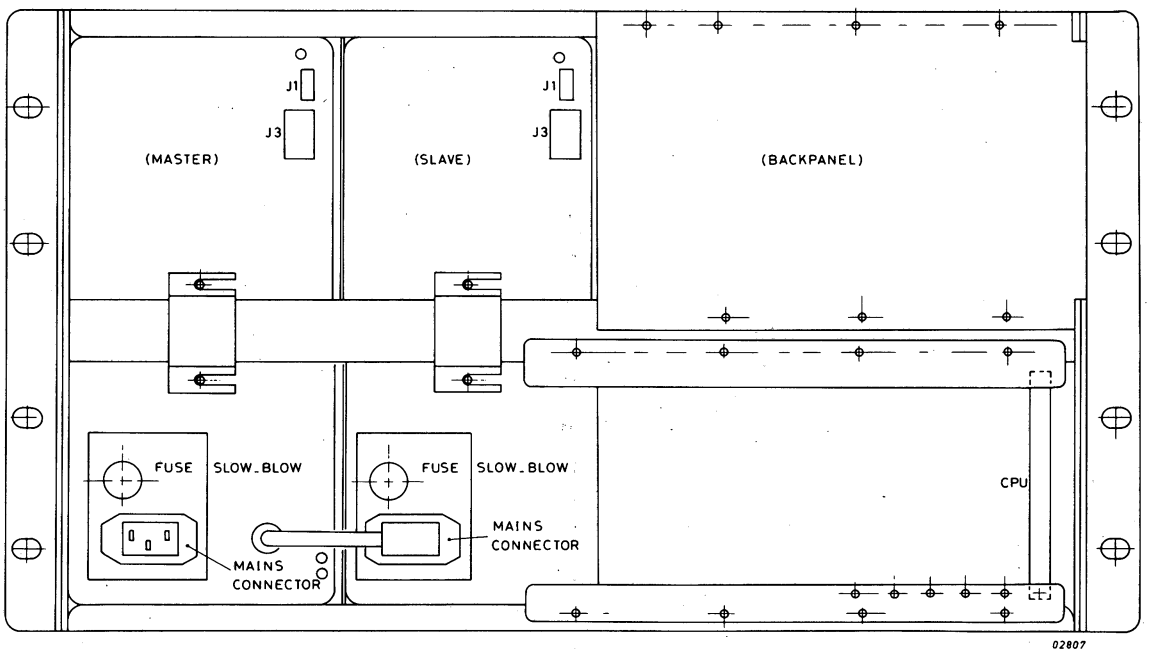


Figure 3.4 REAR VIEW OF 6U12 RACK

Note:

In later versions the slave module of the power supply is mounted on the left (front view) in the rack and the backpanel on the middle.

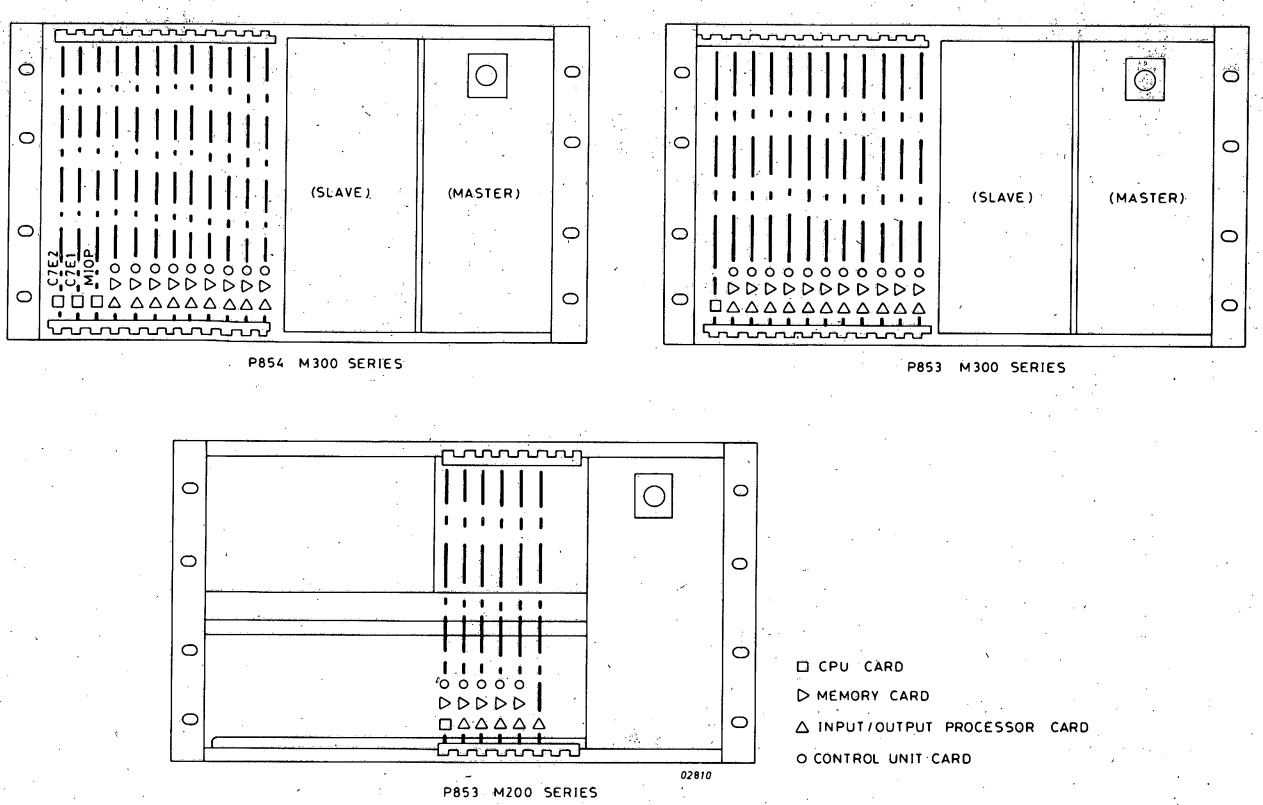


Figure 3.5 6U6/6U12 CARD ARRANGEMENTS

3.3 BACK PANELS 6U6/6U12 RACKS

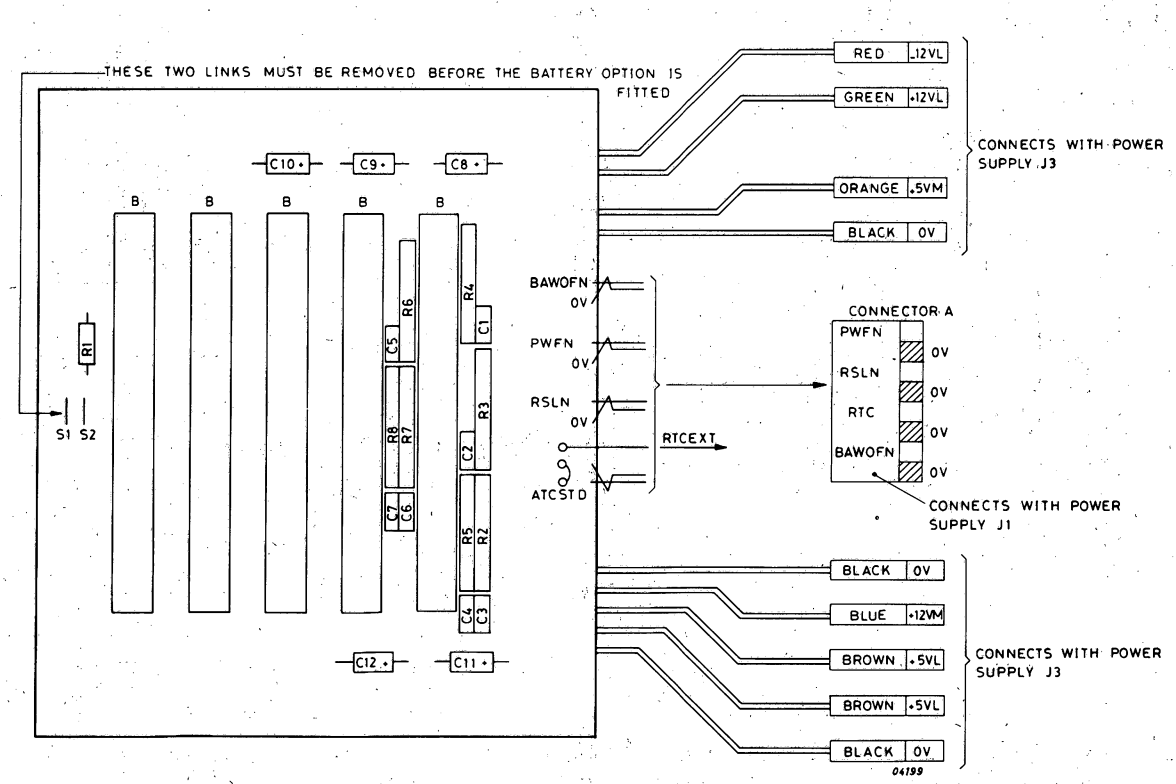


Figure 3.6 6U6 RACK BACK PANEL (UPL BUS) LAYOUTS AND COMPONENTS

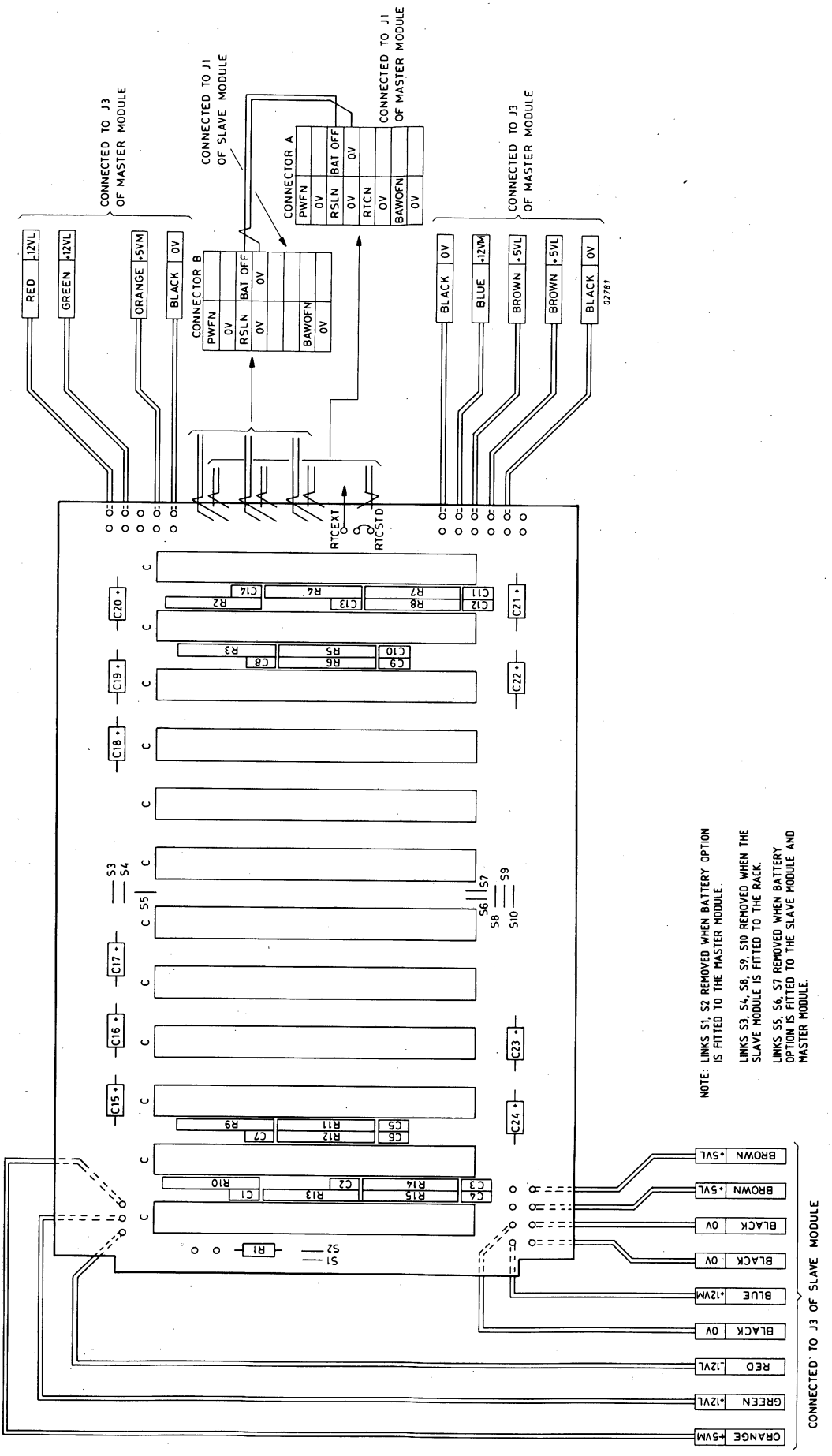


Figure 3.7 6U12 RACK BACK PANEL (UPL BUS) LAYOUT AND COMPONENTS

3.4 POWER SUPPLY 6U6/6U12 RACKS

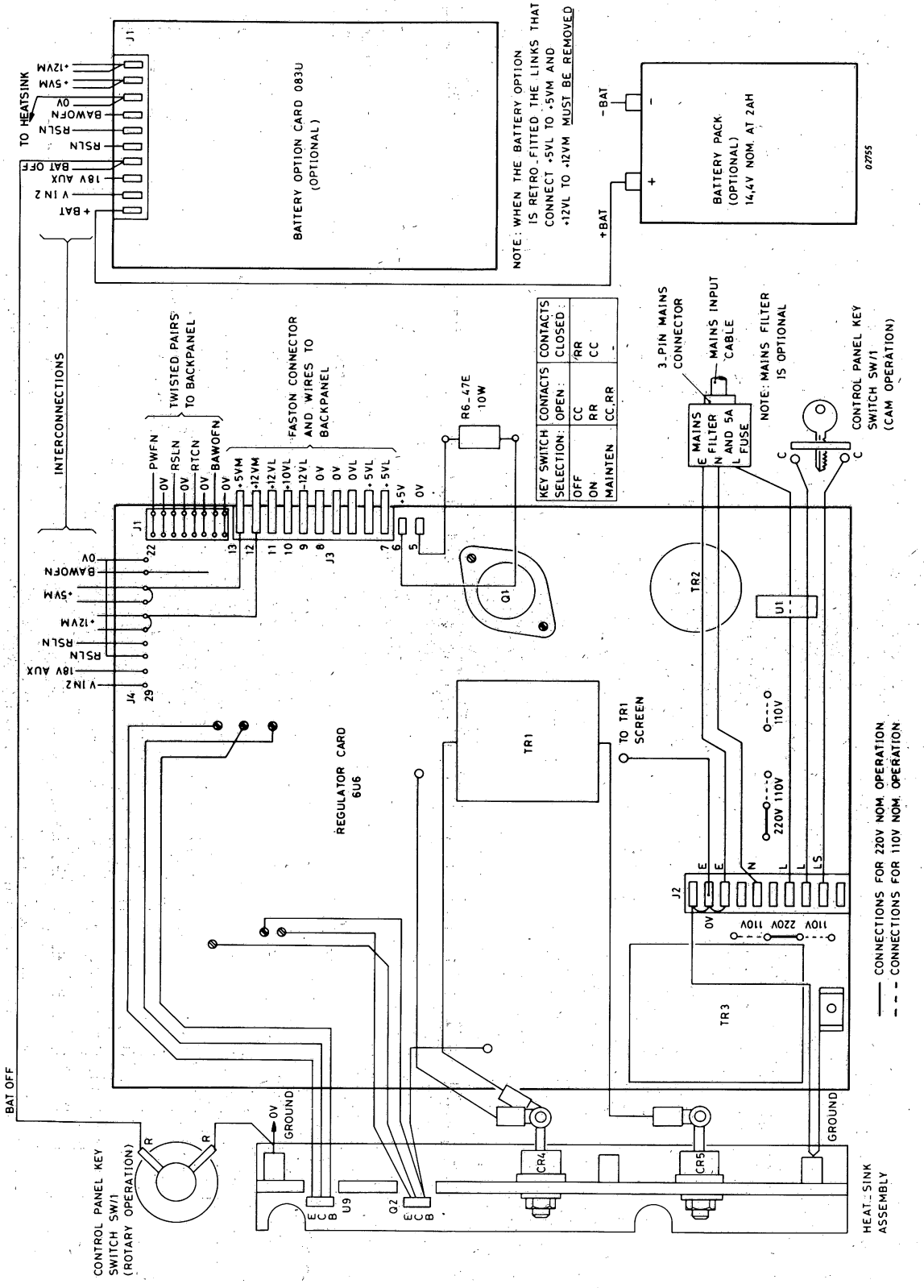


Figure 3.8 6U6 POWER SUPPLY

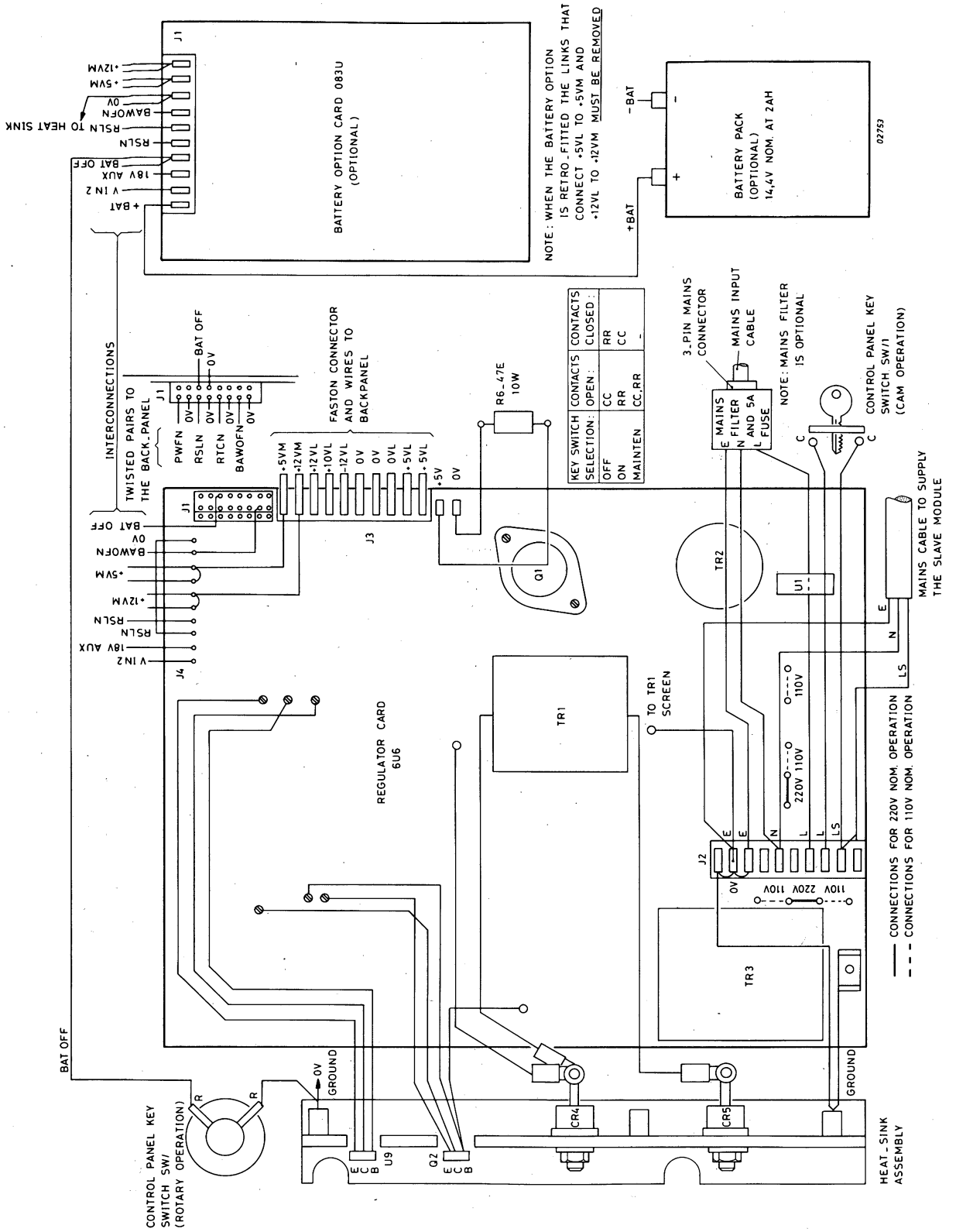


Figure 3.9 6U12 POWER SUPPLY (MASTER)

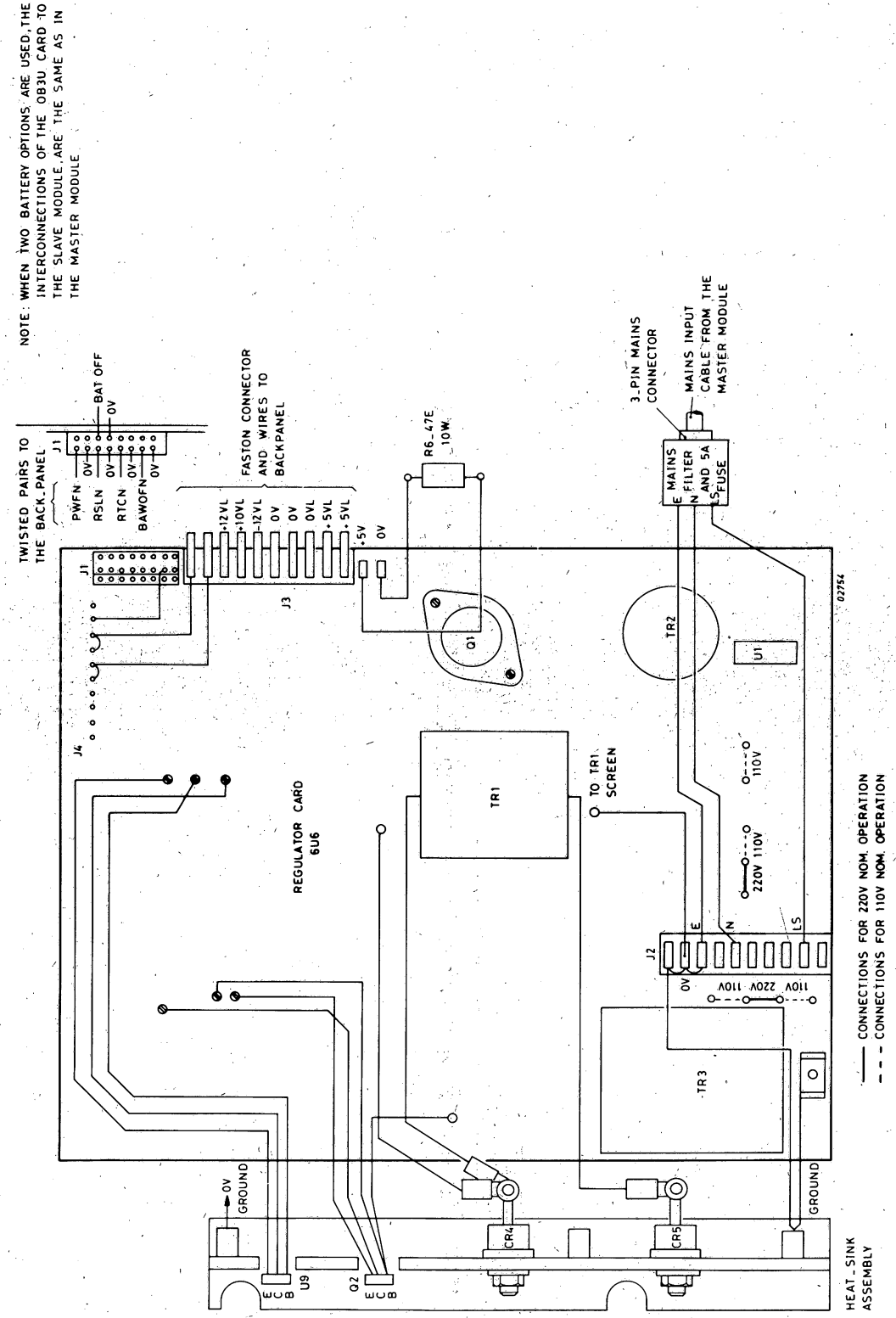
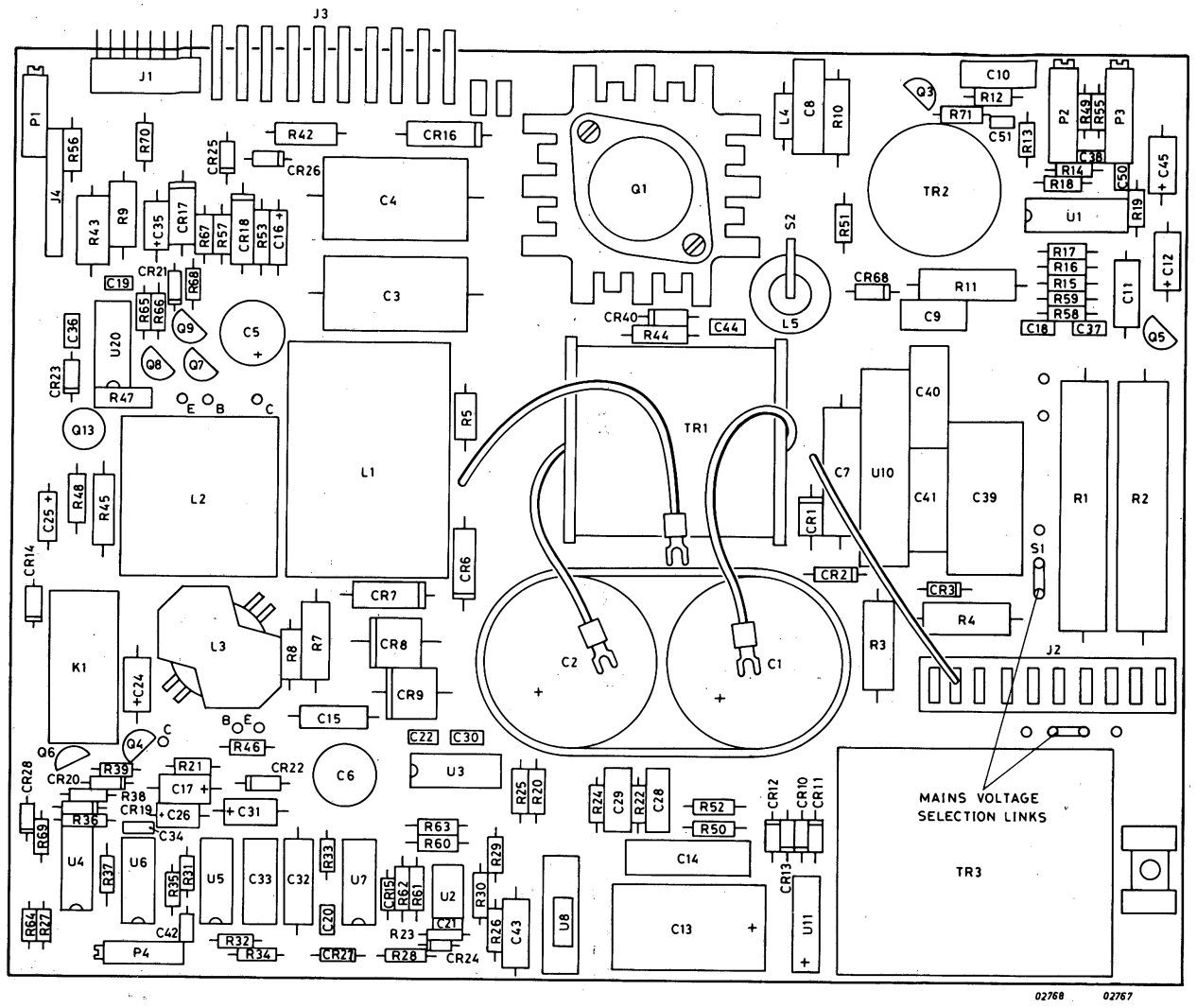


Figure 3.10 6U12 POWER SUPPLY (SLAVE)



NOTE: AS SHOWN, THE CARD IS LINKED FOR 220V MAINS OPERATION

Figure 3.11a CARD LAYOUT REGULATOR CARD

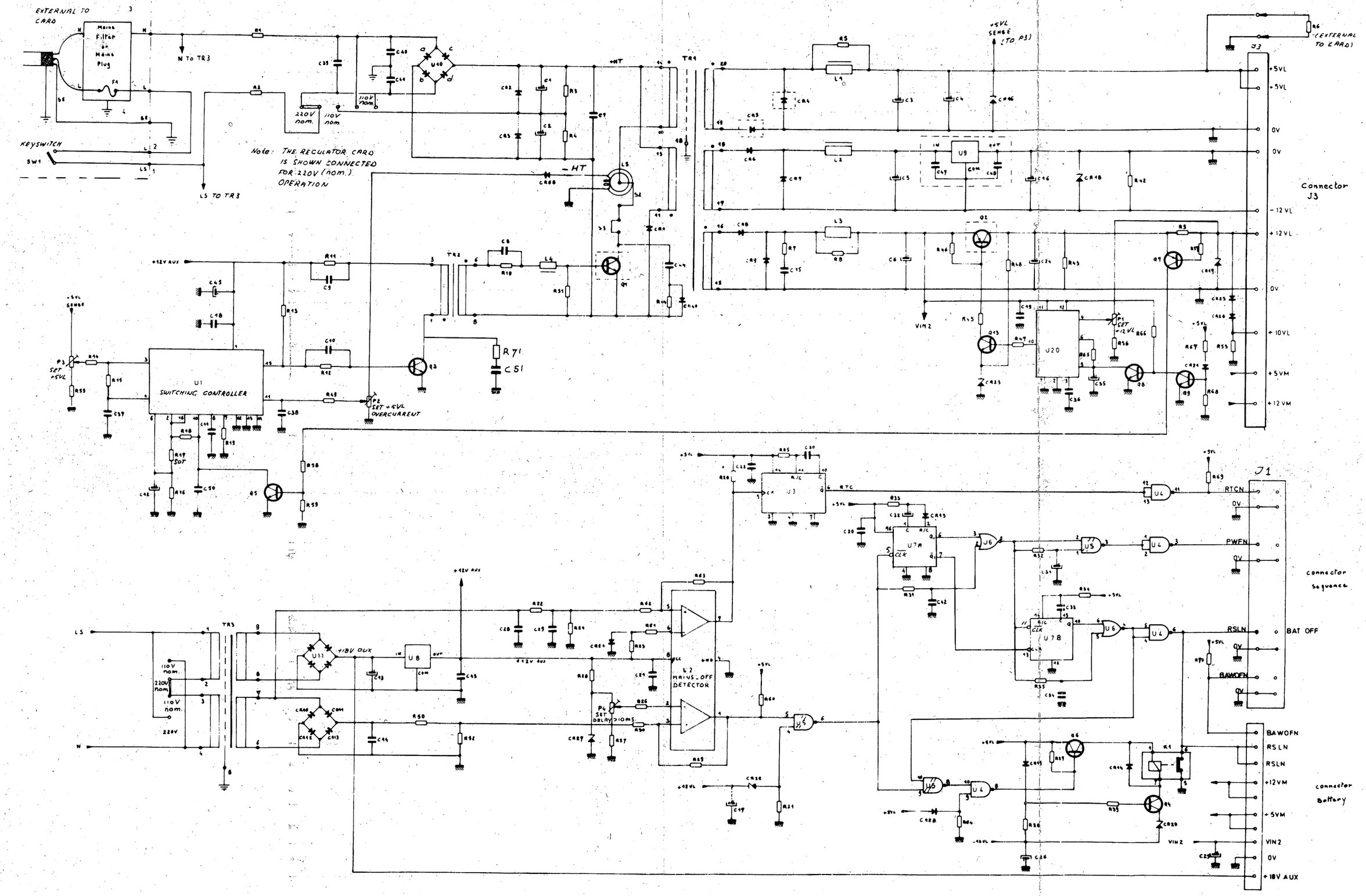
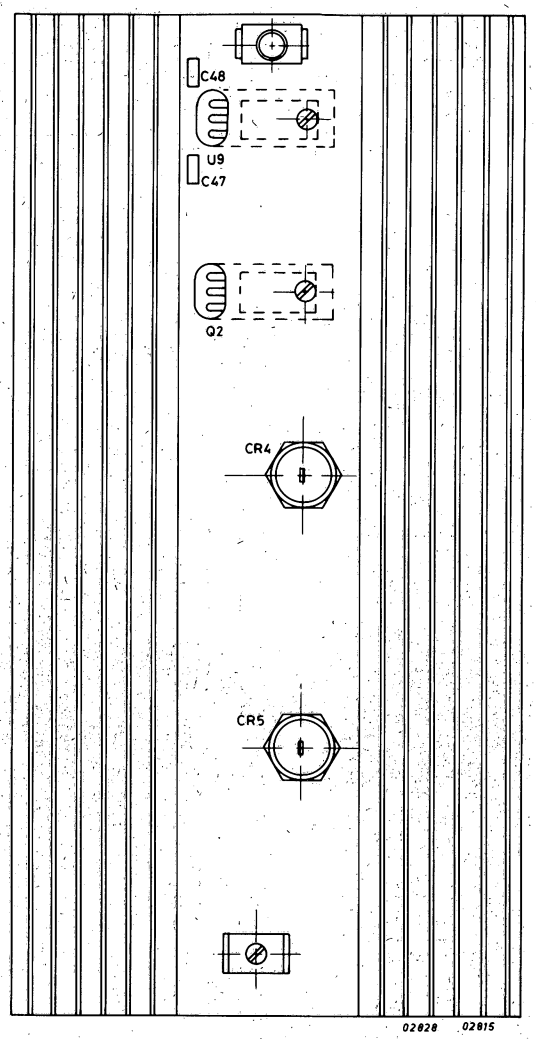


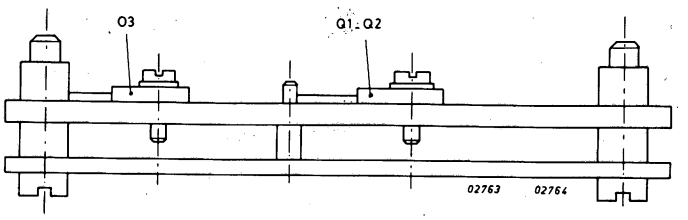
Figure 3.11b REGULATOR CARD



HEAT SINK COMPONENTS

NOTE: C48 CONNECTED BETWEEN U9 EMITTER AND COLLECTOR
C47 CONNECTED BETWEEN U9 COLLECTOR AND BASE

Figure 3.12 HEATSINK



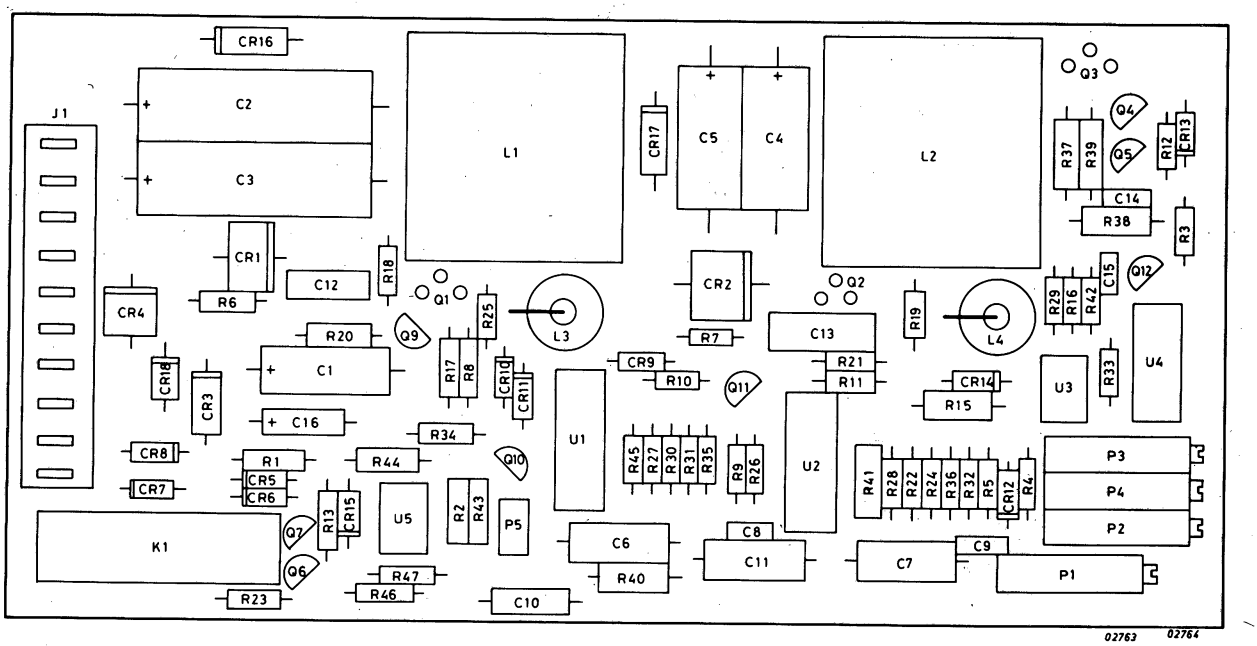


Figure 3.13a CARD LAYOUT BATTERY CARD

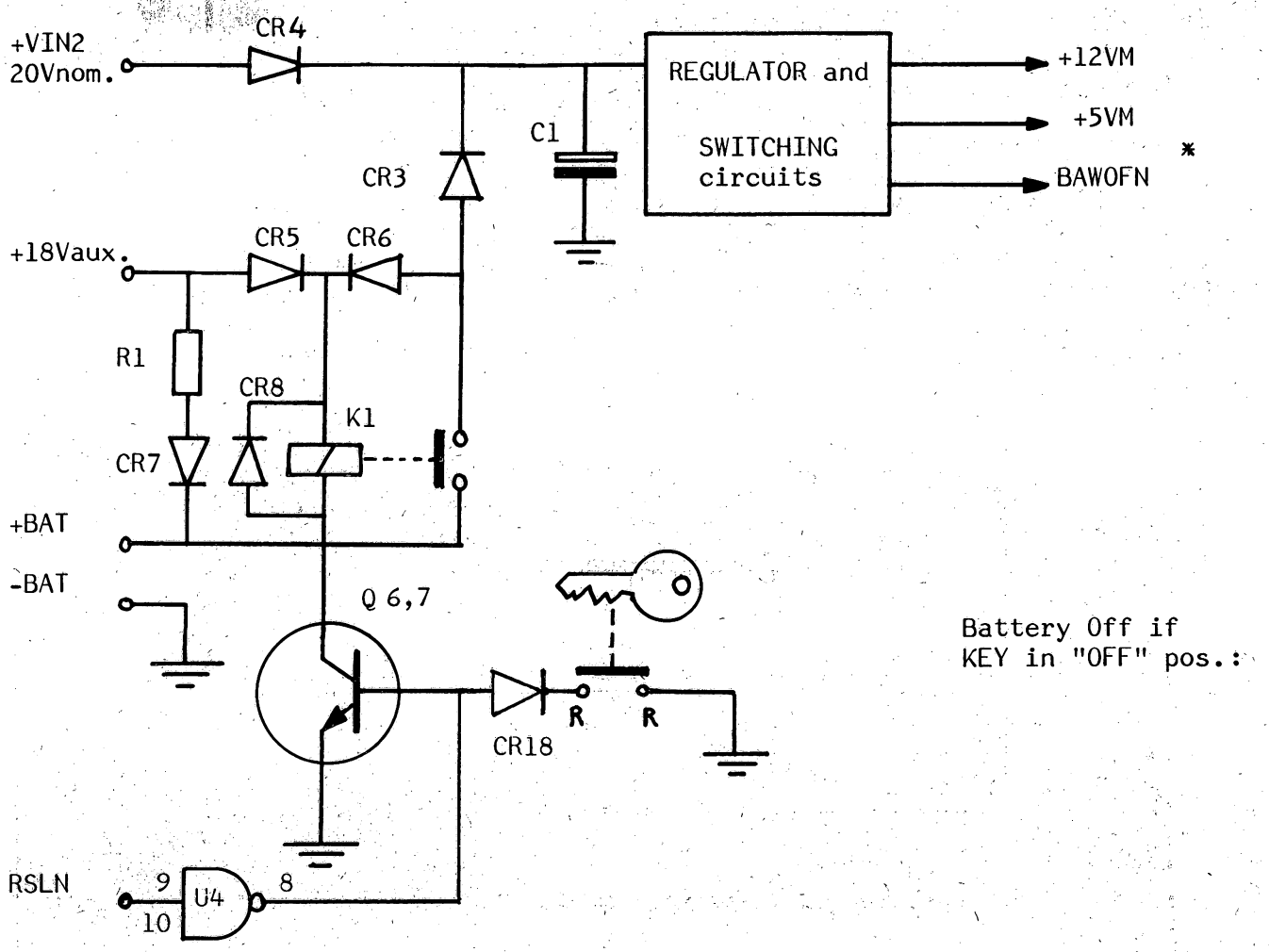


Figure 3.13b BATTERY OPTION CARD

POWER MAINS PRESENT:

+18V aux is used to charge the battery.
Battery voltage not used (Relay contact K1 open).

POWER MAINS NOT PRESENT:

RSLN = Ø, K1 energised.
Battery supplies option card: +5VM & +12VM to supply memory.

POWER OFF:

a) MAINT position: Logic power off, Battery supplies (via OPTION CARD) the memory
b) OFF position: All power switched off.

* NOTE: BAWOFN active when Battery not connected or exhausted, or when memory supplies are not maintained during a power failure.

3.5 INTERCONNECTIONS 6U6/6U12 RACKS

See figures 3.6 and 3.7 for back panels.
Full details of the power supply interconnections are shown on figures 3.8 to 3.9.

3.6 COMPATIBILITY 6U6/6U12

6U6 Racks with six card slots are compatible with P853/GPBS and UPL BUS systems.
6U12 Racks with twelve card slots are compatible with P853 and P854/UPL BUS systems.
Each power supply is compatible with UPL and GPBS bus systems.

Backpanel links S1, S2 are fitted.

Options / Module	Key switch	Mains filter	Mains socket	Battery back-up	
Single Power Supply	yes	no	yes	no	Rack mounted in a cabinet.
Single Power Supply	yes	yes	yes	no	Rack mounted in a mounting box.

Table 3.1 6U6 RACK WITHOUT BATTERY BACK-UP

Backpanel links S1, S2 are not fitted.

Options / Module	Key switch	Mains filter	Mains socket	Battery back-up	
Single Power Supply	yes	no	yes	yes	Rack mounted in a cabinet.
Single Power Supply	yes	yes	yes	yes	Rack mounted in a mounting box.

Table 3.2 6U6 RACK WITH BATTERY BACK-UP

Options / Module	Key switch	Mains filter	Mains socket	Battery back-up	
Master Power Supply	yes	no	yes	no	Rack mounted in a cabinet.
Slave Power Supply	no	no	yes	no	
Master Power Supply	yes	yes	no	no	Rack mounted in a mounting box.
Slave Power Supply	no	no	yes	no	

Back panel links fitted: S1, S2, S5, S6, S7.
Back panel links not fitted: S3, S4, S8, S9, S10.

Table 3.3 6U12 RACK WITHOUT BATTERY BACK-UP

Options / Module	Key switch	Mains filter	Mains socket	Battery back-up	
Master Power Supply	yes	no	yes	yes	Rack mounted in a cabinet.
Slave Power Supply	no	no	yes	no	
Master Power Supply	yes	yes	no	yes	Rack mounted in a mounting box.
Slave Power Supply	no	no	yes	no	

Back panel links fitted: S5, S6, S7.
Back panel links not fitted: S1, S2, S3, S4, S8, S9, S10.

Table 3.4 6U12 RACK WITH BATTERY BACK-UP

Options / Module	Key switch	Mains filter	Mains socket	Battery back-up	
Master Power Supply	yes	no	yes	yes	Rack mounted in a cabinet.
Slave Power Supply	no	no	yes	no	
Master Power Supply	yes	yes	no	yes	Rack mounted in a mounting box.
Slave Power Supply	no	no	yes	no	

Back panel links fitted:
Back panel links not fitted: S1, S2, S3, S4, S5, S6, S7, S8, S9

Table 3.5 6U12 RACK WITH TWO BATTERY BACK-UPS

3.7 RU22 RACK

3.7.1 MECHANICAL DATA

The weights and maximum dimensions of the basic mechanical units of the RU22 are as shown below:

	RU22 LOGIC RACK	RU22 POWER SUPPLY RACK	VENTILATION UNITS
Height	266 mm (6U)	266 mm (6U)	133 mm (3U)
Width	240 mm (19")	240 mm (19")	240 mm (19")
Length	260 mm (with cable shelf)	365 mm	300 mm
Weight	5 kilograms	9.3 kilograms	1.5 kilograms

Table 3.6 WEIGHT AND MAXIMUM DIMENSIONS RU22

3.7.2 VENTILATION

The logic rack and power supply rack ventilator units are electrically functionally identical but their mechanical construction is different.
The Ventilation Unit characteristics are shown below:
SUPPLY (110V - 120V, ± 10%, 50-60Hz.
(220V - 240V, ± 10%, 50-60Hz.

VENTILATION CAPACITY

Extraction for 23 card slots : 450W.
Inter-card air flow speed : 1m/sec.
Air flow temperature increase: 5°C.
(at card rack level)

3.7.3 PERFORMANCE DATA POWER SUPPLY

POWER SUPPLY INPUT REQUIREMENTS

Mains Voltage - lower range: 99V to 132V
- upper range: 198V to 264V
Single Phase with neutral and safety earth or two phases with safety earth.
Mains Frequency : 48 to 63Hz.
Mains Current - Switch on current: 20A for 5ms at 110V
20A for 3ms at 220V
- Operating current, measured at nominal load:
6.8 A rms at 110V
3.78A rms at 220V
The mains input supply is protected by a UL/CSA approved slow operating fuse.

220V: type D8TD4
110V: type D8TD8

DC SUPPLY STABILITY

+5VL, +3%	for: static load variations dynamic load variations temperature variations mains variations	20 to 100% +10% 0 to 50°C +10%
-5VL,+5% +12VL -12VL +12VM	for: static load variations dynamic load variations temperature variations mains variations	10 to 100% +10% 0 to 50°C +10%
+5VM, +3%	for: static load variations dynamic load variations temperature variations mains variations	10 to 100% +10% 0 to 50°C +10%

Table 3.7 DC SUPPLY STABILITY RU22

The supplies are protected for over voltage and over current. Short circuits on the supplies will not damage them.

POWER SUPPLY RATING

The Power Supply Rack can supply different current values depending on the configuration, the examples of maximum permitted current are given below and examples of current consumption for the logic are given in Tables 3.10 and 3.11.

LOGIC VOLTAGES (WITH VENTILATION UNIT OPERATING)

VOLTAGES	1 PSUB1 MODULE	2 PSUB1 MODULES
+5VL	40.0 A	60.0 A
+12VL	1.5 A	3.0 A
-12VL plus -5VL	1.0 A	2.0 A

Note: The -5VL is derived from the -12VL and the current is limited to 0.8 A.

Table 3.8 LOGIC VOLTAGES RU22

MEMORY VOLTAGES (WITH VENTILATION UNIT OPERATING)

VOLTAGES	1 PSUM MODULE	2 PSUM MODULES
+5VM +12VM	2.5 A 1.4 A	5.0 A 2.8 A

Table 3.9a MEMORY VOLTAGES RU22

IN STAND-BY MODE (VENTILATION BY NATURAL CONVECTION ONLY)

VOLTAGES	1 PSUM MODULE	2 PSUM MODULES
+5VM +12VM	2.0 A 1.0 A	4.0 A 2.0 A

Table 3.9b MEMORY VOLTAGES STANDBY RU22

SLOT	CARD	+5VL	-5VL	+12VL	-12VL	+5VM	+12VM
1 2	C7E1 C7E2	7.5		0.06	0.035		
3	MIOP	3.0					
4 5	DFPC(1) DFPC(2)	8.2	0.7				
6	F1MZ	2.3					
7	ASCU4Z	1.8		0.05	0.03		
8	ASCU4Z	1.8		0.05	0.03		
9	ASCU4Z	1.8		0.05	0.03		
10	ASCU4Z	1.8		0.05	0.03		
11	HLCUZ	2.3		0.03	0.03		
12	CRLPZ	1.0					
13	WMB1	5.5				2.24	2.2
14	WMB1						
15	WMB1						
17	WMC1						
18	WMB1						
19	WMB1						
20	WMB1						
21	WMB1						
22	TUGP	1.5					
Control Panel	FRCP	0.8		0.17	0.025		
TOTAL		39.4	0.7	0.46	0.091	2.24	2.2
AVAILABLE		40.0	0.8	1.5	1.0	5/4	2.8/2

Note: Current is given in maximum values.
-5VL is derived from the -12VL supply.

Table 3.10 EXAMPLE OF SYSTEM CONFIGURATION USING A POWER SUPPLY WITH 1 PSU-B MODULE AND 2 PSU-M MODULES

SLOT	CARD	+5VL	-5VL	+12VL	-12VL	+5VM	+12VM
1 2	C7E1 C7E2	7.5		0.06	0.035		
3	MIOP	3.0					
4 5	CDDZ MDDZ	2.9 2.4					
6 7	FPPZ FPPZ	6.0					
8	F1MZ	2.3					
9	HLCUZ	2.3		0.03	0.03		
10	HLCUZ	2.3		0.03	0.03		
11 12	VCCU4 VCCU4	8.0					
13 14	VCCU4 VCCU4	8.0					
15	GMB1	2.12				2.0	0.94 or 0.52
16	GMB1						
17	GMB1						
18	GMB1						
19	TUGP	1.5					
20							
21							
22							
Control Panel	FRCP	0.9		0.17	0.025		
TOTAL		49.22		0.29	0.12	2.0	0.94 or 0.52
AVAILABLE		60.0	0.8	3.0	2.0	2.5/2	1.4/1

Note: Current is given in maximum values.

Table 3.11 EXAMPLE OF SYSTEM CONFIGURATION USING A POWER SUPPLY WITH 2 PSU-B MODULES AND 1 PSU-M MODULE

BATTERY BACK-UP TIMES (FOR A FULLY CHARGED BATTERY)

MEMORY TYPE	CAPACITY	RETENTION TIME
Master Slave	256KB	1H50
	512KB	1H10
	1MB	0H30
GMB1	64KB	6H00
	128KB	3H00
	256KB	1H30

Table 3.12 BATTERY BACKUP TIMES RU22

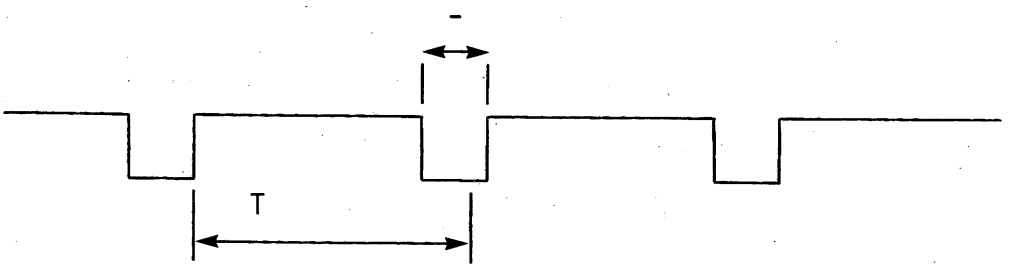
The charging circuit recharges a fully discharged battery in 48 hours at 25°C.

LOGIC SIGNALS

REAL TIME CLOCK - RTCN - ACTIVE LOW

Low level - smaller than or equal to 0.4V, sink current 48mA
High level - open collector output

This signal is a train of 1uS pulses as shown in the diagram below.



- = 1us +20% - 30%
T = mains period (20mS for 50Hz., 16.66ms for 60Hz.)

POWER FAILURE - PWFN - ACTIVE LOW

Low level - smaller than or equal to 0.4V, sink current 48mA
High level - open collector output

See figure 2.2 for timing of this signal and RSLN.

RESET LOGIC - RSLN - ACTIVE LOW

Low level - true ground through a relay contact, sink current 100mA
High level - open collector output

3.8 PHYSICAL DESCRIPTION RU22

The RU22 contains two principal mechanical units which are the 2 racks for the power supply and for the logic cards (23 slots).
The Front Panel which encloses the logic rack of older systems is 10U high.
The keyswitch protudes through a hole in the top right hand corner and the FRCP is mounted at the top left. In newer systems there are three front panels. A 6U panel covers the logic rack and above it is a 4U panel for the keyswitch and FRCP. A 1U covers the cable shelve.

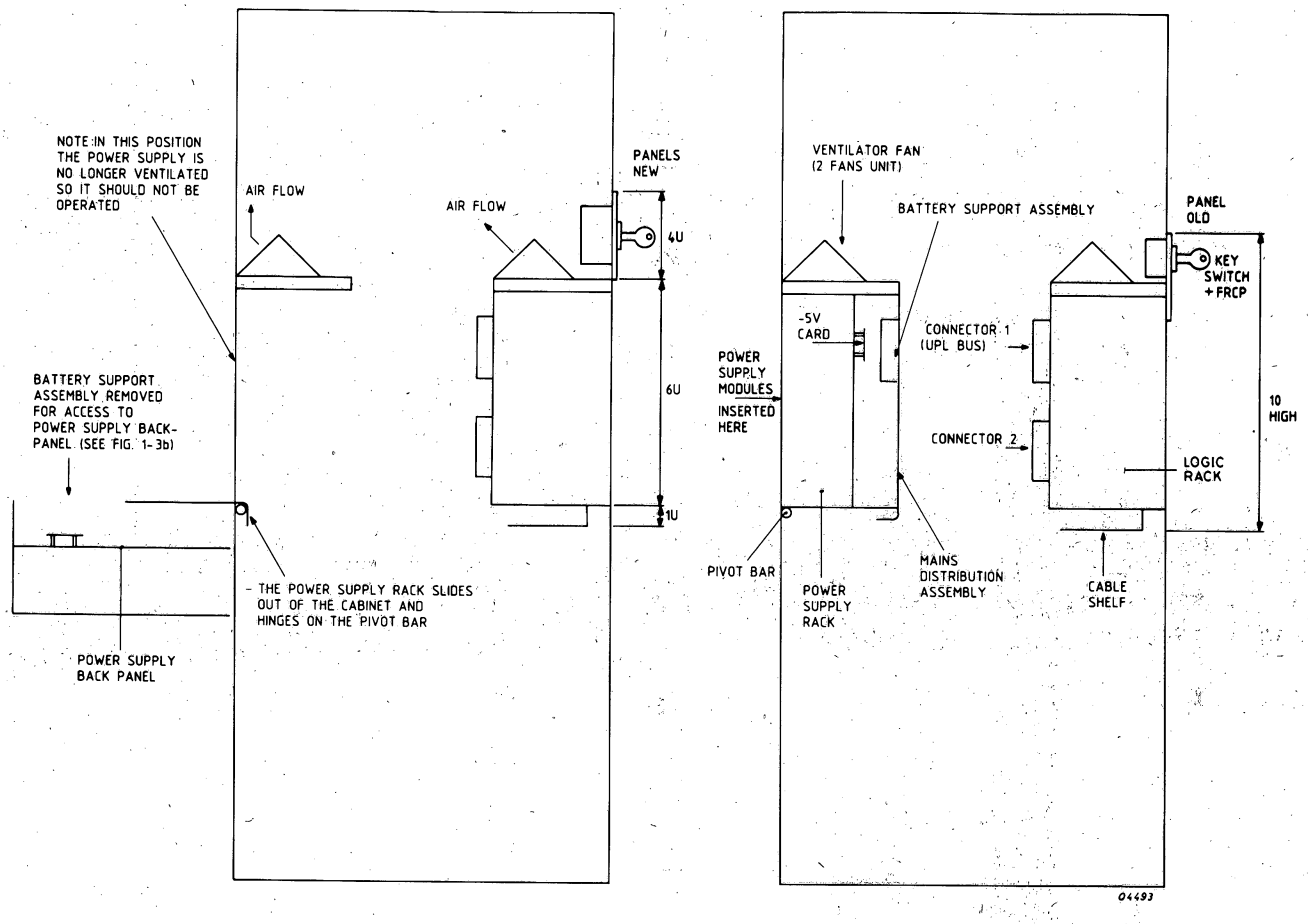


Figure 3.14a RU22 PHYSICAL CONFIGURATION

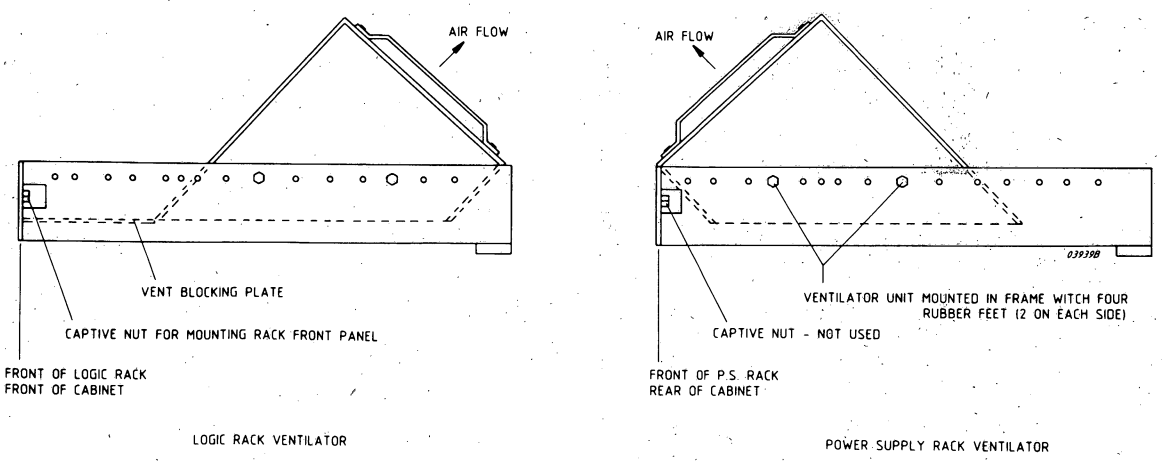


Figure 3.14b VENTILATION ASSEMBLIES

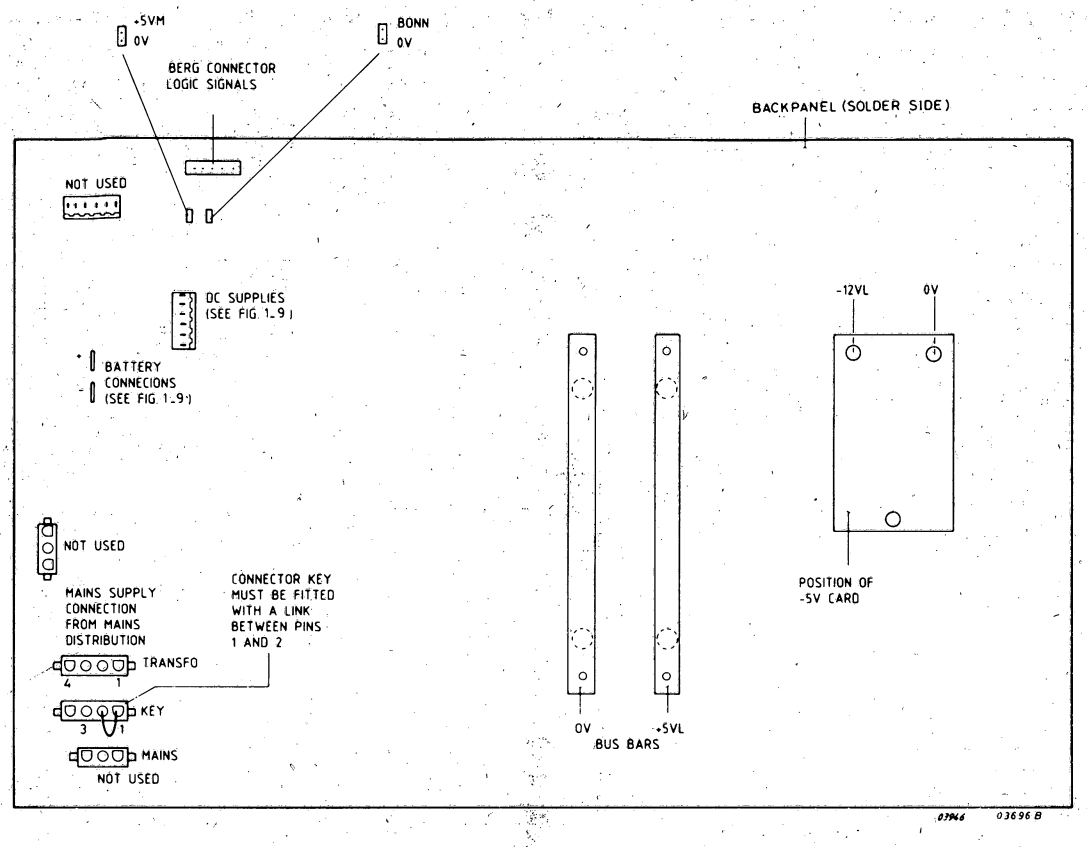
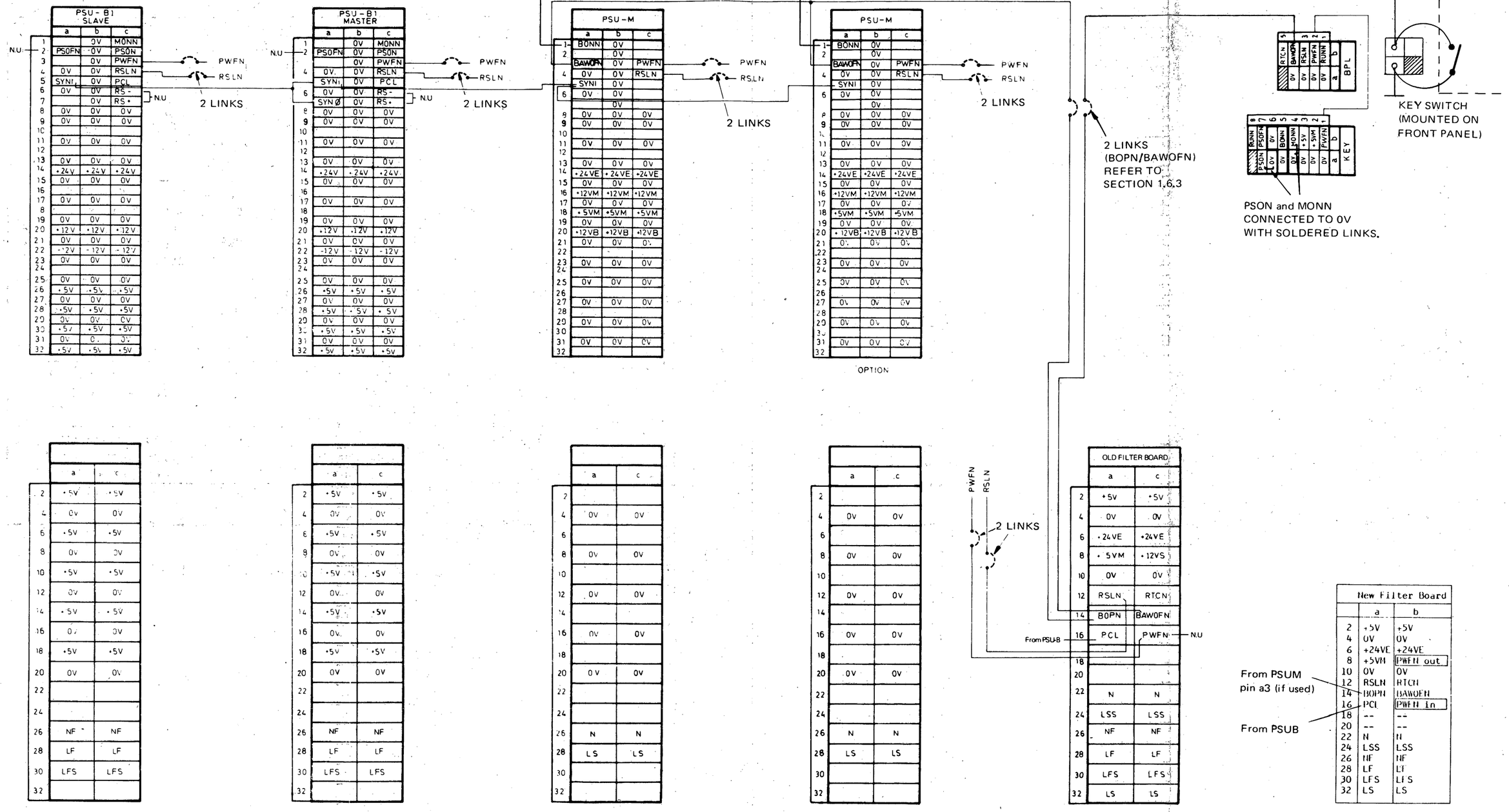


Figure 3.15a POWER SUPPLY BACK PANEL - RU22 - SOLDER SIDE



Note 1: For old PSU-M modules, pin a3 is signal BOPN, connected to pin a14 of filter board. For new PSU-M modules, pin a3 is selected with a U-link on the module:
either . BOPN - connected to pin a14 of filter board.
or . BAWOFN - connected directly to the CPU via connector BPL (Berg).

Note 2: Old filter board must not be used with new Power Supply Back Panel (see table 3.13).

Note 3: PSU-B1 Signal Definitions
. MONN = Master On, Active low
. PSON = Power Supply On
. PWFN = Power Fail, Active low
. RSLN = Reset Logic, Active low
. PCL = Power Control Line
. RS-/+ = Remote sensing
. PSOFN = Power Supply Off, Active low
. SYNI = Synchronisation In
. SYNV = Synchronisation Out (used only by Master)

Figure 3.15b POWER SUPPLY BACK PANEL - RU22 CONNECTOR SIDE

		POWER SUPPLY RACK BACK PANEL TYPE	
		PBP84 (RU22 systems) 5111 199 6035 index 1 or 2 (old) or PBP84 (P8400 systems) 5111 199 6316 index 1 (old)	PBP84 (RU22 systems) 5111 199 6035 index 3 or above (new) or PBP84 (P8400 systems) 5111 199 6316 index 2 or above (new)
FILTER BOARD TYPE	5111 199 6474 index 1 or 2 (old)	This is permitted but a cassette rack must not be used with the system	NOT ALLOWED - The +12VS output from the filter board at pin C8 would destroy the PWFN buffers of other cards in the system
	5111 199 6474 index 3 or above (new)	This is permitted but a cassette rack must not be used with the system	Correct operation with or without a cassette rack.
PSU-M MODULE TYPE	5112 291 42390 (old)	Can be used with either back panel type but the BOPN/BAWOFN U-links must be fitted vertically (see section 3.9.3)	
	5112 291 64860 (new)	Can be used with either back panel type but the BOPN/BAWOFN U-links must be fitted horizontally (see section 3.9.3). The U-link on the PSU-M module must be in the position as indicated on Figure 3.17b.	

Table 3.13 POWER SUPPLY CONFIGURATIONS RU22

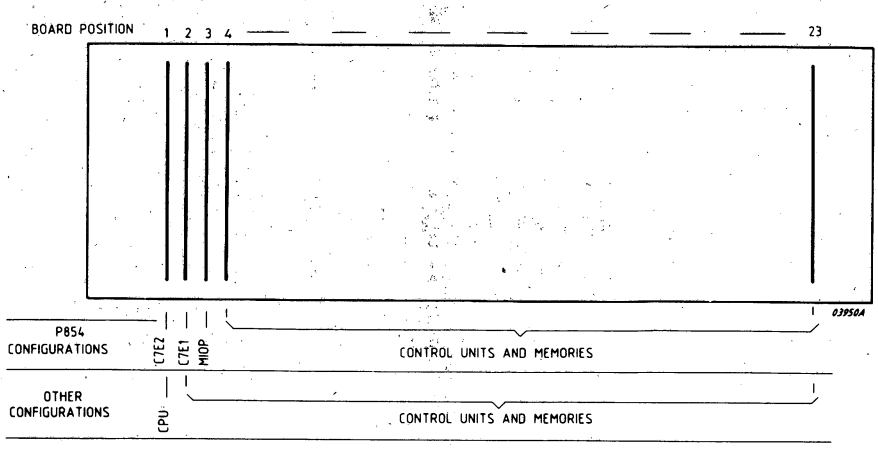
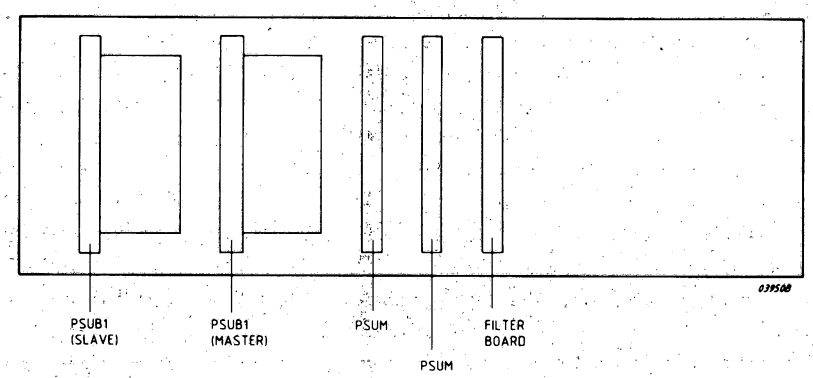


Figure 3.16a LOGIC RACK CARD POSITIONS - RU22



NOTE MINIMUM CONFIGURATIONS IS PSUB1 (MASTER)
FILTER BOARD AND ONE OF THE PSUM MODULES

Figure 3.16b POWER SUPPLY RACK - CARD POSITIONS - RU22

3.9 INSTALLATION DATA RU22

The following information is intended as a guide only for the installation of the RU22.

3.9.1 MAINS INPUT VOLTAGE ADAPTATION

The power supply is adapted to the mains voltage with links on:

- PSU-B module(s) - refer to figure 3.17a
- PSU-M module(s) - refer to figure 3.17b
- Filter Board - two U-links on the card. Figures 3.23 and 3.24 show these U-links in position for 110V. For access to the modules and board, refer to section 3.12.3.

Note also that the ventilator assemblies are already wired for 110V or 220V. For 110V the two vent. fans in each assembly are connected in parallel across the mains supply. For 220V the two fans are connected in series.

3.9.2 FUSES

Fuses are provided on:

- PSU-B Module(s) (fig. 3.17a) - 6 Amp (110 V and 220V)
- PSU-M Module(s) (fig. 3.17b) - 1 Amp (110V and 220V)
- Filter Board - type D8TD1A, see figure 3.23/24 (reference S1). For access to the filter board, refer to section 3.12.3.
- Mains Distribution panel - type D8TD4, see figure 3.18. For access to this fuse the power supply rack must be swung down out of the cabinet as at section 3.12.2 (type D8TD8 must be used if mains is 110V).

3.9.3 STRAP SETTINGS IN POWER SUPPLY RACK

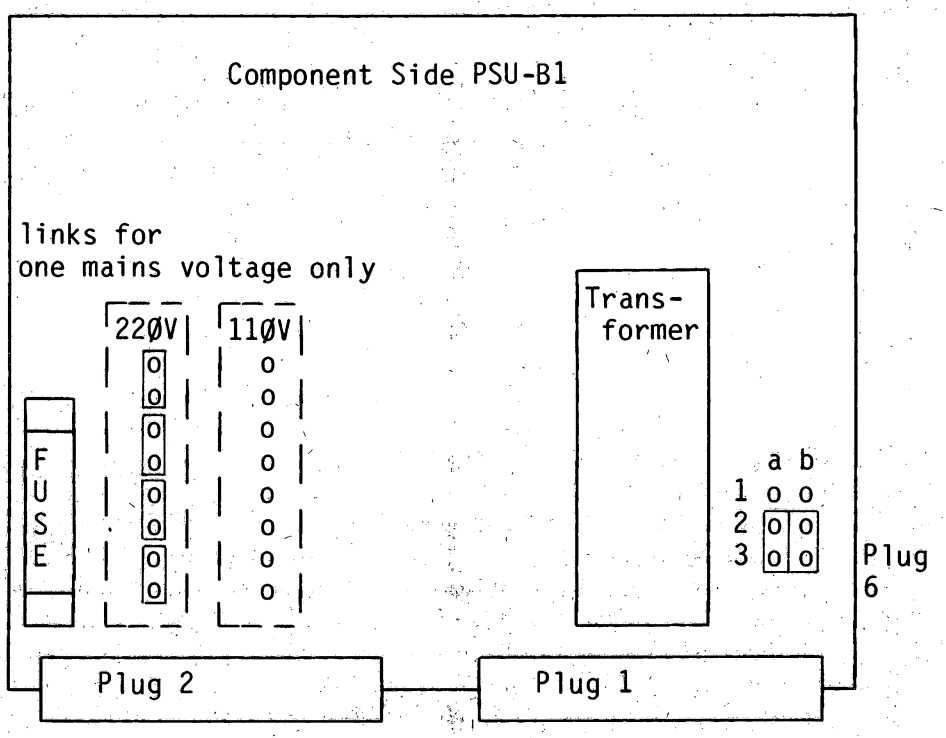
Twelve U-links and a ground connection are fitted on the card side of the power supply back panel, see figure 3.17c. For access to these U-links the power supply modules must be removed as at section 3.12.3. The five PWFN links must always be fitted. The RSLN links for the PSU-M module(s) are not necessary (because these modules do not generate or use signal RSLN) but are fitted for reasons of standardisation. The three other RSLN links must be fitted. The connection between logical and mechanical grounds must be fitted. The two BOPN/BAWOFN links are fitted according to the type of PSU-M module(s) used.

- If old PSU-M module(s) are used, the two links must be fitted vertically. (PSU-M old = 5112 291 42390).
  If new PSU-M module(s) are used, the links must be fitted horizontally (as shown in figure 3.17c). Mind also strap position Figure 3.17b.
- If there are two PSU-M modules, one new and one old; the two U-links must be fitted vertically and the BOPN/BAWOFN link on the new PSU-M module must be fitted in position BOPN.

Connector KEY on the solder side of the power supply back panel must be fitted with a plug with a link between pins 1 and 2, see figure 3.15a. For access to this connector the battery support assembly must be removed as at section 3.12.5. The test socket on the battery support assembly must be fitted with a plug with a link between pins 1 and 2. For access to this connector the power supply rack must be swung out of the rack as at section 3.12.2.

3.9.4 STRAP SETTINGS IN LOGIC RACK

The setting of U-links on the individual cards mounted in the logic rack should be checked against the information given in the system configuration sheets and in the individual service manuals. For access to the logic cards, refer to section 3.12.1. Cards should be mounted in the slots specified in the system configuration sheets.
Discrete wiring connections should be made in accordance with the system configuration sheets. These connections are made at the back of the logic rack on the UPL Bus. For access to the UPL Bus, refer to section 3.12.2.



FUSE : 110V and 220V 6 Amp

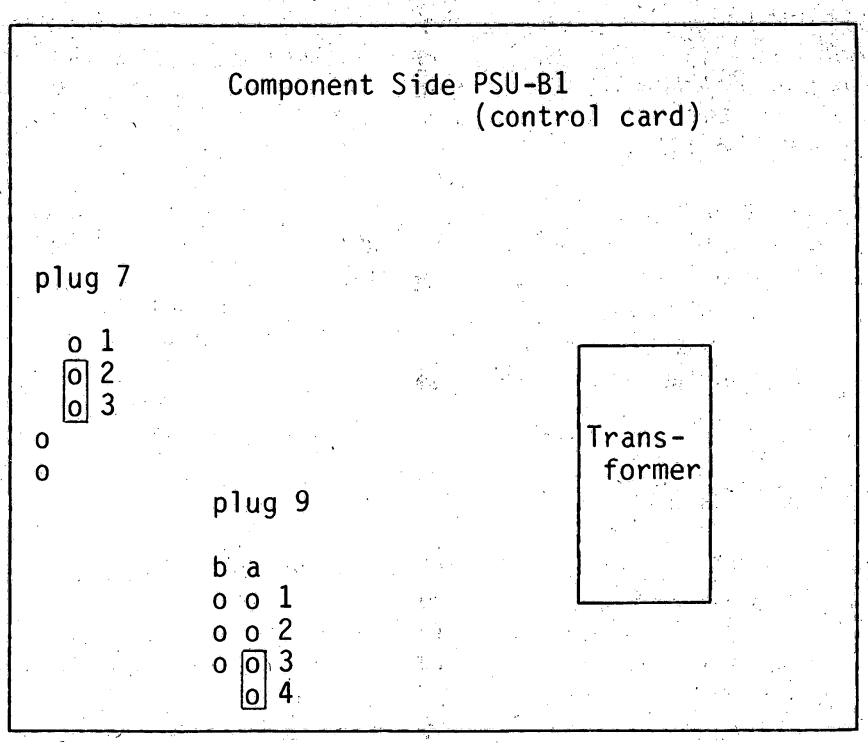
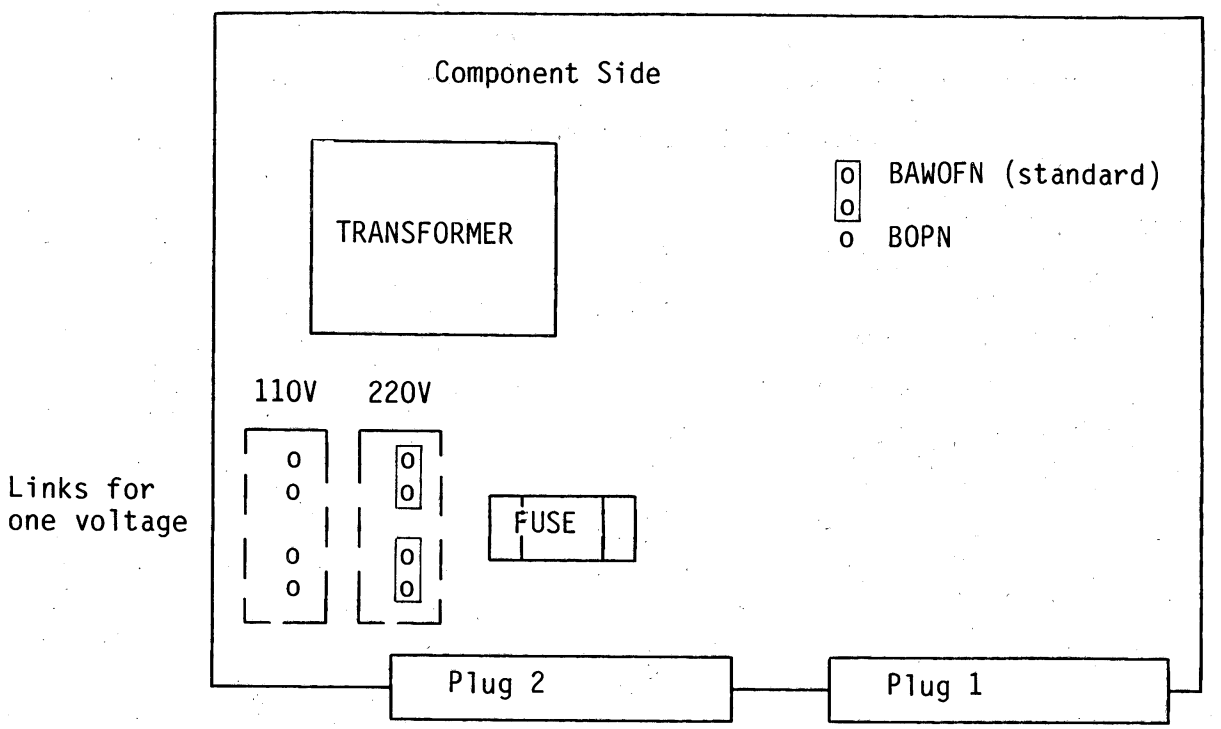


Figure 3.17a U-LINKS PSU-B1



FUSE : 11ØV and 22ØV 1A

Figure 3.17b U-LINKS PSU-M (NEW)

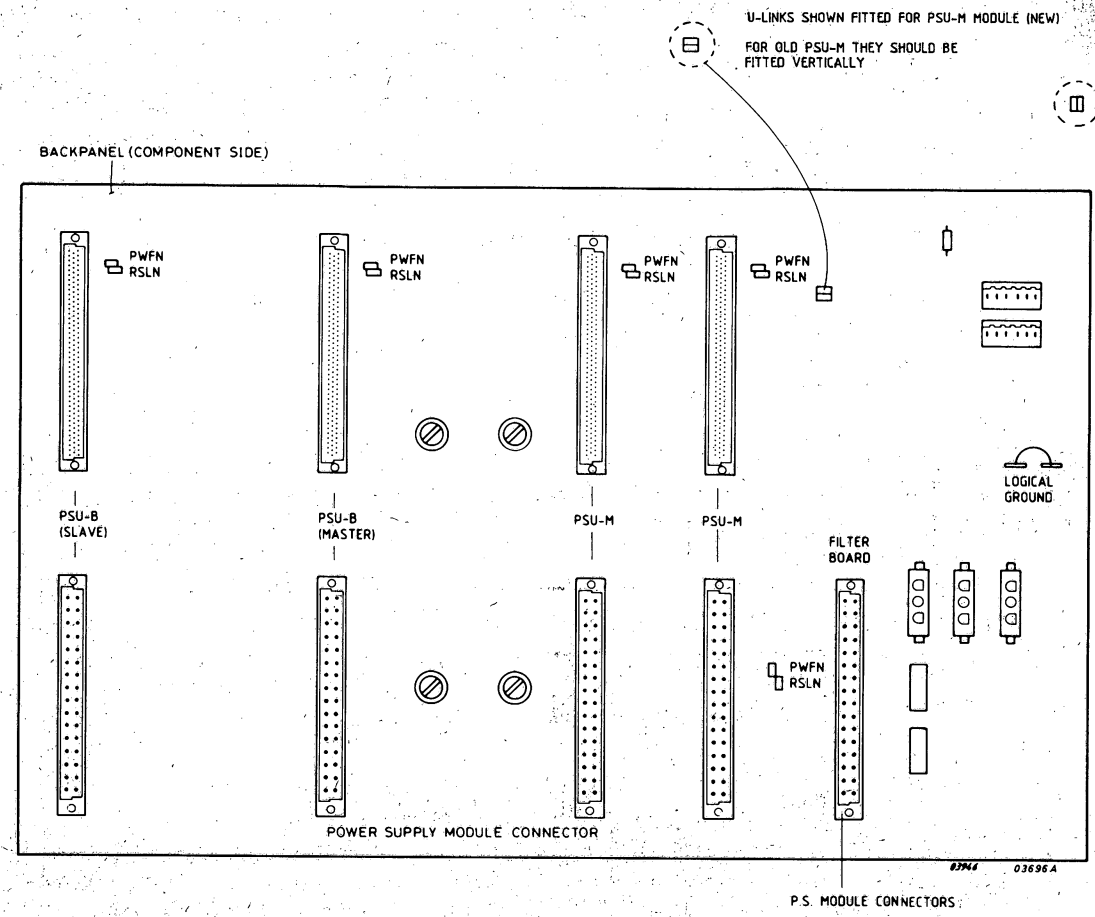


Figure 3.17c VIEW INSIDE RU22 POWER SUPPLY RACK

3.9.5 MAINS CONNECTION

The single phase mains supply is connected via a socket mounted on the rear of the Mains distribution assembly of the power supply rack, see figure 3.18.
For access to this socket, swing down the power supply rack out of the cabinet as at section 3.12.2.
The mains supply is obtained from a socket at the bottom of the cabinet, connected to the exterior. The incoming mains supply comply with the specifications given in section 3.7.3.
Before connecting the mains supply, set the key switch on the front panel to position 'OFF'.

3.9.6 ELECTRICAL CONNECTIONS

Electrical connections inside the cabinet are made with discrete wiring. The connections are shown in figure 3.18. From the point of view of parts lists the cables can be split into four groups:

CABLES PROVIDED WITH THE CABLE ASSEMBLY

- Logic Signals (to UPL) - signals PWFN, RSLN, RTCN and BAWOFN are cabled as twisted pairs, each with a ground lead, between 'Berg' connectors with key ways, on the power supply back panel (marked BPL) and the UPL Bus (connector J2 of slot Ø).

- +5VL/OV Supply - for each of the +5VL and OV supplies there are two 4-cable connectors screwed to the bus bars of the power supply rack back panel. One each of these connectors is screwed to either end of the UPL Bus +5VL and OV bus bars. This arrangement limits voltage drop across the UPL Bus.

- Other DC Supplies - the -12VL, +12VL, +12VM and +5VM supplies are cabled from a single, keyed connector on the power supply back panel (also marked BPL) to 'Faston' connectors on the UPL Bus. The 'Faston' connectors are colour coded to avoid wrong connections.

CABLES PROVIDED WITH THE KEY SWITCH ASSEMBLY

- Signal BONN - this signal is cabled as a twisted pair from connector KEY on the power supply back panel to soldered connections inside the key switch.

- Mains Switching - the mains switching cable is connected between screwed connections inside the Mains Distribution Assembly and soldered connections inside the key switch.

CABLES PROVIDED WITH THE POWER SUPPLY RACK ASSEMBLY

- -5V Supply - if a DFPC is used in the system, the -5V supply is cabled as a twisted pair with a ground lead between 'Faston' connectors on the -5V card (in the power supply rack) and on the DFPC back panel card (mounted on the back of the logic rack). If a DFPC is not used in the system, the -5V cable is stored in a plastic bag inside the cabinet.

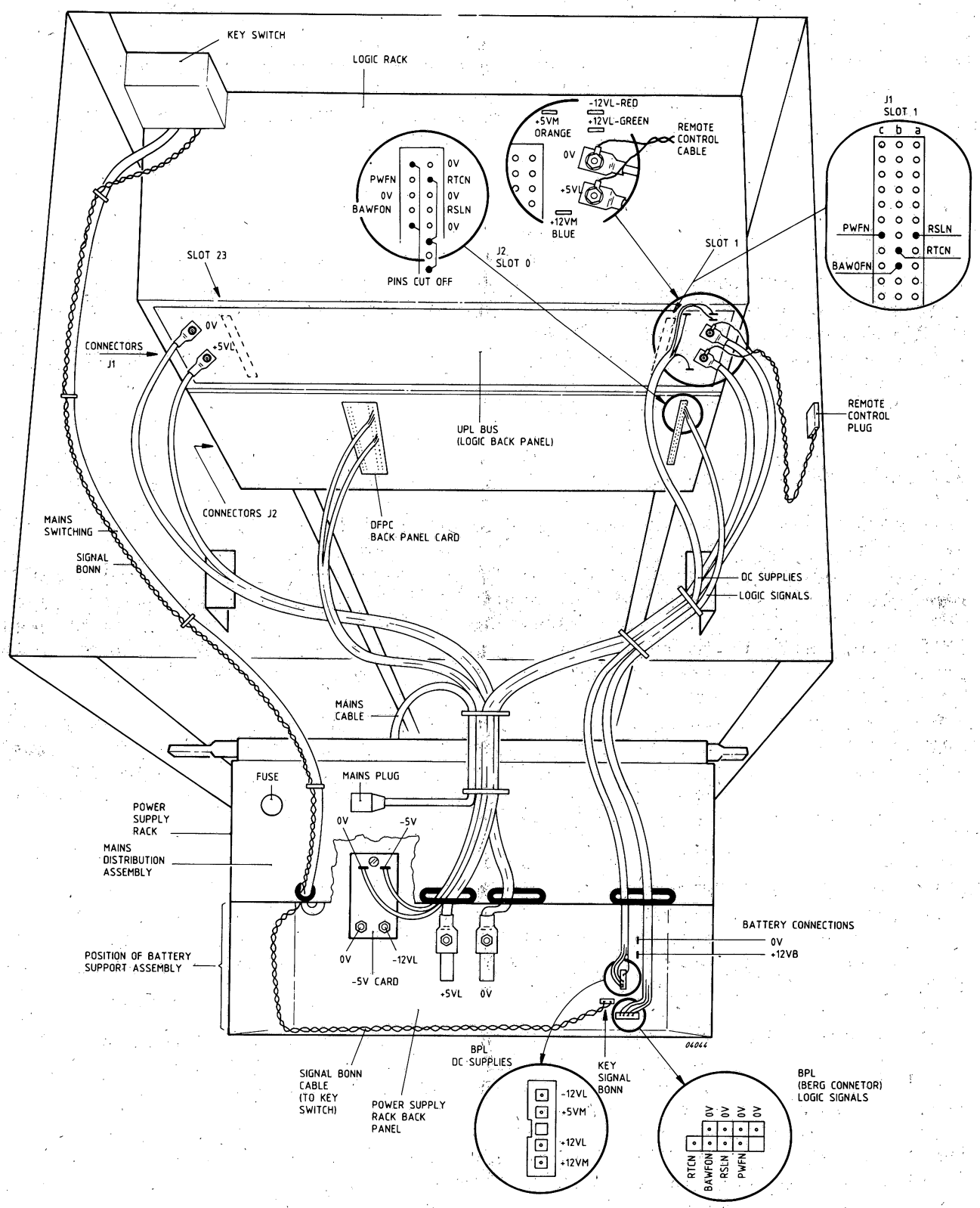


Figure 3.18 CABLING

three pin plug on the back of the mains distribution assembly from a connector mounted in the bottom of the cabinet.

- Remote Cable - the +5VL/0V supply is taken from lugs screwed onto the bus bars of the UPL Bus, to a plug mounted inside the cabinet. This supply may be used as a remote start signal for other units mounted in the cabinet.

WARNINGS

. If tests are to be carried out with the power supply switched on, very strict attention must be paid to the time taken for the test and the load on the power supply. If not, overheating could result in serious damage to the power supply modules.
. Before attempting any disassembly procedures, switch off the mains supply to the cabinet.

3.9.7 CARD/MODULE STATUS

- Several versions exist of cards and modules used in the RU22. Throughout this service manual the terms 'old' and 'new' are used as follows:

- Power Supply Rack Back Panel

  12NC number 5111 199 60350
  index 1 or 2 - old
  index 3 or above - new

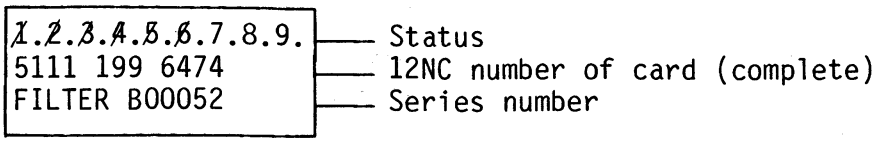
- Filter Board
  12NC number 5111 199 64740
  index 1 or 2 - old
  index 3 or above - new

- PSU-M Module
  12NC number 5112 291 42390 - old
  12NC number 5112 291 64860 - new

- For reference only - Power Supply Rack Back Panel for PTS8400 Systems
  12NC number 5111 199 63160
  index 1 - old
  index 2 or above - new

- The 12NC number of the PCB (naked) is etched into the copper of the PCB. The 12NC number of the Card (complete) is written on a white label which is stuck onto the card after manufacture.
  The status level of the card (complete) is written on the same white label. It is marked off on a series of numbers printed on the label.

Example:
Status 6



3.10 FUNCTIONAL DESCRIPTION RU22

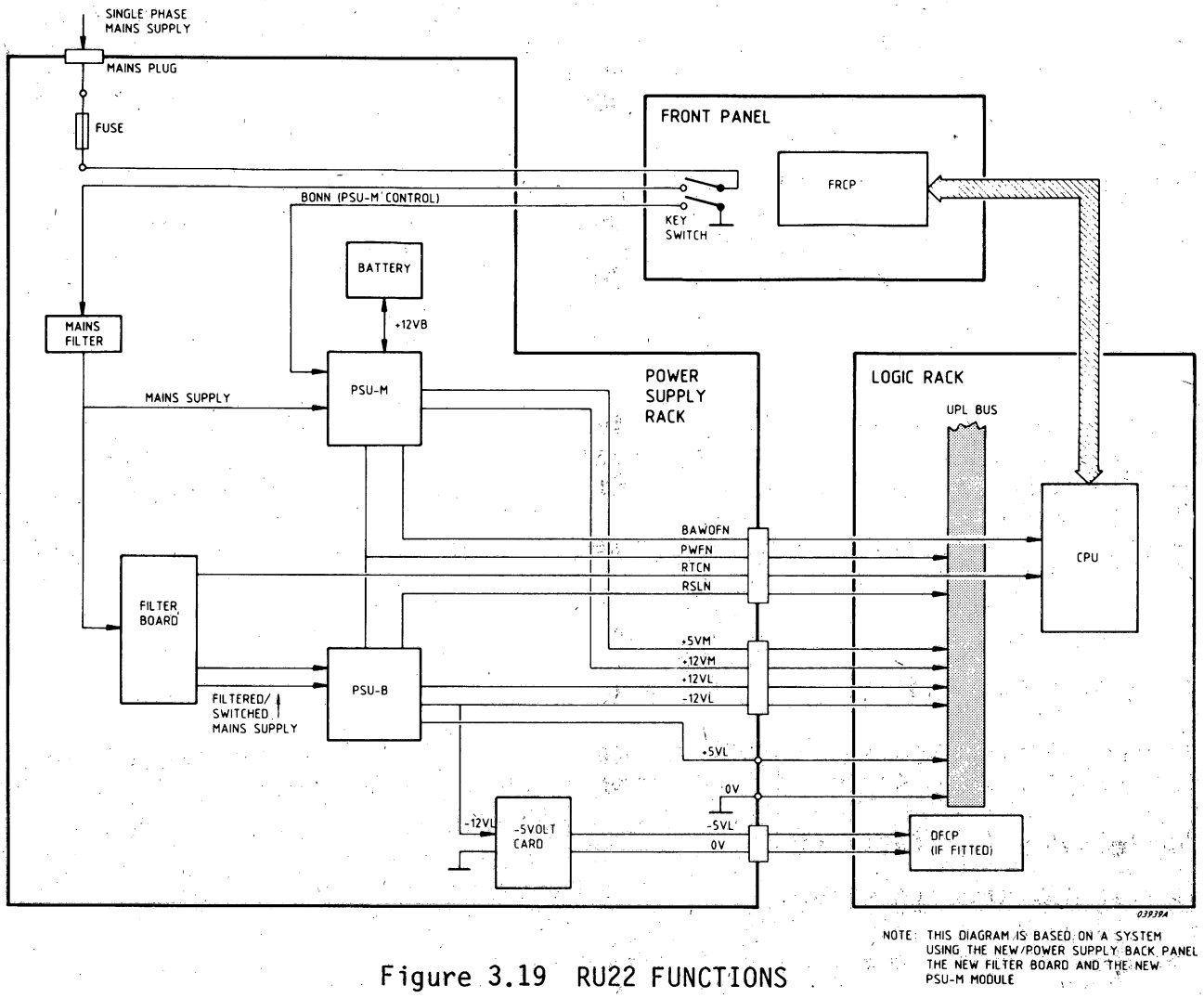


Figure 3.19 RU22 FUNCTIONS

3.10.1 LOGIC SIGNALS

The RU22 power supply rack generates the following signals to the CPU and UPL Bus:

- Power failure protection (PWFN)
- Reset logic (RSLN)
- Battery was off (BAWOFN)
- Real time clock (RTCN)

3.10.2 POWER FAILURE / RESET SIGNALS

These signals are generated during power on/power off sequences, see figure 3.21. For intermittent power failures of less than 10ms, the power supply continues to operate normally.
For failures of more than 10ms, the power supply first indicates the loss of power to the CPU by setting PWFN low. RSLN is then set low which is used by the system units as a protection and reset signal. After these two signals have been generated the power supply dc voltages fall to zero.
During switch on, after the dc supplies have stabilized, RSLN is first set inactive high, followed by PWFN.

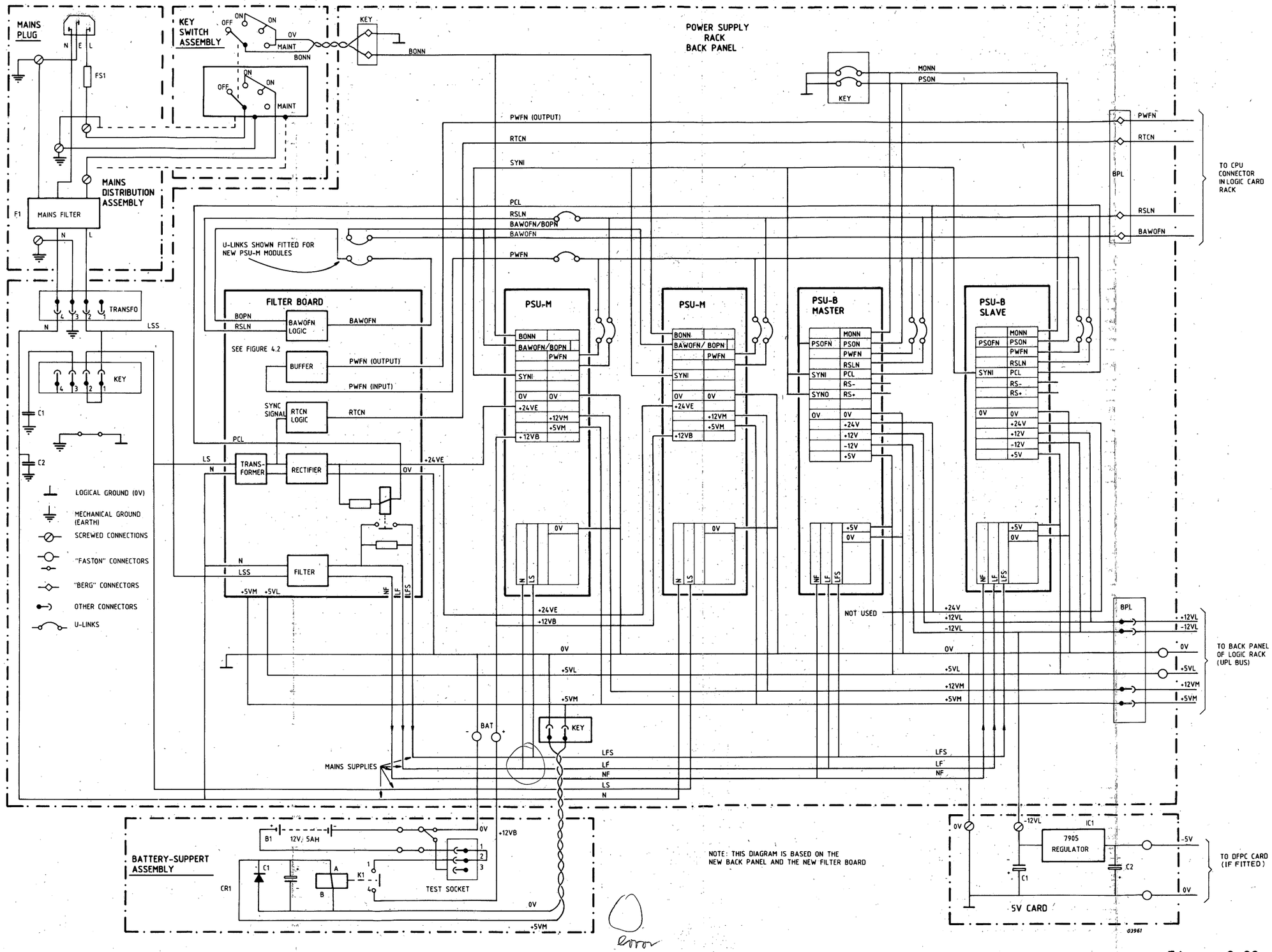


Figure 3.20 RU22 POWER SUPPLY INTERCONNECTIONS

3.10.3 KEY SWITCH POSITIONS

The following table shows the combination of functions:

POSITION	MAINS SUPPLY	LOGIC VOLTAGES	MAINTAINED VOLTAGES	BATTERY	KEY
OFF	Switched OFF	OFF	OFF	Disconnected	Free
ON	Switched ON	ON	ON powered by Mains	Recharge	Captive
ON	Switched ON	ON	ON powered by Mains	Recharge	Free
MAINT	Switched OFF	OFF	ON powered by battery	Connected	Captive

Table 3.14 OPERATOR KEY FUNCTIONS RU22

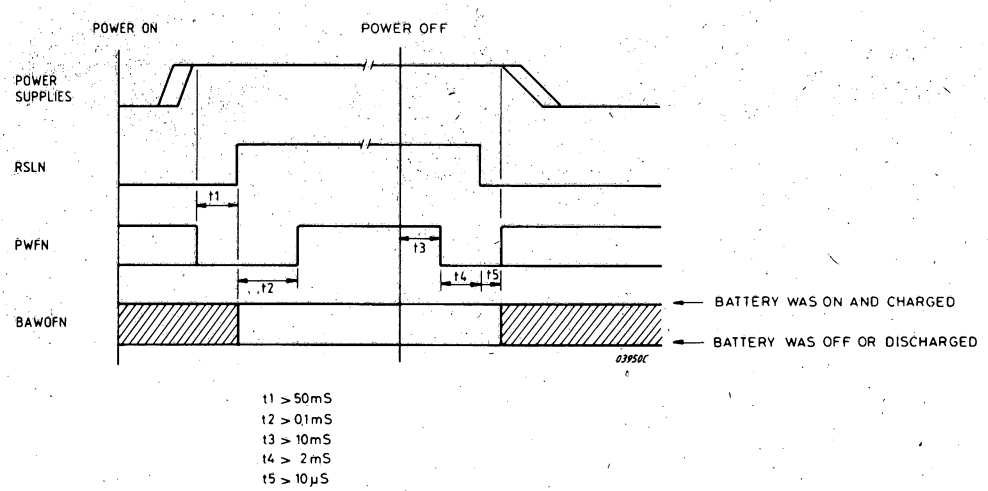
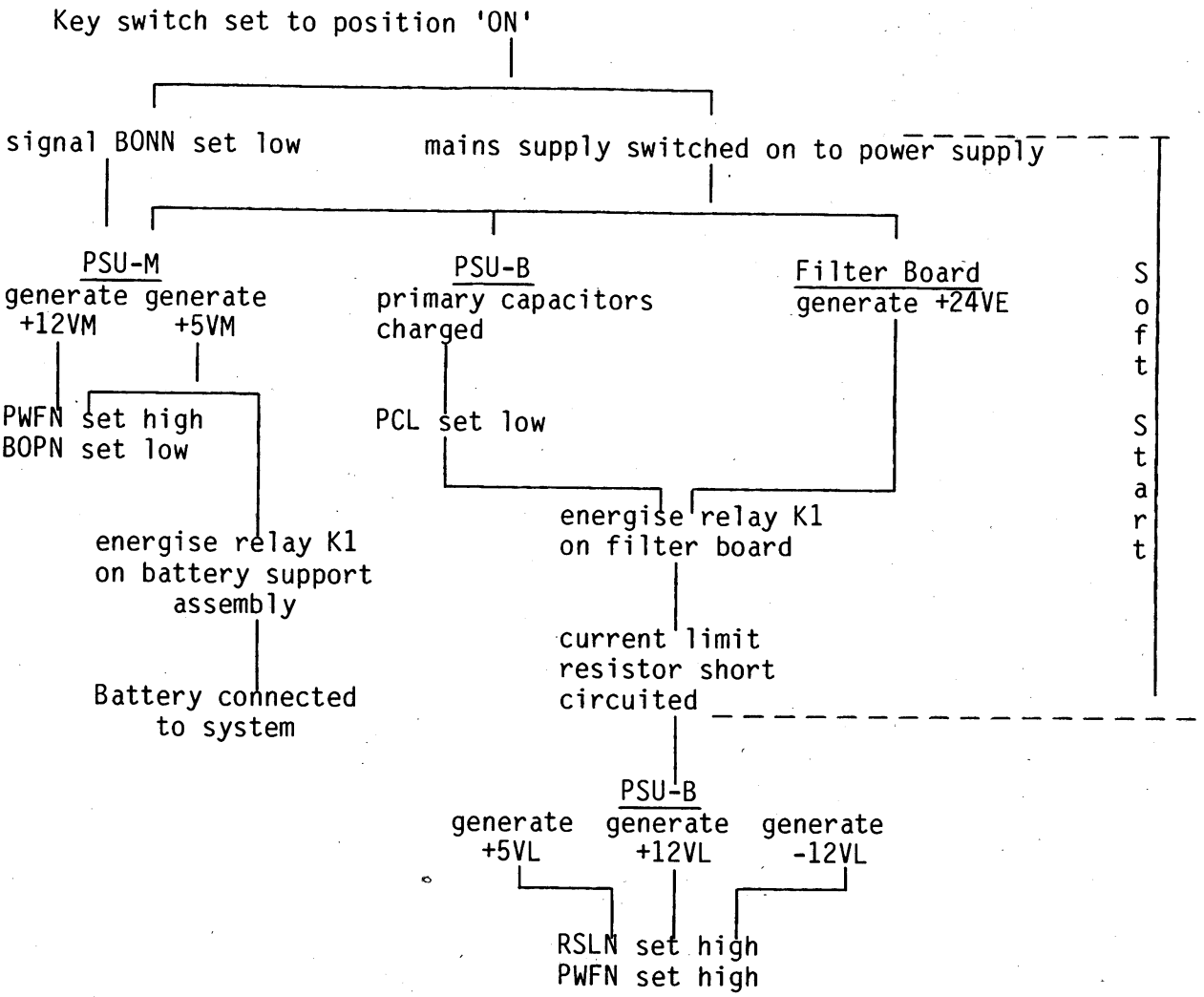


Figure 3.21 POWER SUPPLY LOGIC SIGNALS RU22

3.10.4 SWITCH ON SEQUENCE

The switch on sequence is represented in the diagram below. For the sequence of logic signals refer also to figure 3.22. Specifications for the signals are given in section 3.7.3.



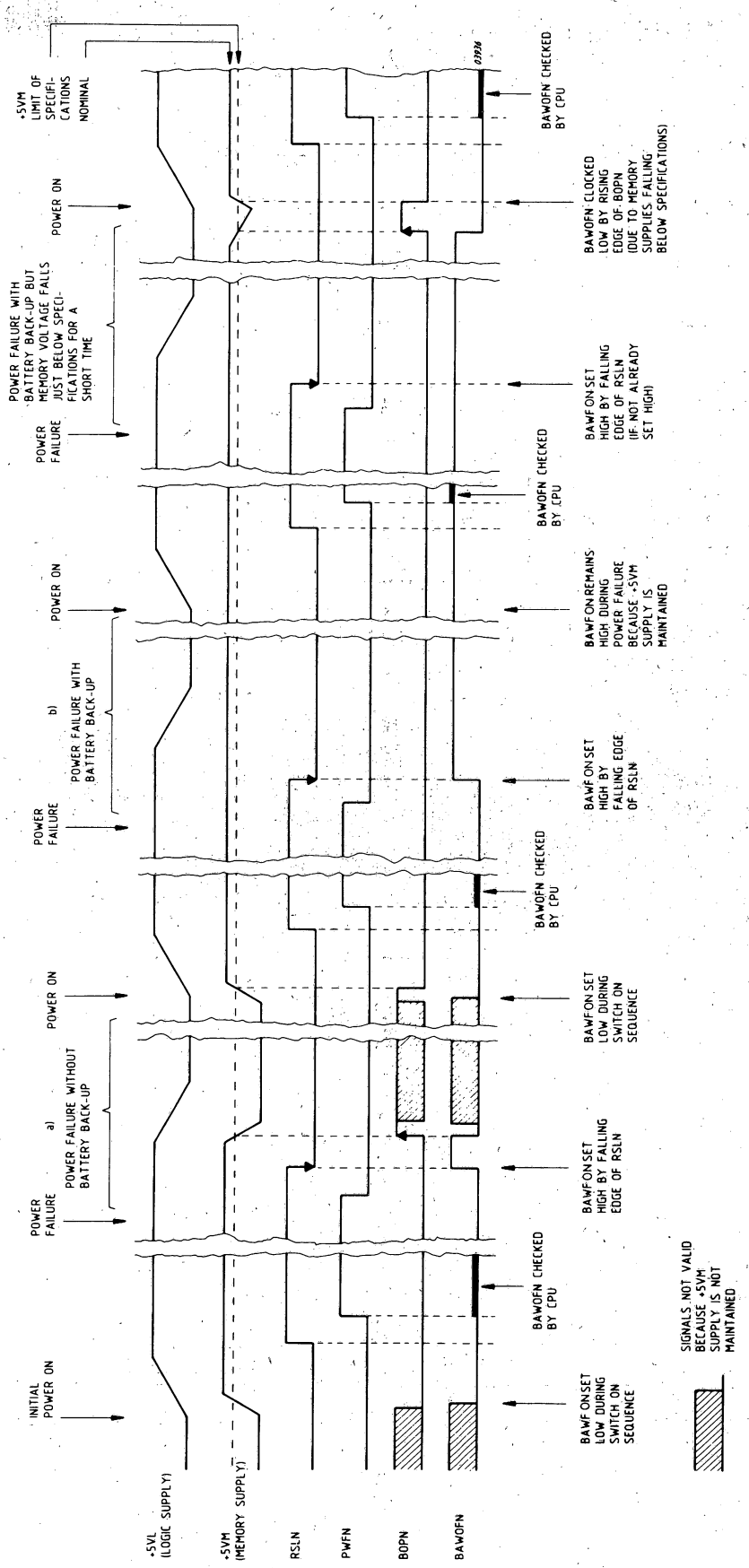


Figure 3.22 TIMING DIAGRAM FOR SIGNAL BAWOFN RU22

3.11 FILTER BOARD RU22

3.11.1 NEW VERSION FILTER BOARD

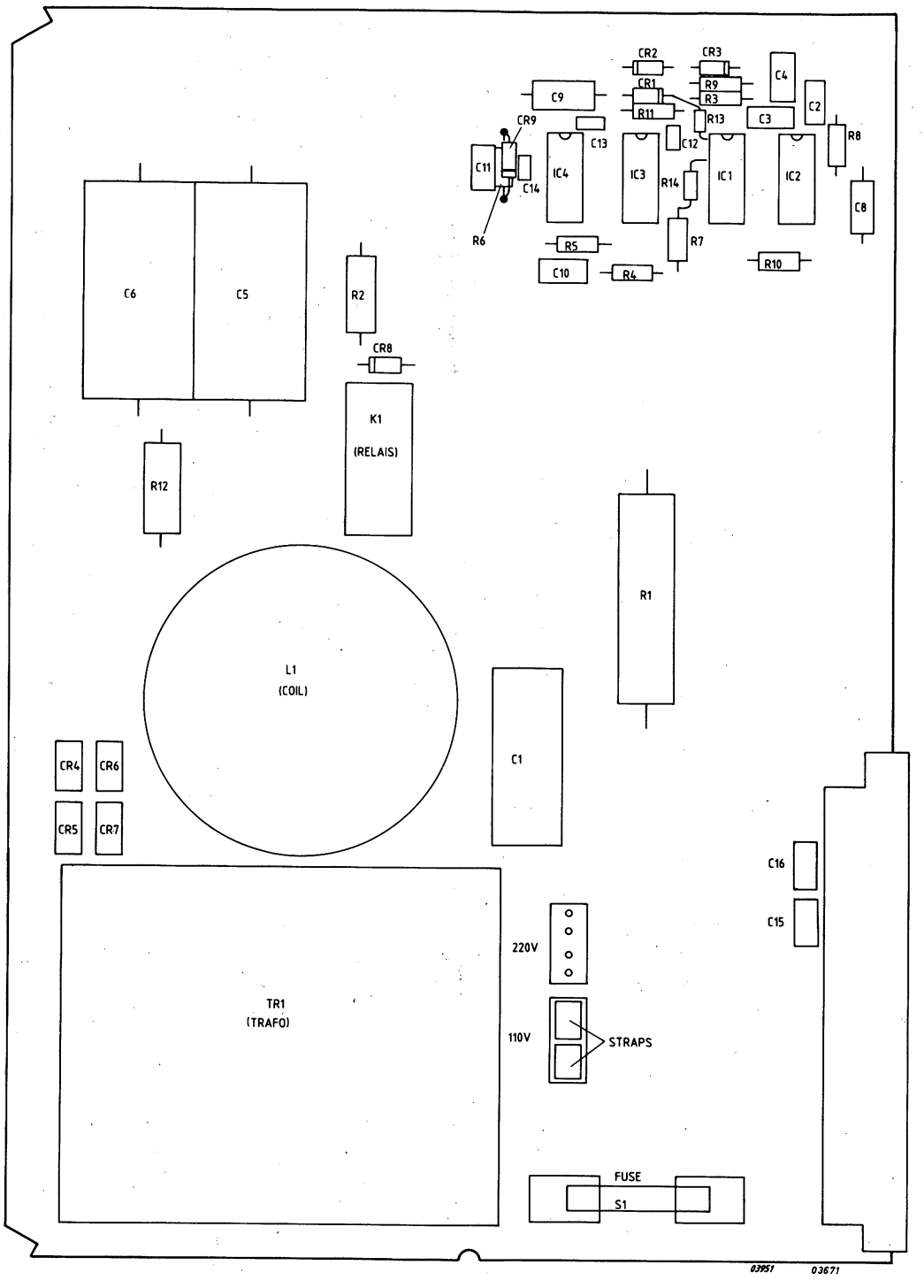


Figure 3.23a CARD LAYOUT FILTER BOARD (NEW) RU22

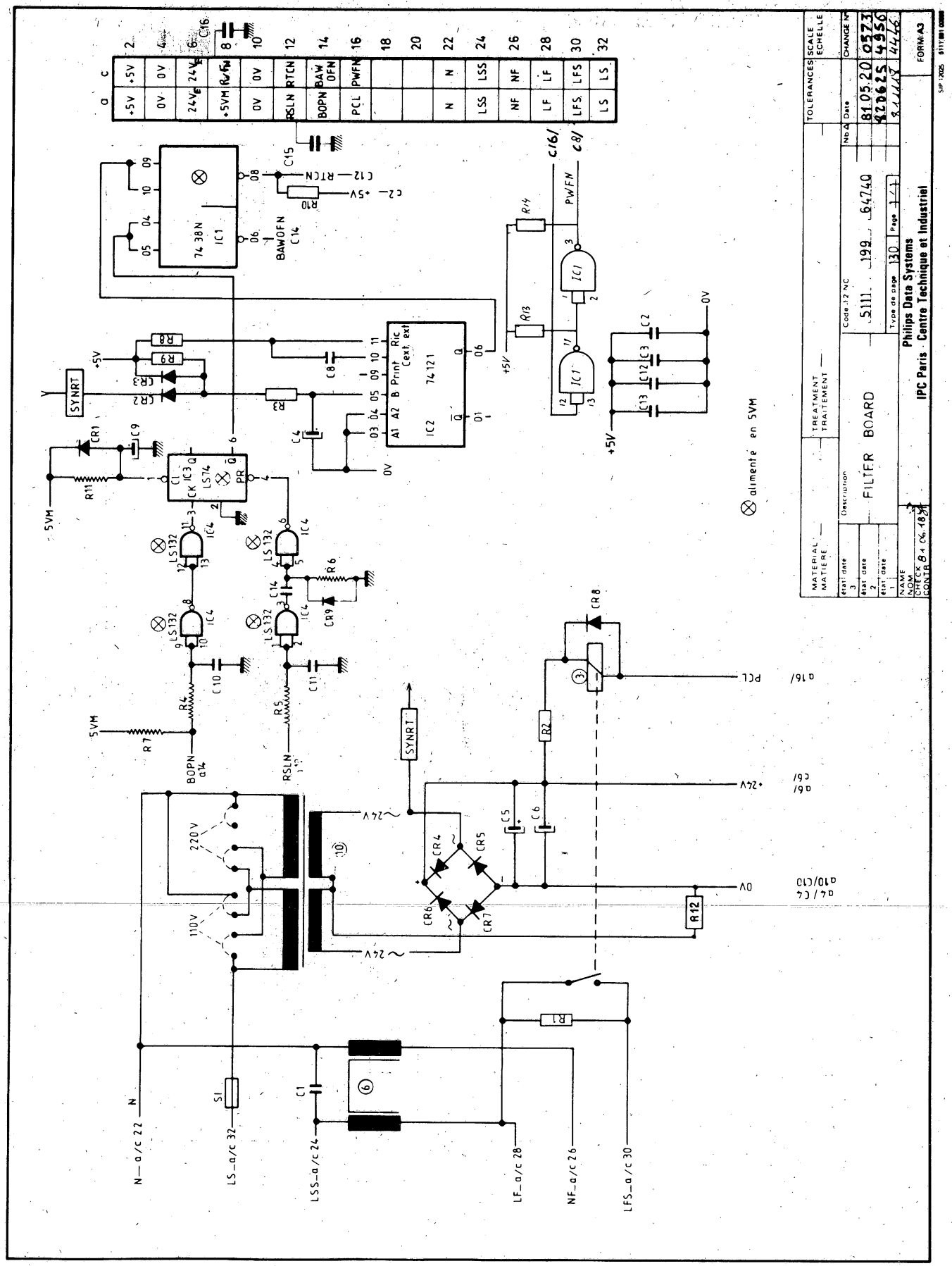


Figure 3.23b SCHEMATIC FILTER BOARD (NEW) RU22

3.11.2 OLD VERSION FILTER BOARD

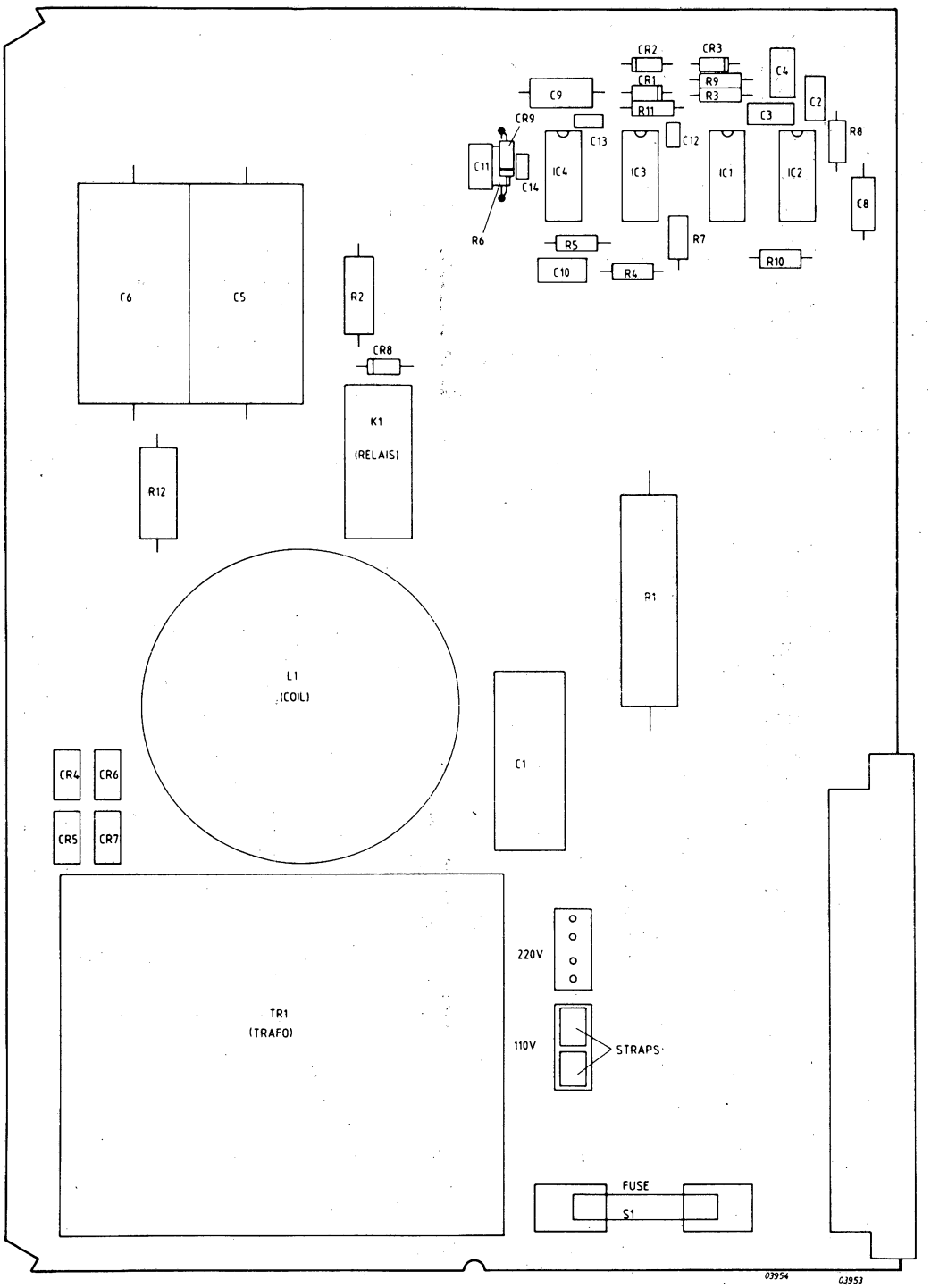


Figure 3.24a CARD LAYOUT FILTER BOARD (OLD) RU22

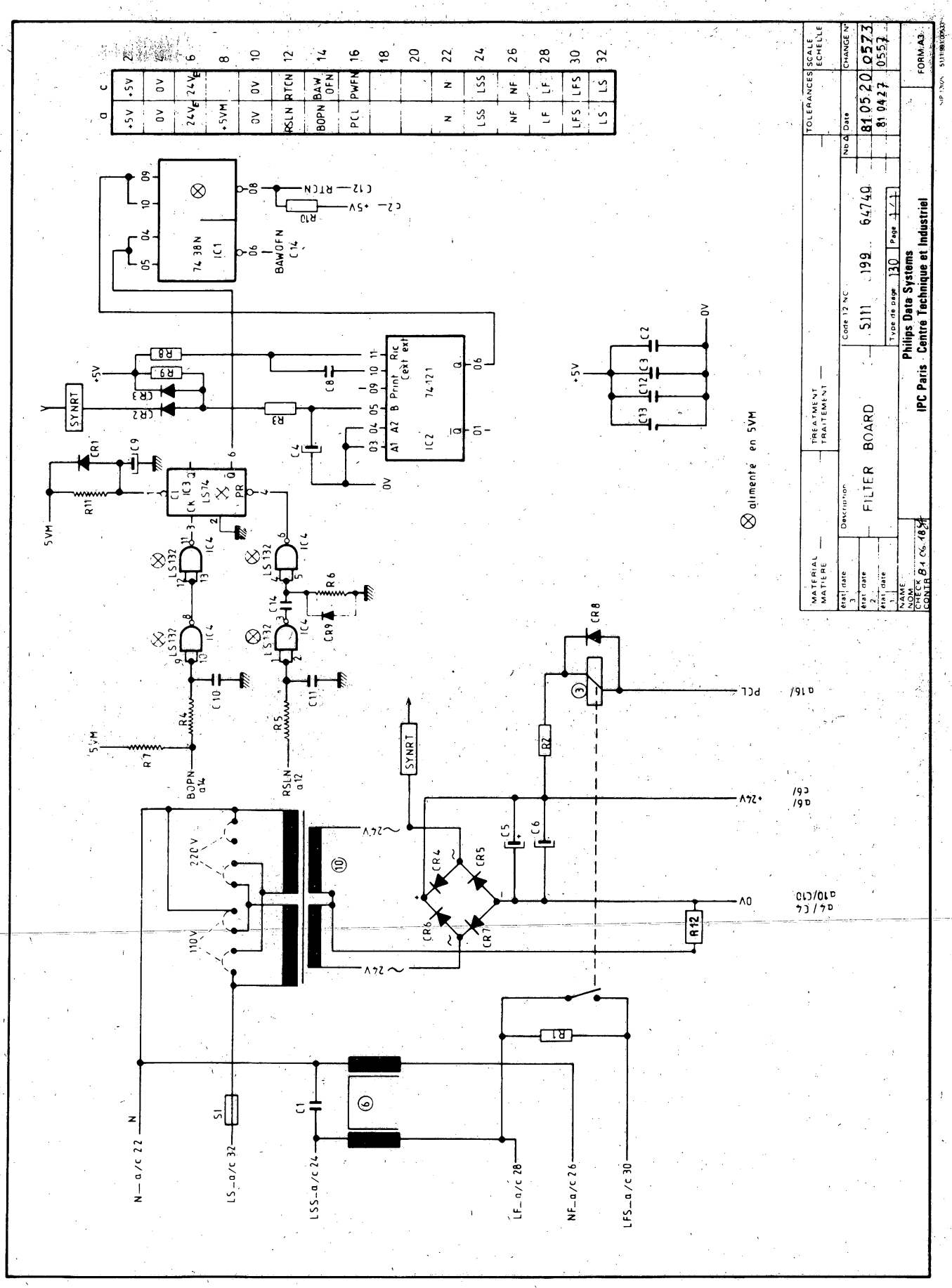


Figure 3.24b SCHEMATIC FILTER BOARD (OLD) RU22

3.12 DISASSEMBLY RU22

3.12.1 ACCESSING LOGIC CARDS AND FRCP

- Unscrew and remove the four Allen screws which hold the front panel to the front of the cabinet. Lift off the panel with FRCP (if fitted).
- Disconnect the cable from the CPU to the FRCP (if fitted) before setting the panel aside.
- Logic cards may be removed from the rack with their plastic release catches.

3.12.2 ACCESSING THE UPL BUS

- Unscrew and remove the four screws holding the power supply rack in the rear of the cabinet.

Note: If the power supply rack cover plate has been removed; either:

  - replace it (and the screws) in order to hold the power supply modules in place when the rack is swung down or
  - remove the power supply modules before swinging the rack down.

- Slide the power supply rack horizontally out of the cabinet (the ventilator assembly remains in place) until it is stopped by the pivot bar under the rack.
  Be carefull not to snag the cables inside the cabinet.
- Lower the rack down carefully - the rack swings down through 90° until it comes to rest against the cabinet.
- The UPL Bus is now accessible from the back of the cabinet.

3.12.3 REMOVING POWER SUPPLY MODULES

- Unscrew and remove the six screws holding the cover plate to the power supply rack.
- Remove the power supply front cover.
- The modules can then be removed from the rack by sliding them along the card slides.

3.12.4 REMOVING POWER SUPPLY RACK

- Remove the front panel of the logic rack as at section 3.12.1.
- Unscrew and remove the two screws which hold the keyswitch in place.
- Remove the power supply modules as at section 3.12.3 (this makes the procedure easier).
- Swing the rack down out of the cabinet as at section 3.12.2.
- Remove the connecting cables from the back of the logic rack. These are:
  . +5V and 0V supply - these are screwed connections on either side of the UPL Bus.
  . -5V supply (if connected) - these are two 'Faston' connectors on the DFPC back panel card.
  . Other DC supplies - these are connected via four colour coded 'Faston' connectors on the UPL Bus.
  . Logic signals - these are connected via a 'Berg' connector on connector J2 of slot of the UPL Bus.
  . Mains supply - remove the mains plug at the bottom of the cabinet.

- Lift the power supply rack off the pivot bar that supports it and remove the rack from the cabinet with the keyswitch assembly and connecting cable.

3.12.5 REMOVING BATTERY SUPPORT ASSEMBLY

- Swing the power supply rack down out of the cabinet as at section 3.12.2
- Unscrew and remove the five screws which hold the battery support in place. Two screws screw into the mains distribution assembly and three screws screw into the top of the power supply rack. Do not remove any other screws which holds the components onto the battery support.
- Slide the battery support towards the top of the power supply rack in order to release the two soldered flanges from under the mains distribution assembly.
- Lift the battery support away from the rack. Disconnect the two 'Faston' connectors at BAT (+ and -) and the keyed connector (not the 'Berg' connector) at KEY on the power supply back panel, before setting the battery support aside.

3.12.6 REMOVING THE MAINS DISTRIBUTION ASSEMBLY

- Remove the power supply rack from the cabinet as at section 3.12.4.
- Remove the battery support assembly as at section 3.12.5.
- Unscrew and remove the seven screws which hold the mains assembly to the rack) (two on each side and three along the bottom). Do not remove any other screws which hold components onto the assembly.
- Slide the three oval shaped rubber grommets (which secure the cables to the logic rack) out of their slots in the mains assembly.
- Lift the mains assembly off the rack.
  In chapter 6 the layout of the mains distribution assembly is shown. This diagram is shown from the component side of the assembly i.e. from inside the power supply rack.

3.13 TESTING THE BATTERY RU22

A test socket is mounted on the rear of the battery support assembly for testing the battery without removing it from the power supply. To gain access to the socket the rack must be swung down out of the cabinet as at section 3.12.2

For normal operation a plug is inserted with a link between pins 1 and 2. This connects the battery to the system via the contact of a small relay mounted on the battery support.

1) To totally isolate the battery in case of faults, simply remove the plug.
2) To measure the charge/discharge current connect an ammeter across pins 1 and 2 in place of the link (pin 1 positive wrt pin 2 when the battery is discharging).
3) To measure the battery voltage connect a voltmeter across pins 1 and 3 (pin 1 positive).
   After testing the battery always replace the link.

3.14 EQUIPMENT SHELF E2 (P843-001)

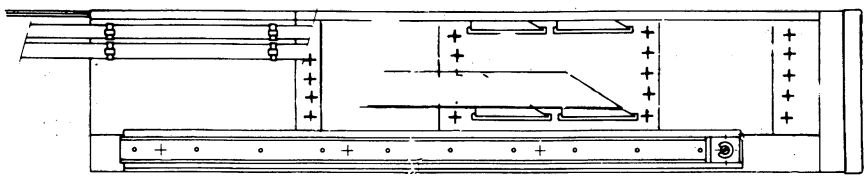
Equipment Shelf : E2.

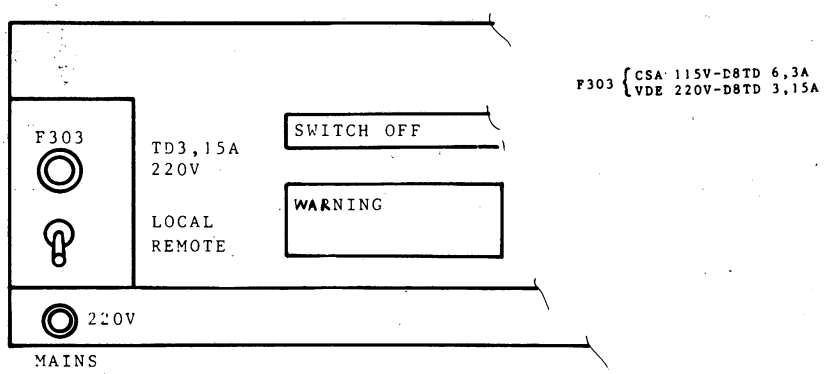
Number of Slots : 6 sub-assembly slots for control units connected directly to the GP Bus.

Size : Height 3U (approx. 132.5 mm).

Power Supply : +5V 18A
+18V 2A
-18V 2A

Other Facilities : Where the Equipment Shelf is situated at the end of the GP Bus a termination is necessary. The Bus can be terminated by the inclusion within the shelf, or the required termination boards.





MAINS INPUT VARIATIONS

Figure 3.25 EQUIPMENT SHELF P843-001 LAYOUT (E2)

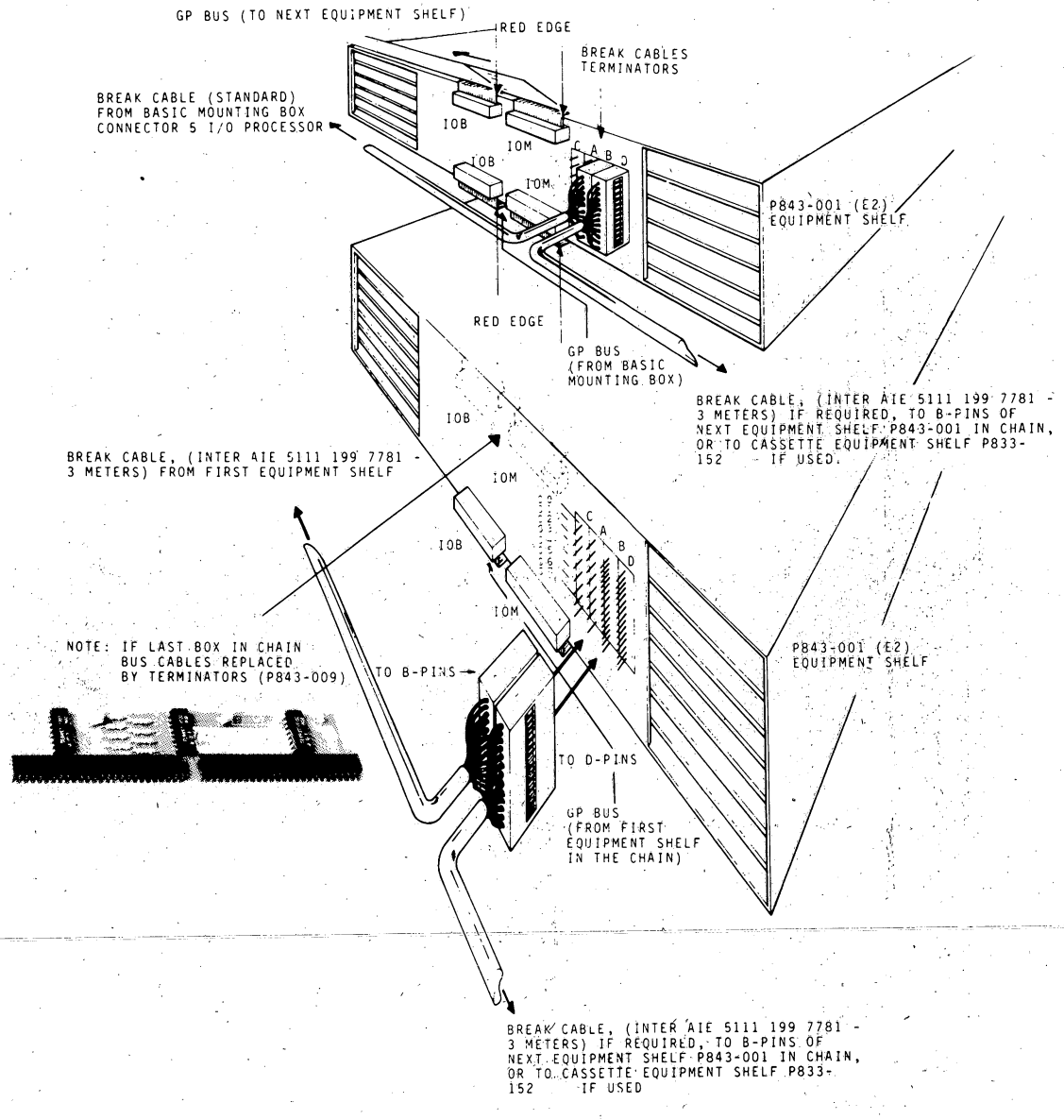


Figure 3.26 BUS AND BREAK CABLE EXTENSION (E2) (USING P843-001 EQUIPMENT SHELF)

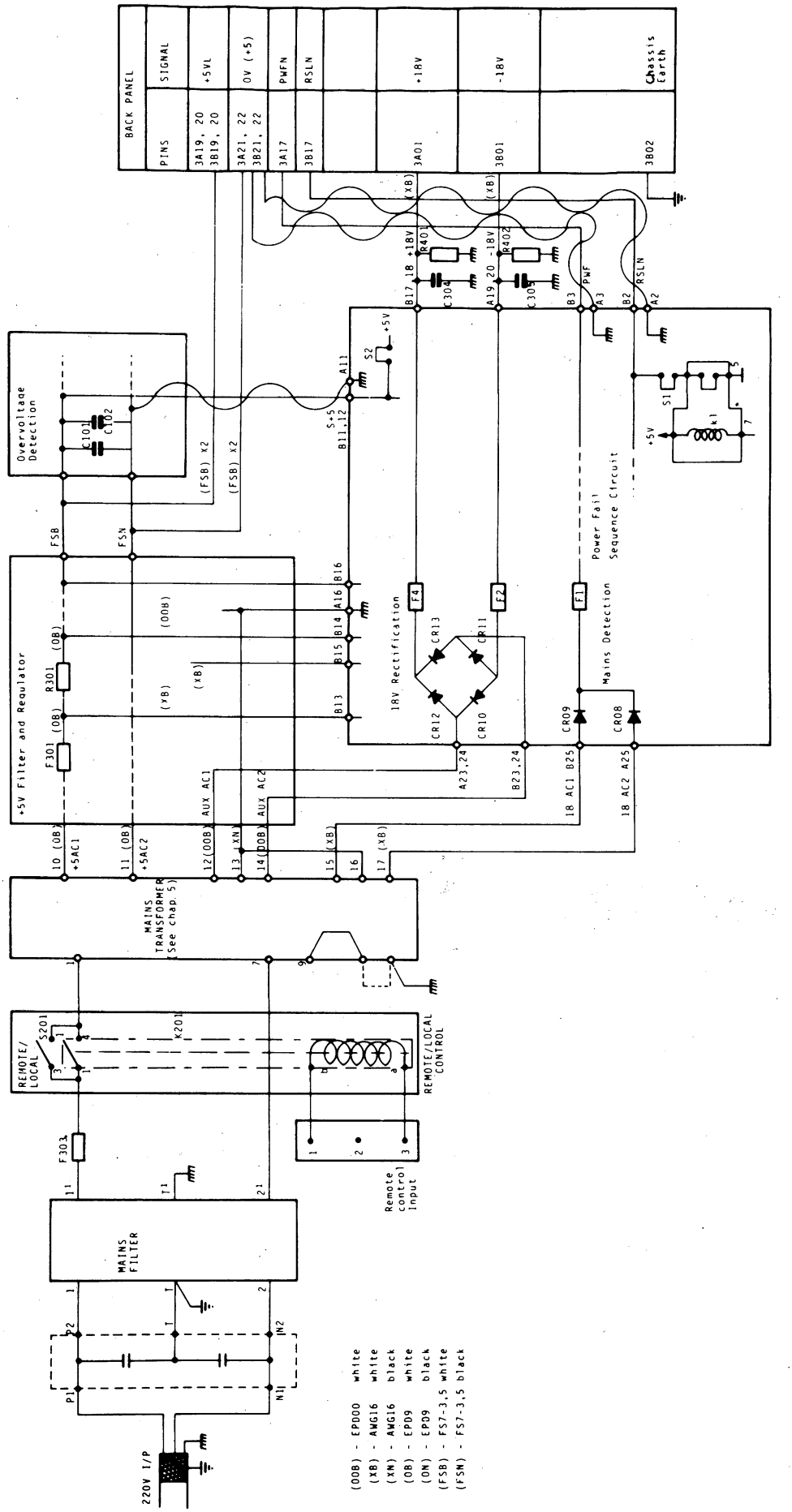


Figure 3.27 EQUIPMENT SHELF P843-001 CIRCUIT-DIAGRAM (E2)

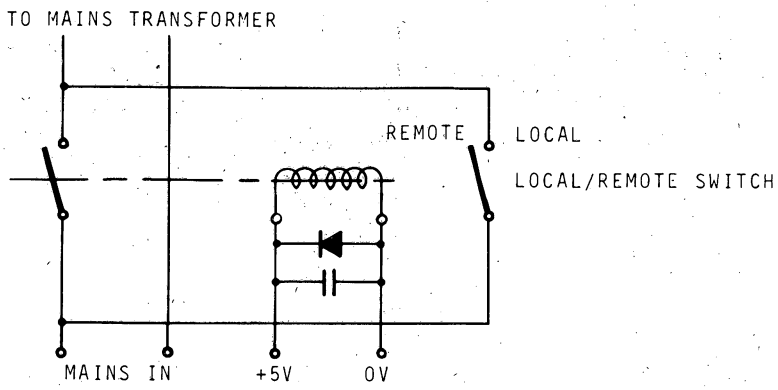


Figure 3.28 REMOTE CONTROL CIRCUIT P843-001 AND P833-152 EQUIPMENT SHELVES

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4.1 INTRODUCTION

Each P800 computer system is supplied with a set of configuration Sheets (that were compiled when the system was tested in the factory) which give the following details:

. Invoice sheet of the system or units ordered.

. Parts list specifying the major items in system (including I/O cards and logic options.

. Wiring instructions for the interconnecting and signal cables.

With the information in these sheets most systems can be installed without any problem; however, for large systems (and when enlarging existing systems) problems can arise which are not always covered by the Configuration Sheets.

4.2 SITE PREPARATION

Extensive site preparation is not normally required before installing a system. For simple configurations that will be part of a much larger existing system no site preparation is necessary. In general the only requirement is a floor strong enough to support the component parts of the system. A floor able to support a static loading of 500 kg/m^2 is strong enough for any mini-computer system.

4.2.1 ENVIRONMENTAL CONDITIONS (TABLE 4.1)

The CPU can operate through a wide range of environmental conditions so the need for air conditioning etc., will depend on the peripherals used by the system. It is expected that the CPU and its peripherals will be located in an office/factory environment where the air is not contaminated by industrial processes. The general conditions for storage (with or without packaging), transport and operating are given in the following two tables; however, peripherals using magnetic media may specify more stringent conditions.

CLIMATIC CONDITIONS		O	NO	T
Temperature Range		0 to 50°C	-40 to 70°C	-40 to 70°C
Temperature Gradient		.LE. 1° C/mn	.LE. 1° C/mn	.LE. 1° C/mn
Pressure		600 to 1100 mb	600 to 1100 mb	600 to 1100 mb
Humidity without Condensation	RH%	.LE. 95%	.LE. 95%	
	TRE	.LE. 40°C	.LE. 40°C	
	DEW POINT	.LE. 30°C	.LE. 30°C	

Table 4.1 CLIMATIC CONDITIONS

MECHANICAL CONDITIONS	O	NO	TS
Vibrations	Freq. Range: 10-58Hz Peak Value : 0.75mm	Freq. Range: 10-500Hz	Freq. Range: 10-500Hz.
		Peak Value: 0.75mm	Peak Value: 0.75mm
	Freq. Range: 58-500Hz Acceleration: 0.5 g.	Acceleration: 1g.	Acceleration: 2.5g.
	Sweep Rate: 1 oct./mn	Sweep Rate: 1 oct./mn	Sweep Rate: 1 oct./mn
Shocks	Acceleration: 5 g.	Acceleration: 15g.	Acceleration: 15g.
	Duration: 11ms	Duration: 11ms	Duration: 11ms
	Motion: Half-sine One direction: -Oz	Motion: Half-sine One direction: - Oz	Motion: Half-sine Six directions

Note: For Operating conditions, the vibrations and shocks are those encountered at rack level.

Table 4.2 MECHANICAL CONDITIONS

4.2.2 ELECTRICAL REQUIREMENTS

A single phase a.c. supply complying with the following specification should be provided for the exclusive use of the computer system. It should be either a 3 wire single phase, neutral and earth, or two phases and earth; its current carrying capacity must be adequate for the total power requirements of both the CPU and the peripherals. The requirements are:

Voltage: : 115V, 220V or 240V r.m.s. ± 10%

Frequency : 50±2Hz or 60±3Hz

Voltage Transients : 1.5kV peak amplitude for a duration not exceeding 10 microseconds between half peak points at a repetition frequency of 3 to 10Hz. for not more than 10 minutes.

Transient State : The time between the voltage falling from nominal to zero and then returning to nominal must be not greater than 0.5 seconds.

Power Interrupts : Less than one every 10 seconds for a duration not exceeding 10ms.

If the mains supply is subject to frequent interruptions or failures, it is advisable to install an alternative supply source such as a rotary motor/generator.

4.3 CONFIGURATION GUIDE

This guide mainly concerns operational access and uniformity of appearance, but is not important as far as system performance is concerned. The only critical layout restrictions concern the interconnecting peripheral signal cables and transmission lines. The rack is divided into imaginary levels and table 4.3 shows the recommended positions for the different units.

LOCATION	ITEM	UNITS* REQUIRED	
		Front	Back
Level 7 (2 units)	Nameplate Ventilation Unit	1 -	- 1
Level 6 (7 units)	Tape Punch Equipment Shelf	6 3,4,5	- 3,4,5
Level 5 (7 units)	6U6/6U12/RU22 Punched Tape Reader Tape Punch Equipment Shelf	6 3 6 3,4,5,	- - - 3,4,5
Level 4 (7 units)	6U6/6U12/RU22 Punched Tape Reader Tape Punch Moving Head Disc Equipment Shelf	6 3 6 6 3,4,5	- - - 6 3,4,5
Level 3 (7 units)	Moving Head Disc Tape Punch Equipment Shelf	6 6 3,4,5	6 - 3,4,5
Level 2 (3 units)	Equipment Shelf	3	3
Level 1 (4 units)	Power Distribution Panel Magnetic Tape Formatter	- -	3 2
Levels 5+6 or 3+4 (14 units)	Magnetic Tape Transport	14	-
Levels 2+1	Magnetic Tape Formatter Tape Punch	- 6	2 -

* 1 unit = 1.75 inches = 44.45 mm.

Table 4.3 RECOMMENDED UNIT POSITIONS

4.4 RULES FOR CONNECTING GROUNDS IN A SYSTEM

Each cabinet must have a mechanical ground or safety earth point to which the safety earth points of all the units mounted in the cabinet are connected. This safety earth point must be electrically connected between the main frame and the earth wire of the power cable supplying the cabinet from the site mains. Each cabinet must also have an electrical ground of OV and the shields of cables must not be used as inter-unit safety earth conductors. Cable shields must be connected to the safety earth using earthing leads as short as possible and of the same cross sectional area. To avoid either internal or inter-cabinet Electromagnetic interferance, the mains cables to the different units should be mounted against the left-hand side of the mainframe and the I/O cables should be mounted against the right-hand side of the mainframe (as indicated in Chapter 2, Figure 2.8).

4.4.1 GROUNDING RULES FOR MOUNTING BOXES AND CABINETS

The following rules should ensure a good ground continuity between the cabinets and the mounting boxes:

- Fixed Mounting Boxes
  These mounting boxes are fastened to the mainframe by screws and a good continuity between the cabinet and the box is ensured by keeping the mating surfaces clean.

- Slide Mounted Boxes
  A box mounted on telescopic slides does not have a reliable ground path so it is essential that an electrical link is made using metal braid. Remember using the ground conductor of the main lead or cable shielding for the ground connection is NOT acceptable.

- Cabinet Panels and Doors
  All doors and panels must have a good electrical link to the mainframe and in particular the doors must be connected with metal braid.

The following diagram shows some examples:

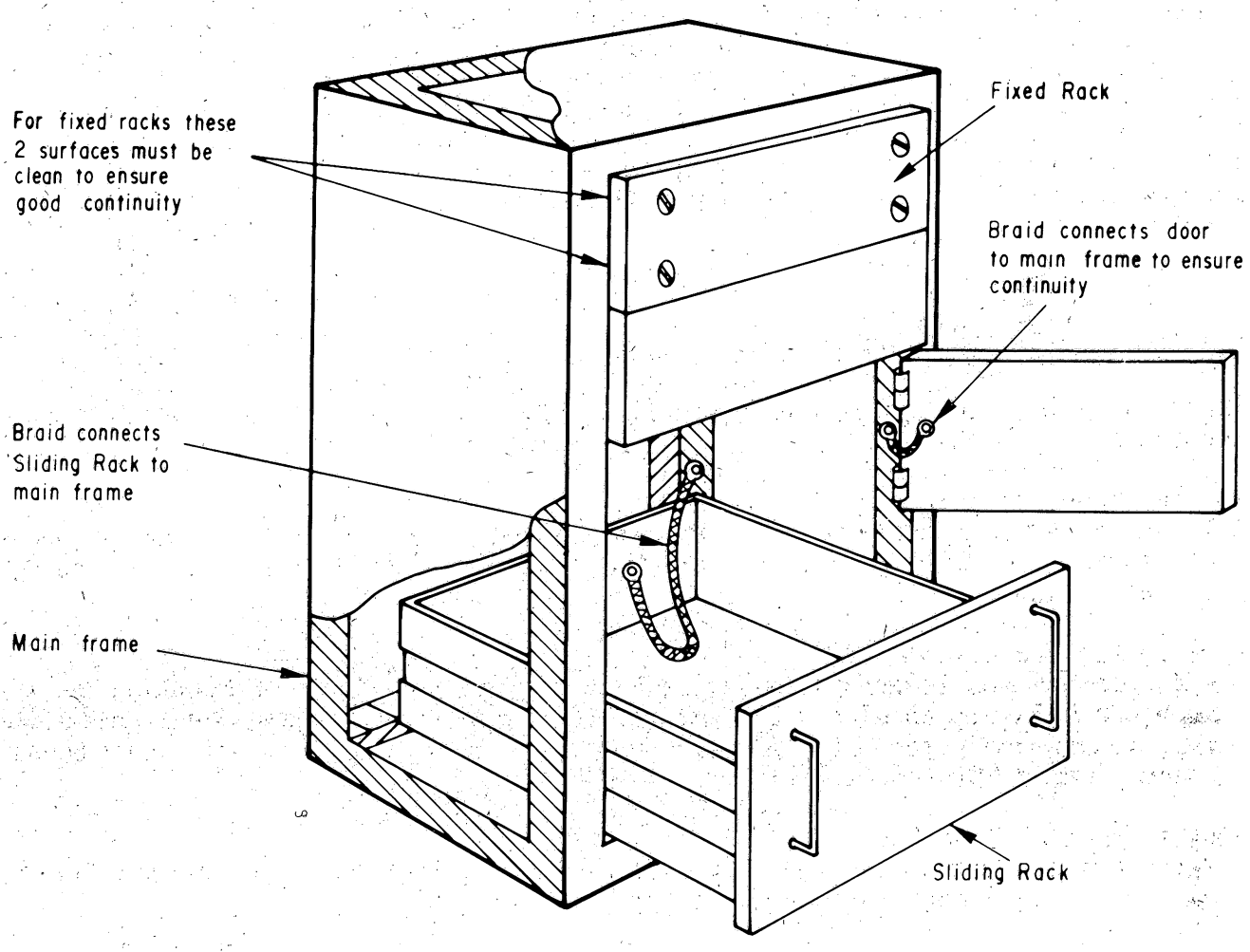


Figure 4.1 EXAMPLE FOR SYSTEM GROUNDING

4.4.2 LOGIC GROUND AND MECHANICAL GROUND

Logic ground and mechanical ground points are provided in each cabinet. They are situated close to each other and may be either connected or disconnected.
Figure 4.2 gives an example for Flexible Disc Drive shelves.

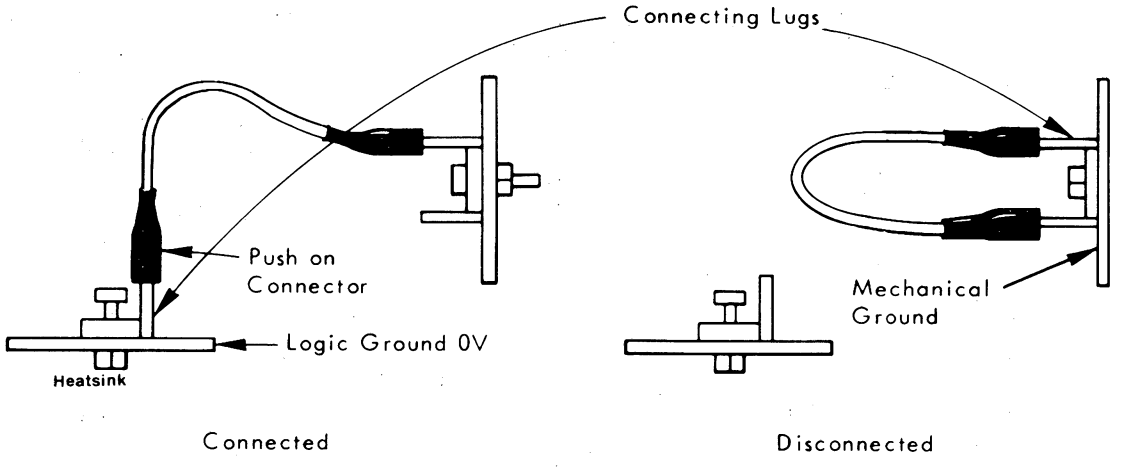


Figure 4.2 LOGIC AND MECHANICAL GROUND

A system may use several cabinets each containing a number of Mounting Boxes, but only one may have this link connected. All other cabinet links are disconnected.

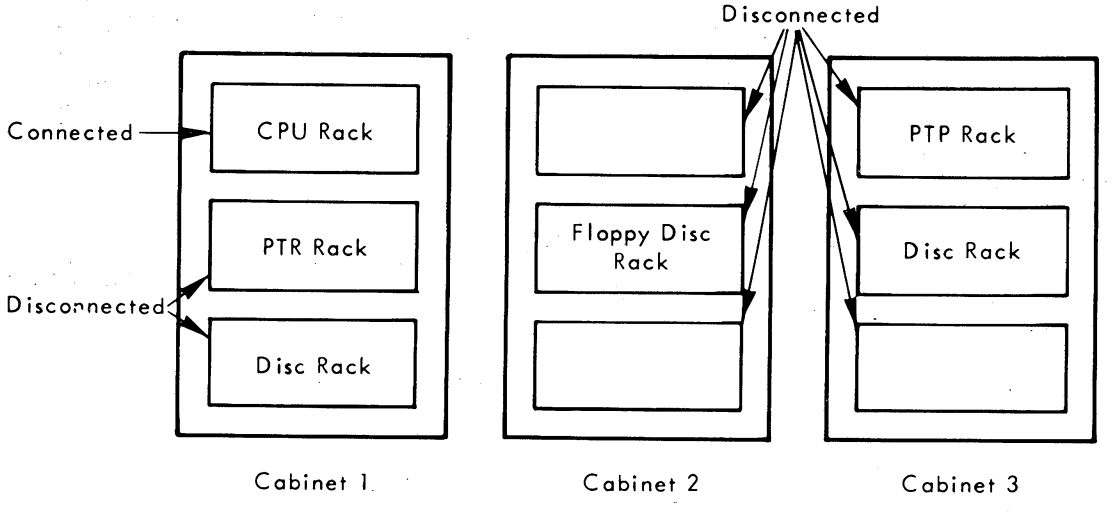


Figure 4.3 GROUNDING OF MOUNTING BOXES

In a normal configuration the cabinet that holds the CPU/CIP is connected and all other cabinets are not connected. If more than one CPU/CIP is being used in the system then the user decides which CPU/CIP cabinet is to have the link connected.

4.4.3 FLAT CABLES

Flat cables without shielding may cause electromagnetic fields to be set up in the equipment, so the use of such cables should be avoided. If this is not possible, the following special precautions must be taken:

- If channel type supporting members are in the cabinet, then they should be used so as to provide a shield around the cable.

- If these supporting members are used, then the cables should be run separately; either clamped flat against the panels or against the outside of other supporting members.

- Mounting flat cables one on top of the other should always be avoided. If this method must be used, then a metal plate (suitably supported and electrically connected to the cabinet) should be inserted between the cables.

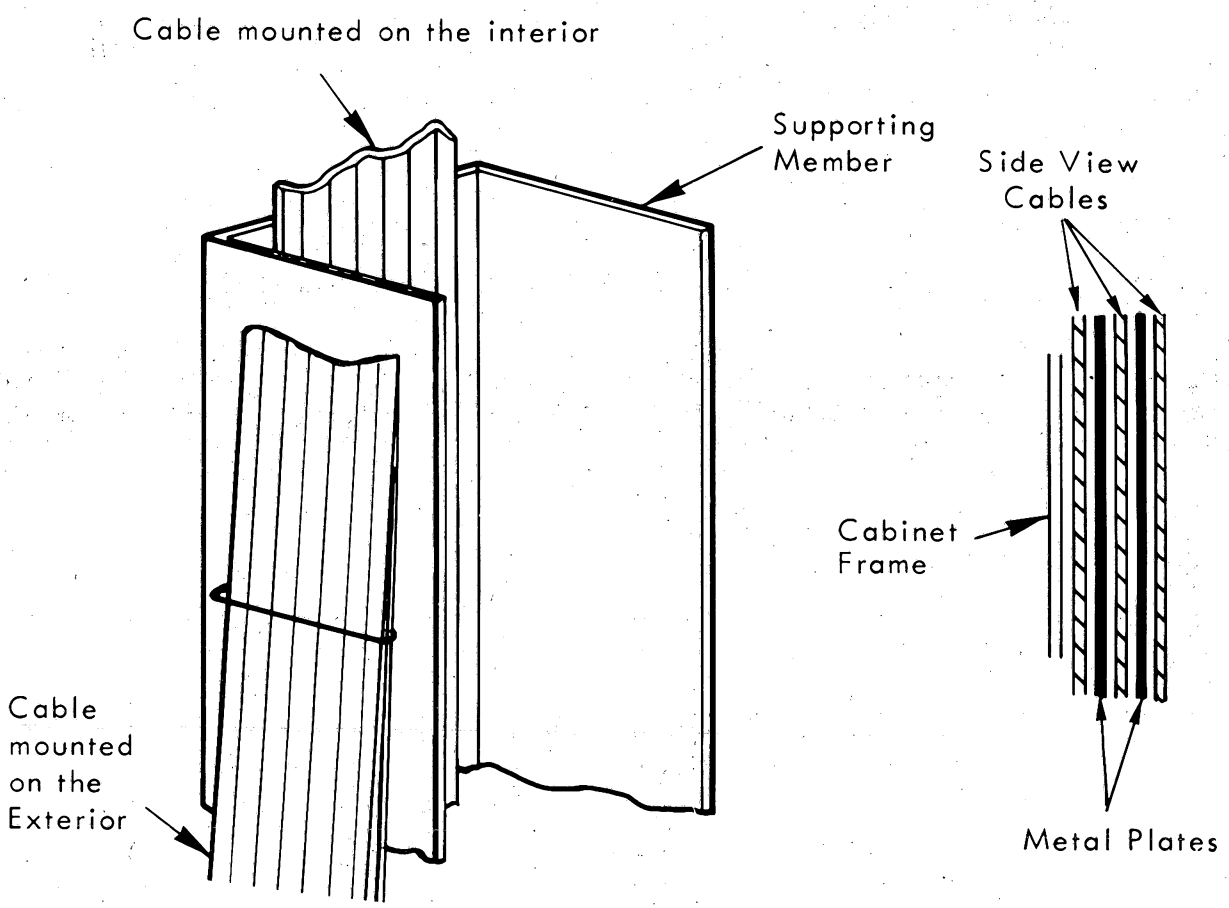


Figure 4.4 FLAT CABLE MOUNTING

4.4.4 MAINS CABLES

When planning an installation, an area along the mainframe should be reserved for the mains cables and all other cable should be kept as far as possible from this part of the mainframe. It is recommended that the cable be shielded either before or after the mains filter and that this shielding be connected to the mechanical ground at each end of the cable. The mains cable must be secured to the chassis by a metal clamp at the point where the shielding extends outof the cable sheath. Remember that the screw fixing the ground conductor to the chassis must be as close as possible to the metal cable clamp.

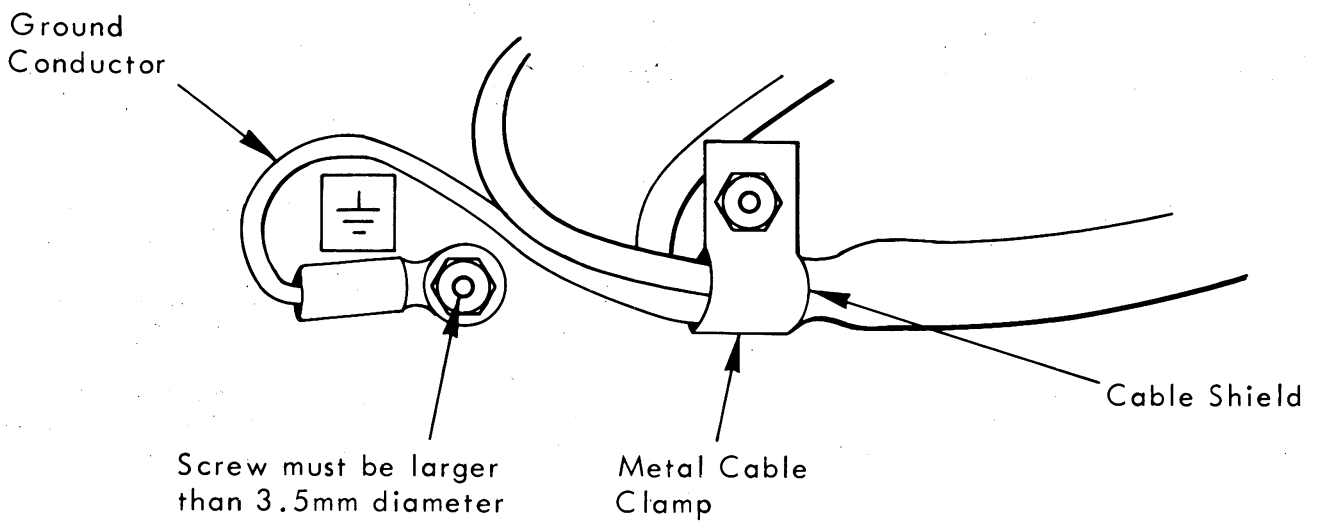


Figure 4.5 MAINS CABLE MOUNTING

4.4.5 GENERAL RULES FOR SHIELDED CABLES

All twisted pairs must be contained inside a shielded cable and this shield must be connected to mechanical ground at each end. Specific lead dimensions are given for some peripherals but as a general rule the following dimensions should be adhered to:

- The lead must be as short as possible and never exceed a maximum length of 15 cm.
- Connections to the shielding must be soldered and connections to the mechanical ground must be made with either an eye-lug (for a 3 mm screw) or a push-on type connector (Faston 6.35 or equivalent).
- The cross section of the lead must be a minimum of AWG16 guage.

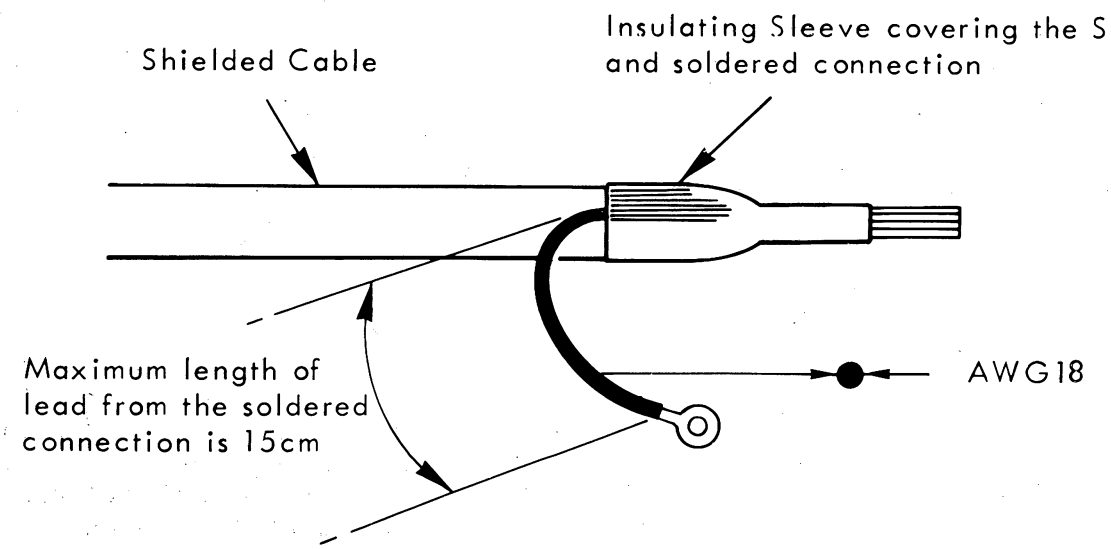


Figure 4.6 SHIELDED CABLE MOUNTING

4.4.6 SPECIAL RULES FOR SHIELDED CABLES

For some devices the lead dimensions for connecting the shielded cables at the device and at the CPU/CIP are different from the general rules. These devices are listed in the following table.

	AT THE DEVICE			AT THE CPU/CIP		
	AWG	MAX. LENGTH	EYE LUG	AWG	MAX. LENGTH	EYE LUG
Magnetic Disc X1215/16	16	20cm	4mm	16	15cm	3mm
Magnetic Disc 9760/9762	16	08	3	16	10	3
Line Printer X1415/25	16	10	3	16	10	3
PER3100 (V24 Interface)	16	15	4	16	10	3
PER3100 (Curr. Loop Int.)	16	15	4	18	03	Molex pin 3
ASR33 (V24 Interface)	16	10	3	16	10	3
ASR33 (Curr. Loop Int.)	18	03	Molex pin 6	18	03	Molex pin 3
Tape Reader 2540EP	16	10	3	16	10	3
Card Reader CM300L	16	10	4	16	10	3
Tape Punch 4070	16	10	4	16	10	3
Display P817	16	10	4	16	10	3
	At the Terminal Box					
Remote Control Cables	18	10	--	18	03	Molex Center Pin
Break Cables	At the Extension Box					
	16	10	3	16	15	3
Break Cables	At the Cassette Box					
	16	10	3	16	15	3

Table 4.4 SPECIFIC LEAD DIMENSIONS

4.4.7 GROUND LEADS IN CABINETS OR BOXES

The connection of ground leads for cabinets or boxes depends on the type of installation. The following examples show the different type of ground connections:

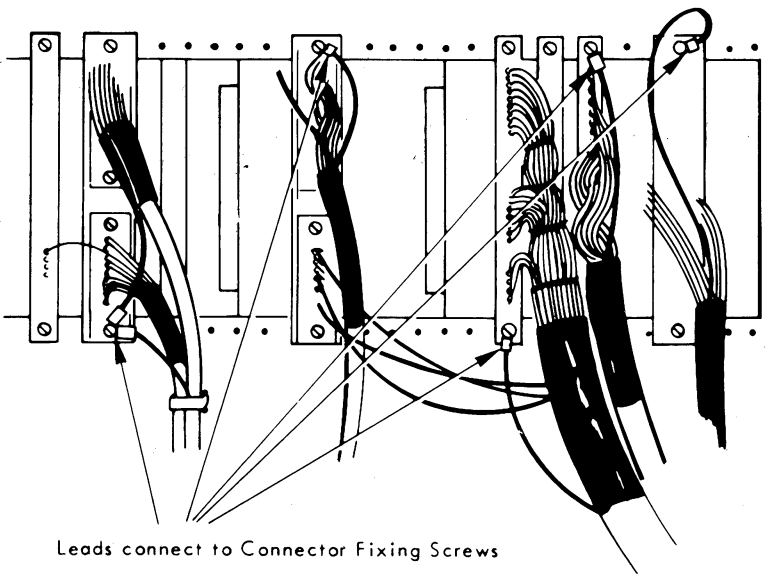


Figure 4.7 EXAMPLE USING CONNECTOR FIXING SCREWS

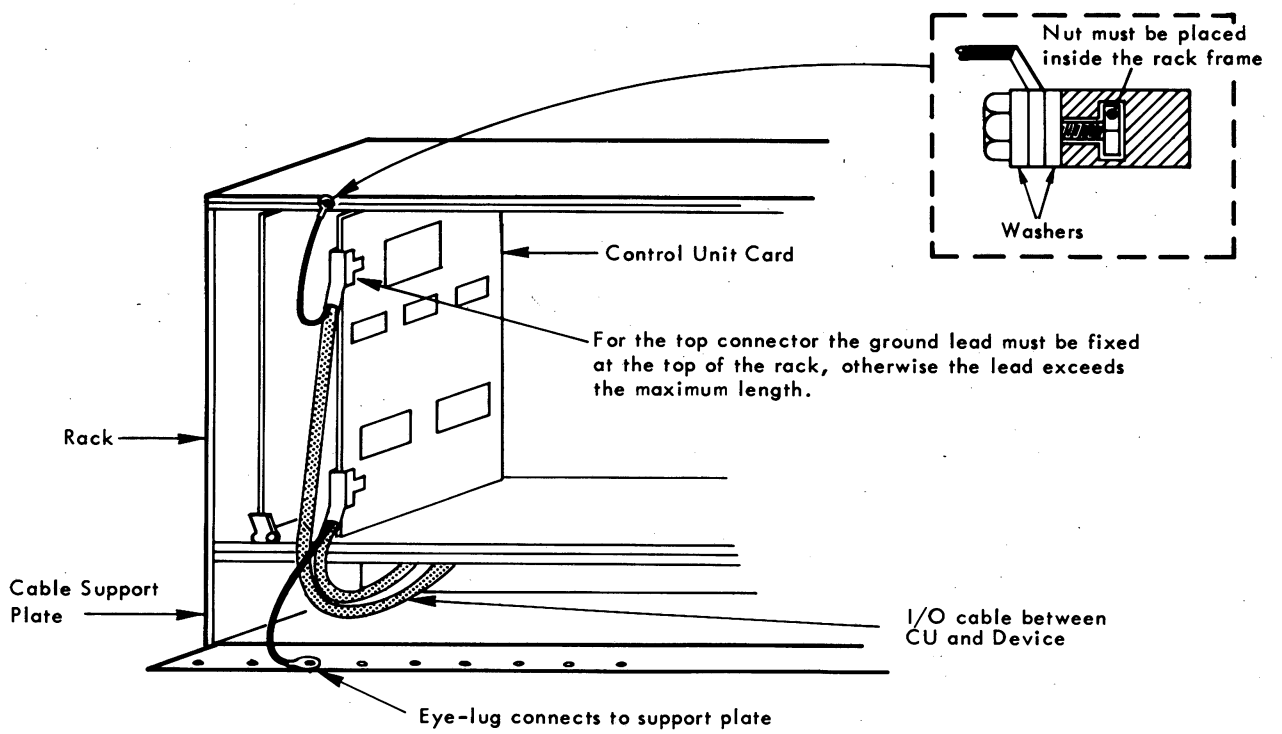


Figure 4.8 EXAMPLE USING CABLE SUPPORT PLATE

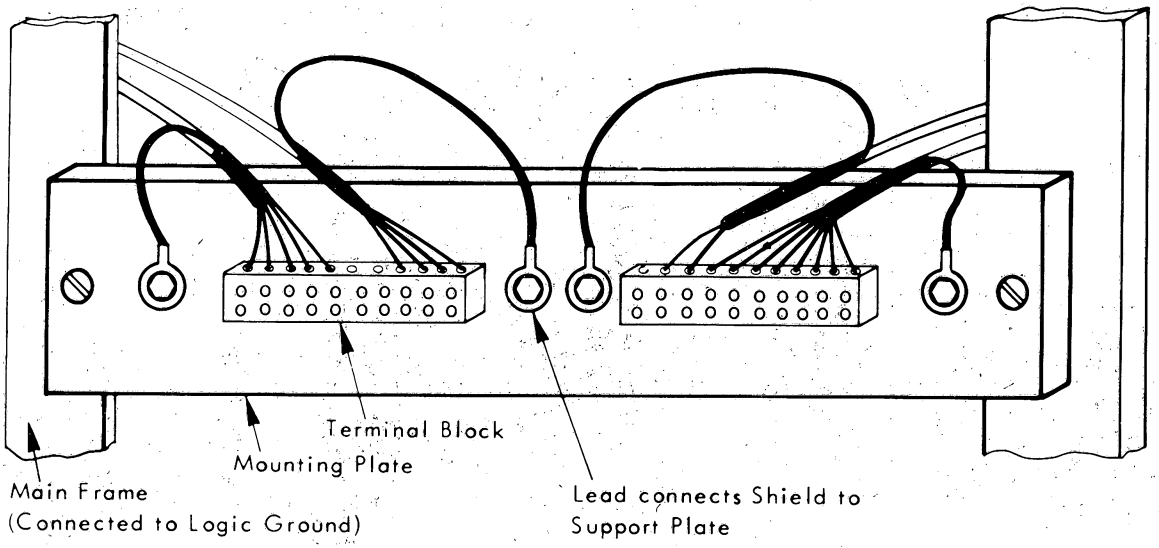


Figure 4.9 EXAMPLE USING TERMINAL BLOCKS

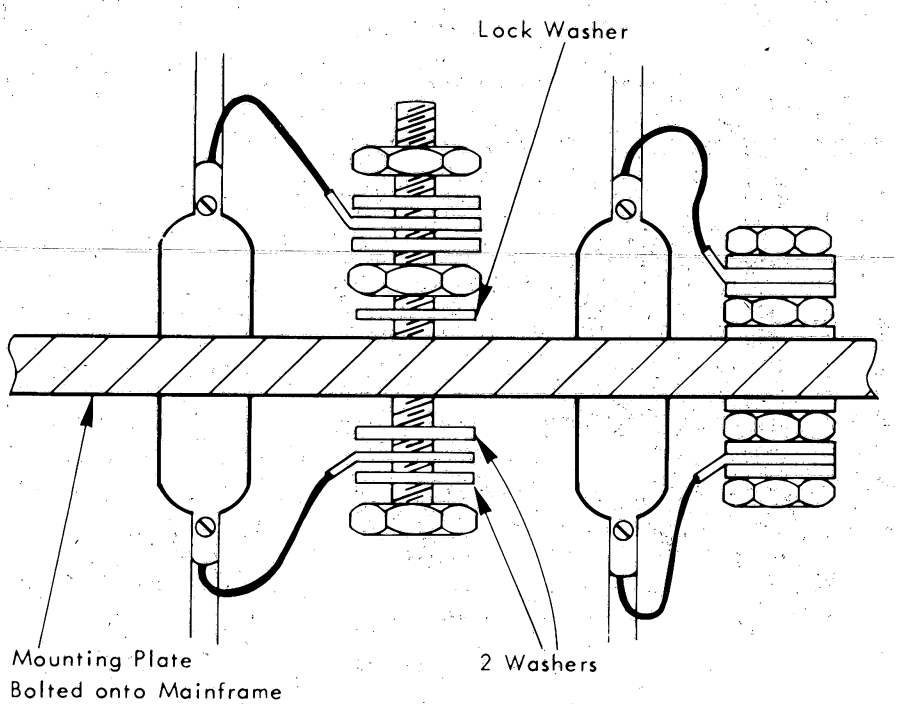


Figure 4.10 EXAMPLE USING CONNECTORS (TOP VIEW)

4.4.8 GROUND LEADS TO DEVICES

The following illustrations show how a ground lead is connected at some of the peripheral devices:

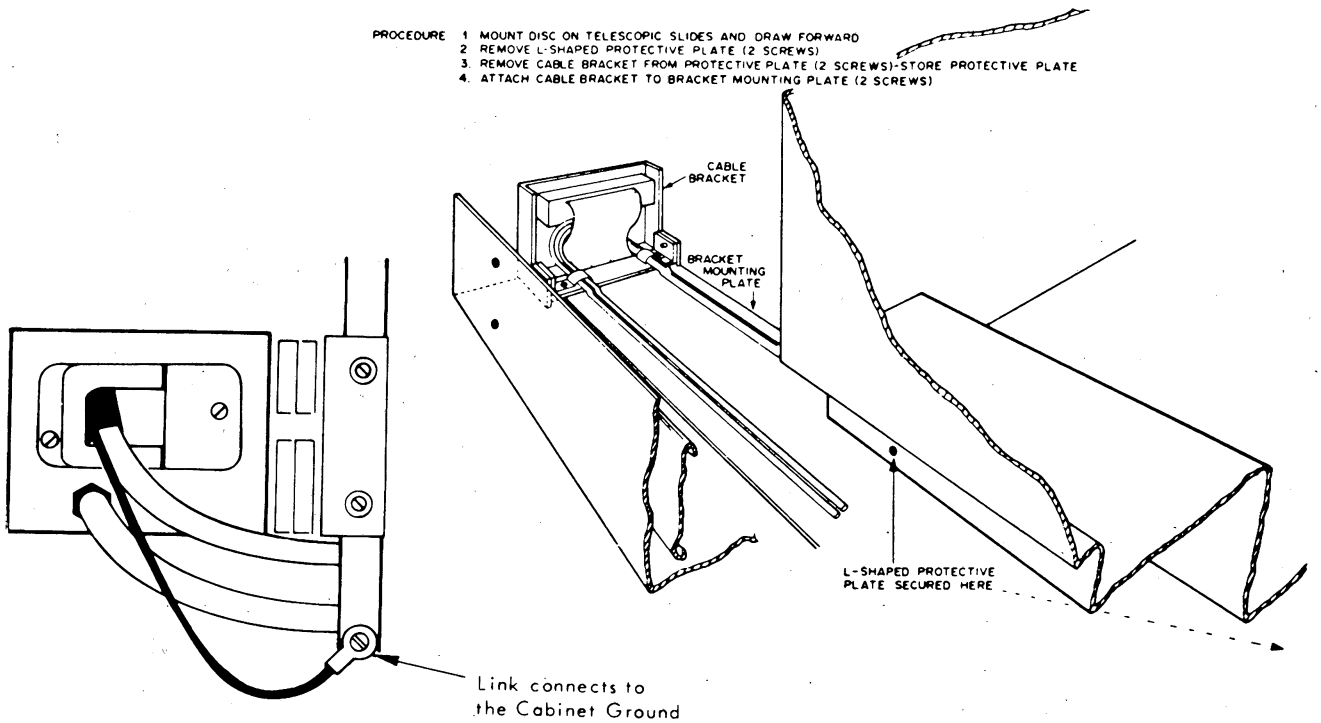


Figure 4.11a GROUND LEAD P824-012/014 (CARTRIDGE DISC DRIVE)

Figure 4.11b MOUNTING THE P824-012/014 (CARTRIDGE DISC DRIVE)

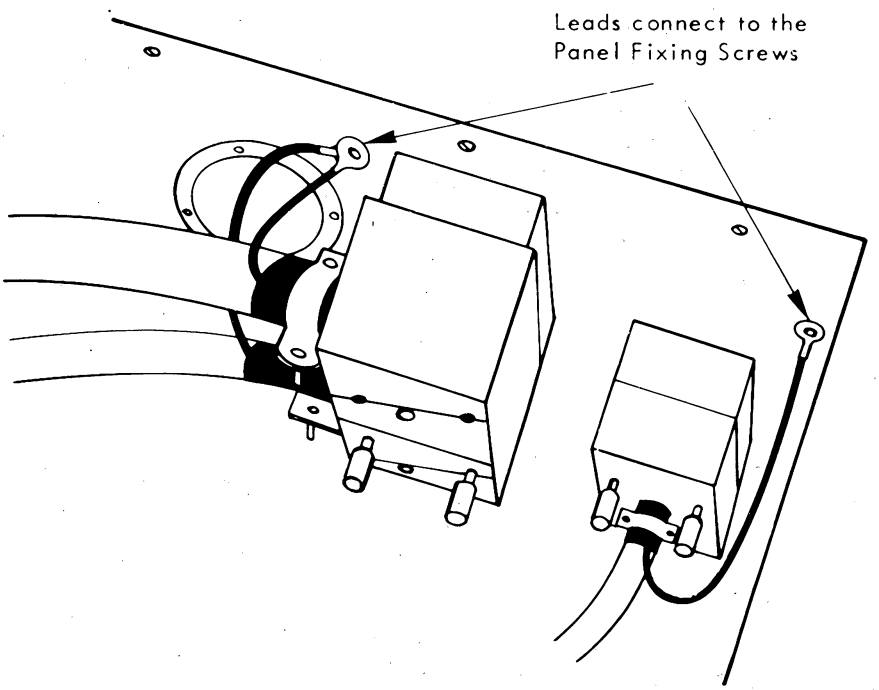


Figure 4.12 GROUND LEAD - P825-008 (STORAGE MODULE DISC DRIVE)

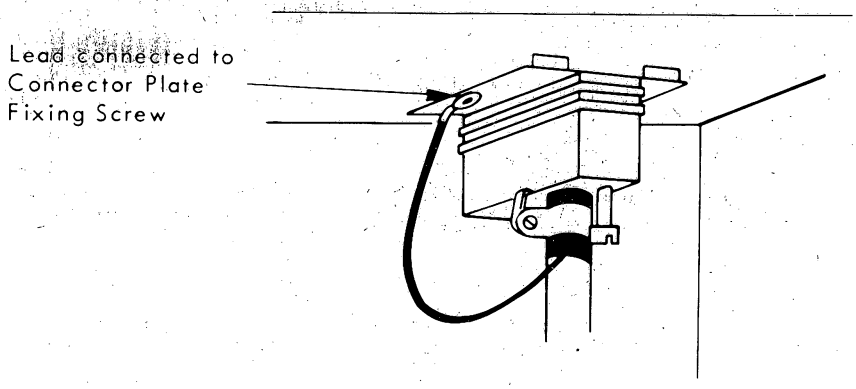


Figure 4.13 GROUND LEAD - P809-002/004 (LINE PRINTER)

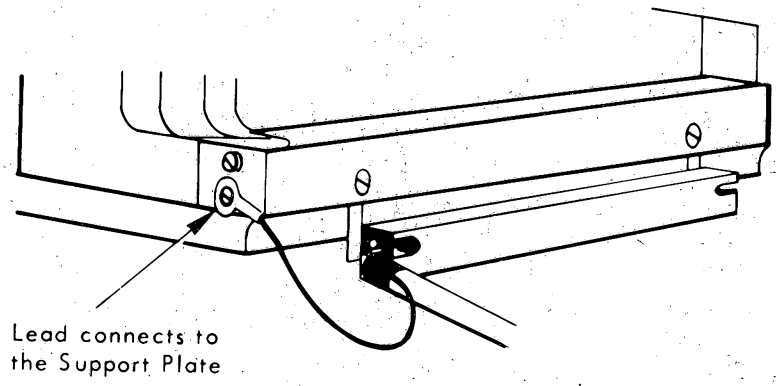


Figure 4.14 GROUND LEAD - P801-802 (PAPER TAPE READER)

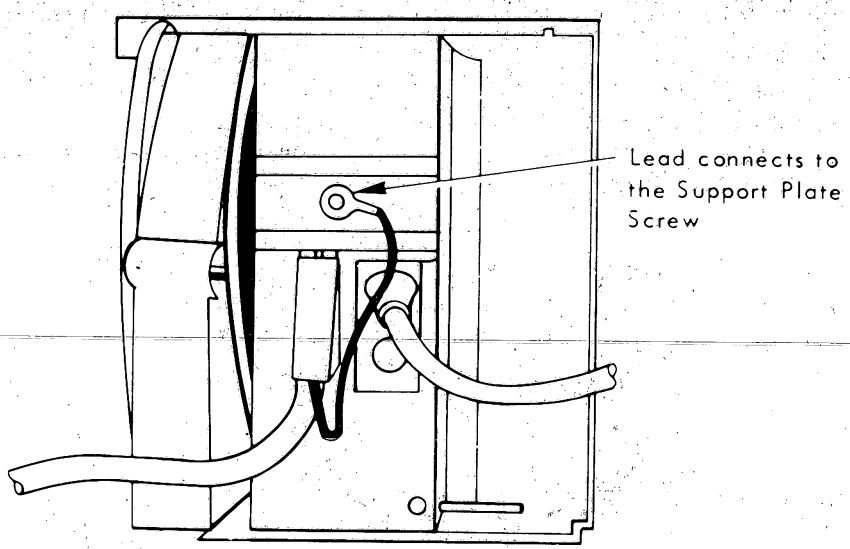


Figure 4.15 GROUND LEAD - P803/804 (PAPER TAPE PUNCH)

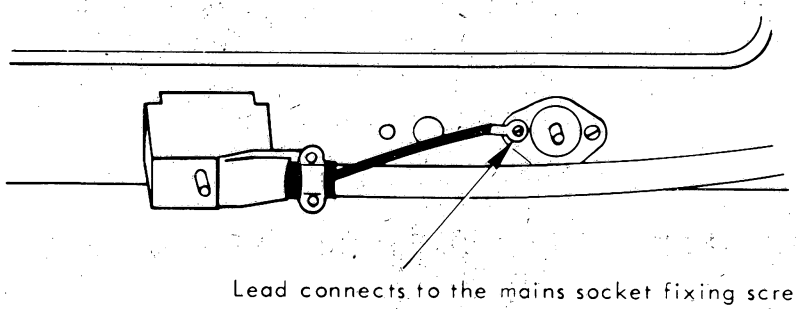


Figure 4.16 GROUND LEAD - P806/102 (CARD READER)

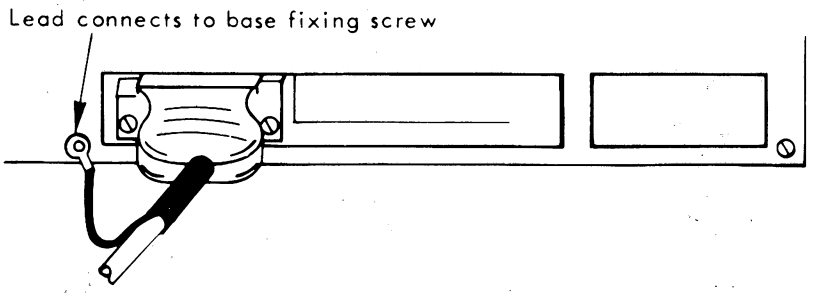


Figure 4.17 GROUND LEAD - P817 (VIDEO DISPLAY UNIT)

V24 Interface - At the device a tapped hole near the connector should be used to attach the lead.

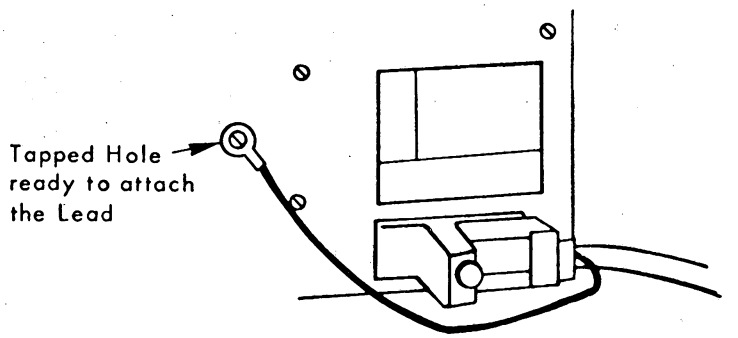


Figure 4.18 GROUND LEAD - P842 (PER3100)

Current Loop Interface - At the device when using the extension cable the connection between the Molex connector pin 6 and the ASR mechancal ground is made with the cable shielding. Note that under no circumstances the Molex connectors must be situated outside the ASR base.

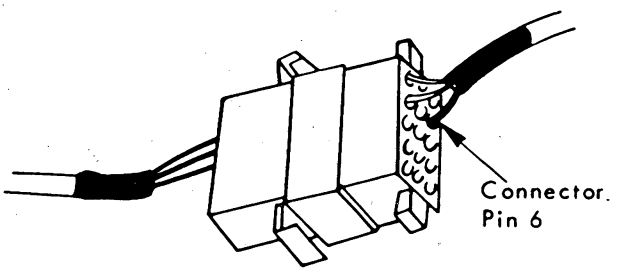


Figure 4.19 CURRENT LOOP INTERFACE CONNECTION

Remote Control Cables

Cabinet side - The shielding is connected to the central pin of the Molex connector.

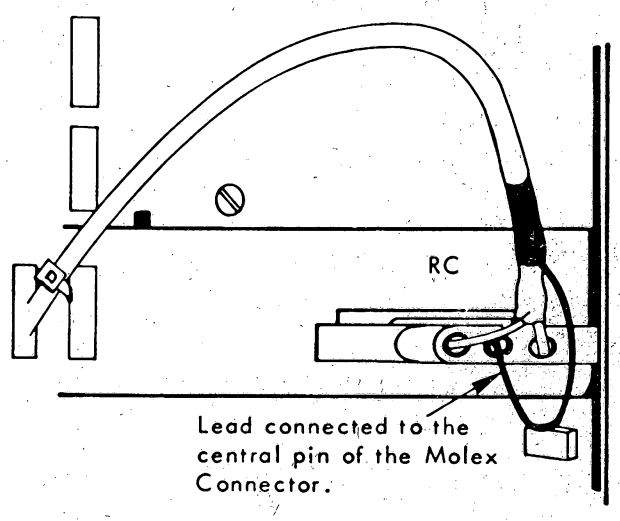


Figure 4.20a REMOTE CONTROL CABLE - CABINET SIDE

Connection at the Cabinet Terminal Box - When connecting the shielding of two cables at the Terminal Box, connect to the same terminal to ensure good continuity.

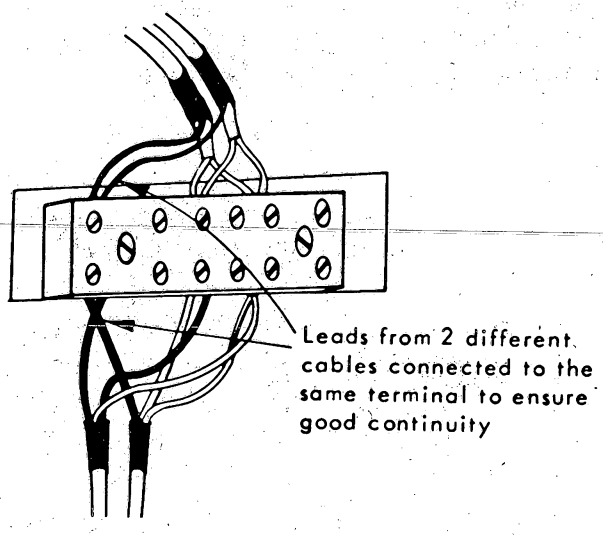


Figure 4.20b REMOTE CONTROL CABLE - CABINET TERMINAL BOX SIDE

Break Cables

At Extension Rack

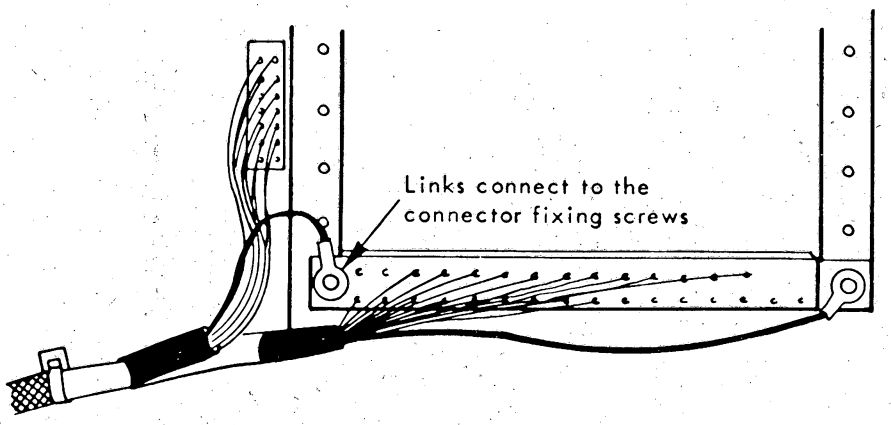


Figure 4.21 BREAK CABLE EXTENSION RACK

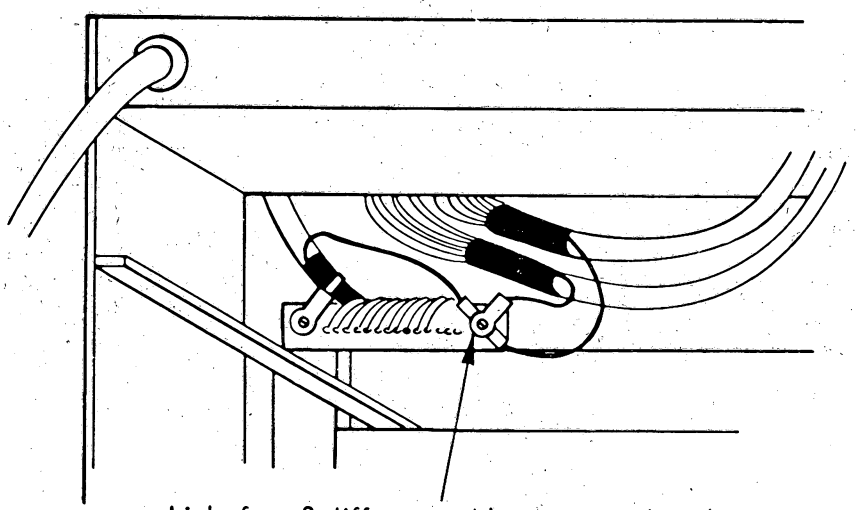


Figure 4.22 BREAK CABLE CASSETTE RACK

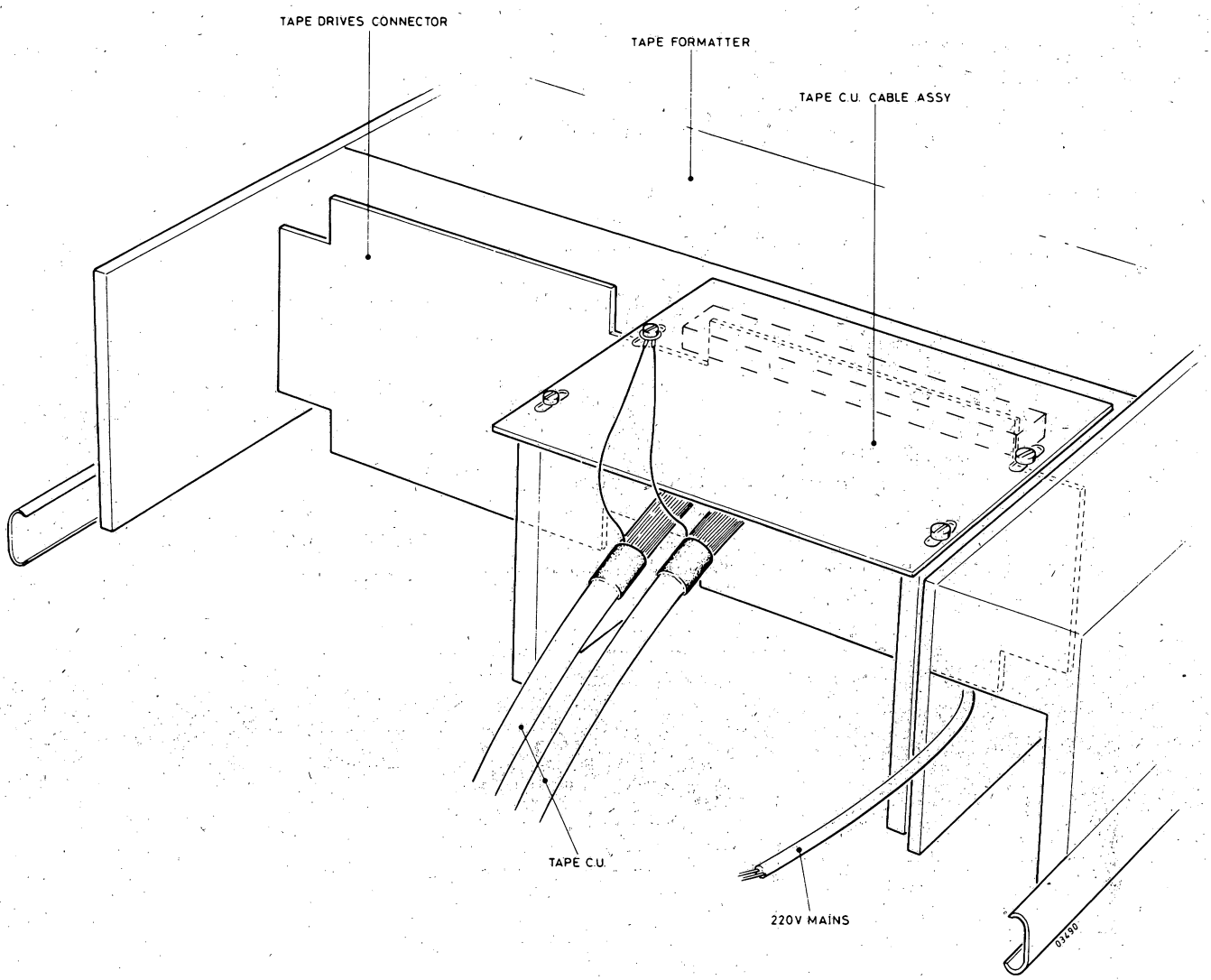


Figure 4.23 CABLE - TAPE FORMATTER

4.5 INSTALLATION SCHEDULE

You receive:

- pre-wired cabinet
- CPU-box with cards
- devices with cables
- documentation)
- testprogram) to be ordered separately

To be done:

- mount boxes in cabinets according received drawings
- connect remote control, breaks and device cables
- set straps on cards/devices for:
  - interrupt levels and device addresses
  - transfer speed, parity etc.
- connect mains cable
- run testprograms
- fil in the evaluation-form

Note: Normally the system is tested before delivery and so straps and connections are put in a proper working position.

4.6 CONNECTOR DETAILS FOR PRINTED CIRCUIT BOARDS

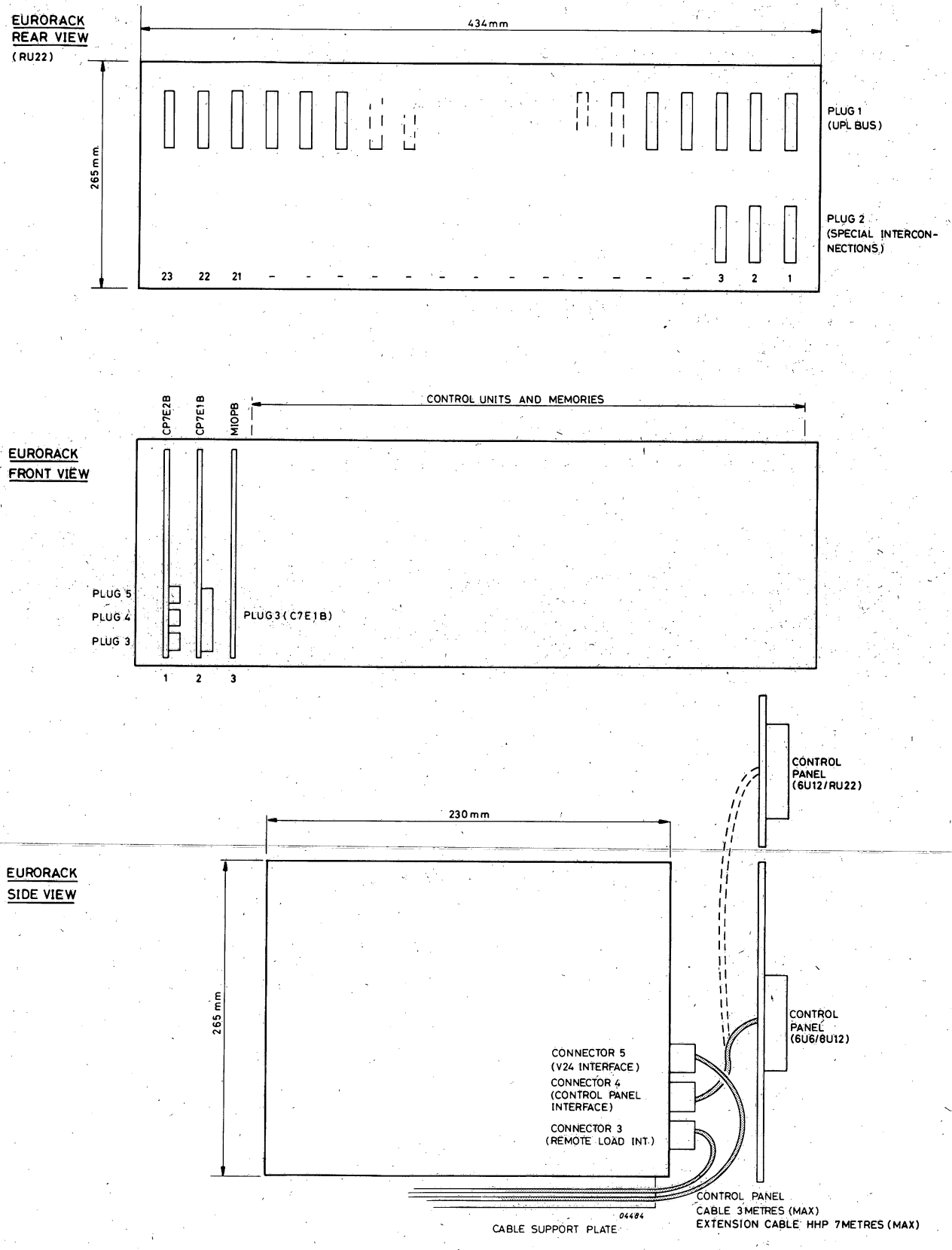


Figure 4.24 EURORACK

When the P857E configuration is being assembled the following rules must be taken into account.

. Cards C7E2, C7E1 and MIOP must be in rack position 1, 2 and 3 respectively.
. Other Masters follow in order of their system priority, determined by links OKO and OKI.
. Card MIOP contains 2 IOP's IOPA and IOPB. IOPA must always have a higher priority than IOPB (determined by links OKOA/B and OKIA/B).
. Control Unit addresses for connection with MIOP less than or equal to /F, without MIOP connection any address may be used.
. The UPL Bus must not be extended out of the basic Eurorack without the signals being terminated.

Figure 4.25 shows the system of pinning and numbering for card C7E2. In general the same principle applies for all double EURO-CARDS Plug 1 and 2.

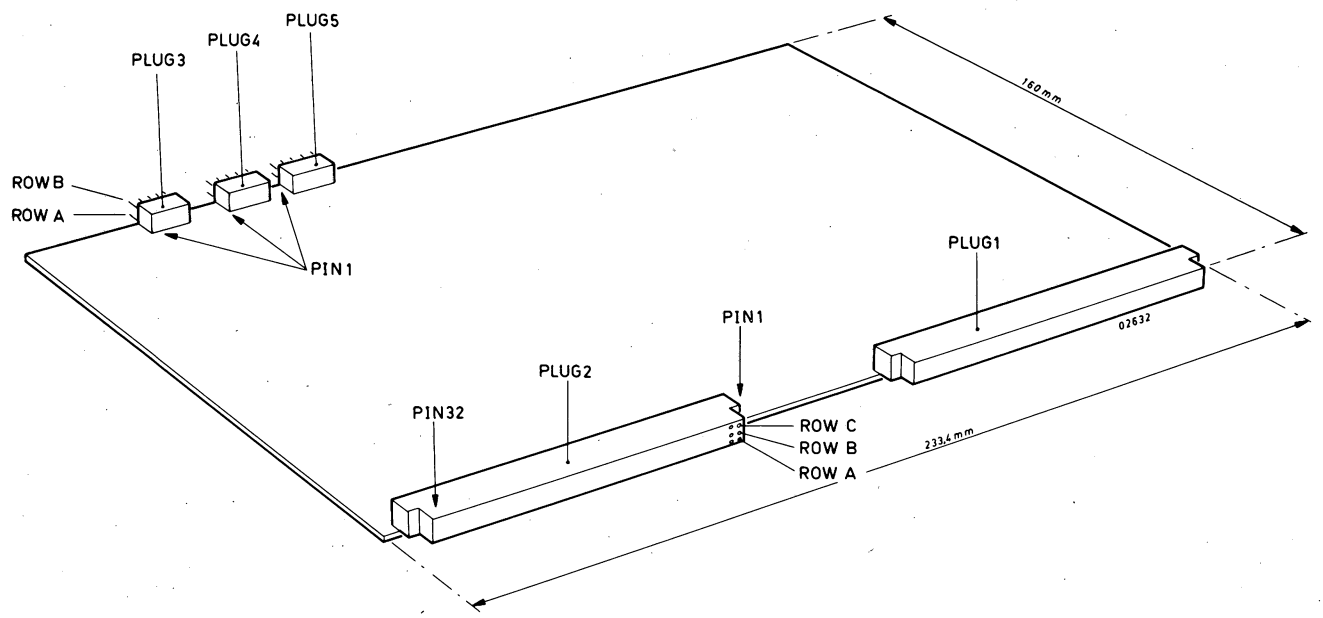
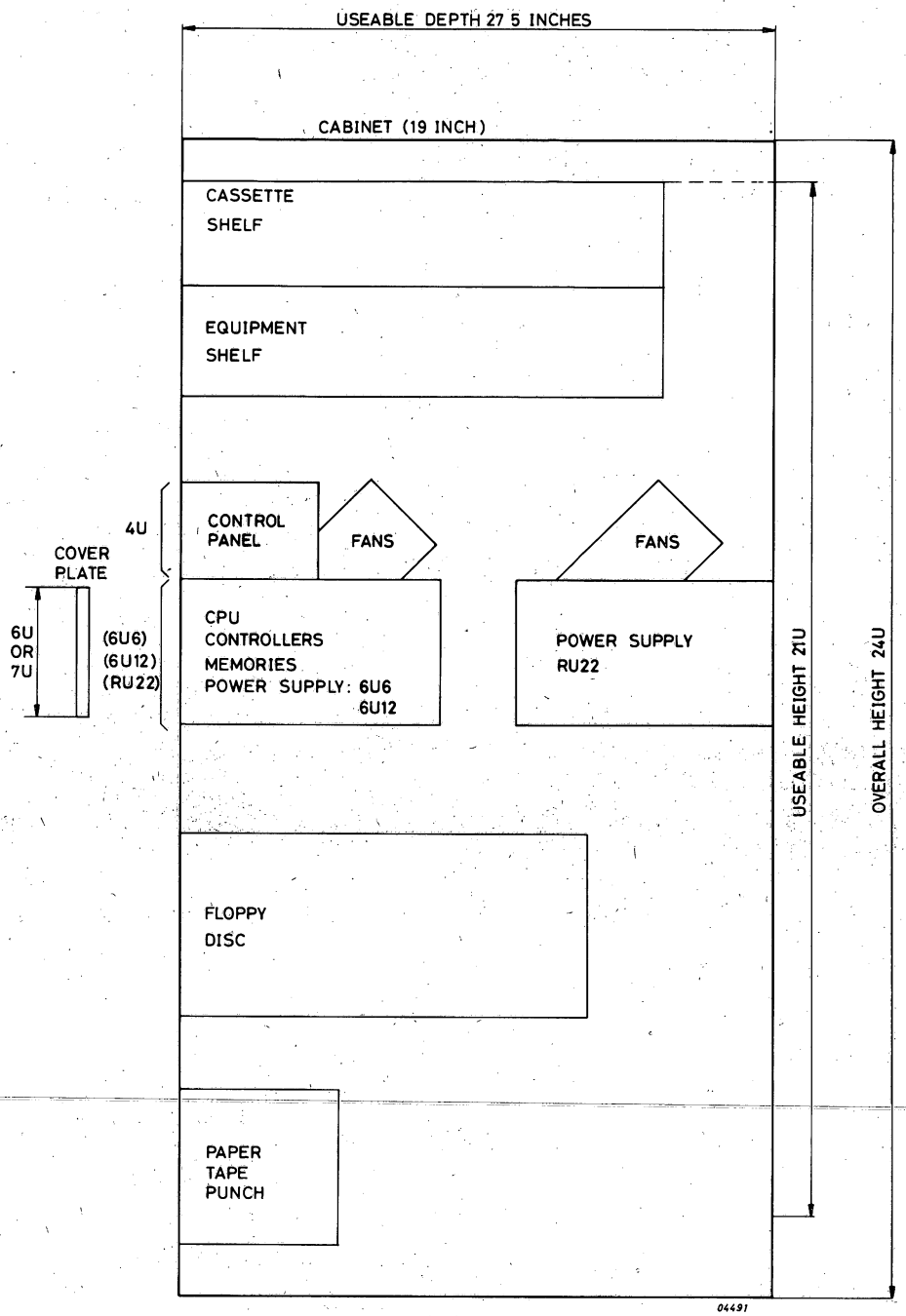


Figure 4.25 EUROCARD FORMAT (C7E2)



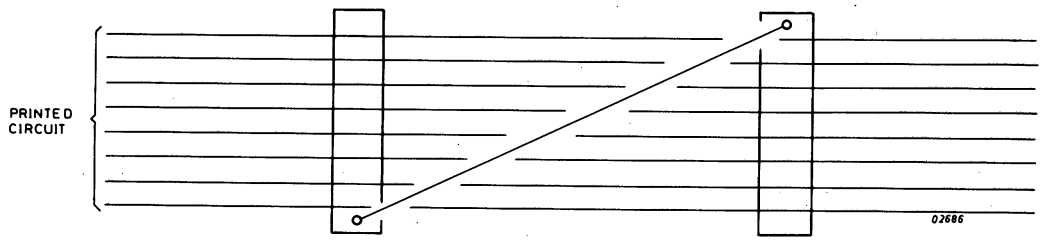
Notes: 1) 6U6 rack (P853) : Control panel and key switch in 6U6 rack
2) 6U12 rack (P853/4): Control panel if necessary in 4U cover-plate
Key switch in 6U12 rack
3) RU22 rack (P854) : Control panel and key switch in 4U cover-plate.
Fan assy's on both logic rack and separate power rack.

Figure 4.26 EXAMPLE OF A CABINET CONFIGURATION

4.8 INTERCONNECTION

The following instructions are only intended to highlight the important aspects of installing this system.

- Insert the Eurorack into the front of the cabinet and screw into position.
- Ensure that the mains are connected in accordance with the specification (this may differ depending upon the country of installation.
- Ensure that the Grounding Rules are observed.
- Check the card links before inserting cards into the Eurorack.
- Ensure that the cables between Control Units and Devices are firmly secured and that the screens of these cables are connected in accordance with the Grounding Rules.
- Interrupts and Breaks must be wired so that they run across the printed circuit wires and NOT parallel to them (see below).



WIRED CONNECTION RUNNING ACROSS THE PRINTED CIRCUIT

STRAP SETTINGS (SEE CHAPTER 8)

There are straps fitted to all 3 cards but only C7E2B houses the straps that are selectable by the user:

- IPL links to select the IPL and program loading device for remote and/or auto IPL.
- CT133 link.
- Speed Selection Links for the V24 peripheral interface. All cards must be checked to ensure that the workshop test links are in position.

Interrupt and Break wiring can be found in the CPU chapters.

12NC Code	CONNECTION	Length	Reference	
			Table	Figure
5111 199 6128x	P857E - PER 3100	7.5m		8.7
6310x	ASCU4Z - Modem Panel (CL)			12.4
6317x	MDDZ - 3 or 4 x X1250			17.1
6388x	CRLPZ - Line Printer (new)		20.2	
6455x	PRO16 - Program Tool			10.4
6471x	MDDZ - 1 or 2 x X1250			17.1
6473x	Modem Panel - PER 3100 (V24)			
6476x	CDDZ - X1215/16	7.5m	18.3	
6477x	CDDZ - X1215/16	3.5	18.3	
6540x	P857E - P817 (V24)	5m		8.7
6541x	P857E - Front Panel	3m		8.6
6617x	Modem Panel - P817 (CL)			
6770x	Front Panel - HHP	3m		8.6
6772x	Front Panel - HHP	7m		8.6
6785x	ASCU4Z - PER3100 (V24)			12.3
6786x	ASCU4Z - P817 (V24)			12.3
6804x	ASCU4Z - Open End (CL)			12.4
6805x	ASCU4Z - PER3100 (CL)			12.4
6908x	Modem Panel - P817 (V24)		13.2	
6909x	SCUZ - P817 (CL)		13.4	
6911x	SCUZ - P817 (V24)	10m	22.2/23.1	
6956x	SALCUZ - V24			
7003x	CRLPZ - Line Printer (old)	5m	20.2	
7004x	CRLPZ - Card-Reader	7.5m	20.1	
7102x	FLDZ/FIMZ - 3 or 4x Floppy drive		15.1/16.3	15.2/16.3
7103x	FLDZ/FIMZ - 1 or 2x Floppy drive		15.1/16.3	15.2/16.3
7199x	TUGP - Extension Box (Break)		14.3	
7206x	MTCU - Formatter		19.1/2	19.1
7242x	SCUZ - PER3100 (CL)		13.2	
7243x	SCUZ - PER3100 (V24)		13.4	
7247x	TRPZ - Tape - Reader	3m	21.1	21.2
7248x	TRPZ - Tape - Punch	3m	21.2	
7279x	SALCUZ - V24		22.2	
511 199 7579x	HLCUZ - V24		23.1	

Table 4.5 LIST OF CABLES

Note: CL = Current Loop interface
V24 = V24 interface

4.9 TRANSLATOR UPL BUS TO GP BUS FOR MAGNETIC TAPE CU

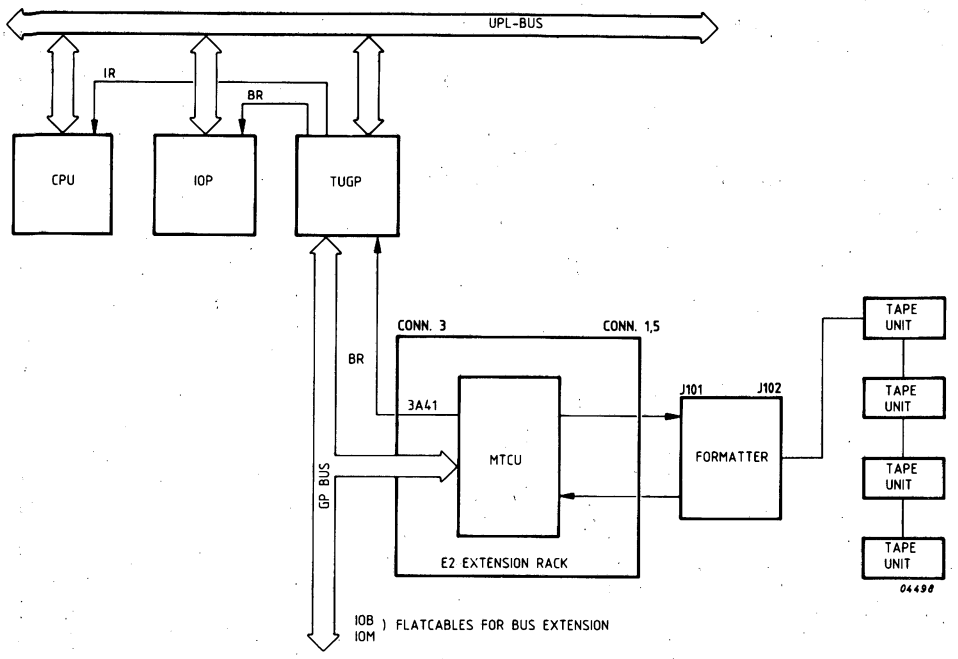


Figure 4.27 USE OF TUGP FOR MTCU

5 TROUBLE SHOOTING

SECTION	5.1	GENERAL	PAGE 5-2
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	5.3	CHECK INTERRUPTS	5-3
	5.4	CHECK DEVICE ADDRESS	5-4
	5.5	TESTPROGRAMS	5-5

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5.1 GENERAL

A number of short routine (simple programs) have been added to the various chapters. They can be used if official testprograms give problems or when you want to test only the basic functions of each device or Control Unit.

NAME	CHAPTER	DESCRIPTION
LINE	8,13	Output on Console Typewriter (CTW), or display - V24 CU
ECHO	8,13	Input, Output on Console Typewriter, or display - V24 CU
MEM	10	Memory test, 32K maximum.
DUMP	10	Memory dump on CTW, 32K maximum.
MMU2	11	MMU test
ASCU	12	Loop test (output to input check)
ASCU2	12	Input, Output test (input to memory, memory to output)
FDDRT	15	Write and Write-Key commands on FLDZ
FDDRD	15	Read and Read-Key commands on FLDZ
FDDRWD	15	Write and Read on FLDZ
FLTST	15	Write, Read test of Discette on FLDZ
ADJF1M	16	Adjust or Check 1M drive on F1MZ
F1SEEK	16	Seek test F1MZ
F1LOOP	16	Write and Read on F1MZ
MDSEEK	17	Seek test MDD-FXD
MDLOOP	17	Write and Read on MDD-FXD
SEEK	18	Adjust 2.5M or 5M drives X1215/16 on CDDZ
DISCTS	18	Write and Read on CDDZ via IOP
DKPROG	18	Write and Read on CDDZ via Programmed Channel.
WRITE	19	Write Test Pattern on Tape
READ	19	Read Test Pattern from Tape and compare
MTTEST	19	Write and Read all ones on MTCU
LINELP	20	Output on Lineprinter via PC
LPIOP	20	Output on Lineprinter via IOP
CPROGR	20	Read 80 column card into memory via PC
CRTEST	20	Read 80 column card into memory via IOP
PTR	21	Read 80 characters from papertape
PUNCH	21	Punch 80 characters on papertape
SALCUT	22	Output test (output to CTW display or oscilloscope)
SALCLA	22	Loop test (output to input and check), asynchronous
SALCLS	22	Loop test (output to input and check) synchronous
HLCUT	23	Output test (output to oscilloscope, data = /FC)
HLCUL	23	Loop test (output to input and check)

Table 5.1 SHORT ROUTINES

5.2 CORRECTIVE MAINTENANCE

The cause of the trouble may be difficult to find because of the great variety, such as:

- Intermittent failures
- Temperature dependant failures
- Software errors
- Design errors (timing e.g.)
- Mains causing problems
- Crosstalk, induction etc.

Philosophy: Card exchange (repair in factory or workshop of the National Organisation).

1. Use your eyes, ears, nose and mouth - ask operator for symptoms.
2. Run microdiagnostic (if possible)
3. Run testprograms: CPU-MEM-I/O devices - terminals
4. Check all strap settings and board locations

If not found:

5. Take out all boards you do not need for the test you are running. Note: PSU must have a min. load of 15%.
6. Load in a few instructions, via hand held panel (if available) with which you can test (instruction by instruction) the system.
   Think of: - straps, U-links on cards and backpanel
   - weak mechanics: fuses, switches, cables, lamps.
7. After repair: run testprograms.

Note: Switch off power before you exchange cards. Bus-transceivers can be blown, which may block the bus.

5.3 CHECK INTERRUPTS

To check if interrupts come in and to verify which level they are, the following small procedures are supplied.
Note: On HHP the switches RTC and LOCK must be off.

Power Failure (level Ø)

1. Depress MCL
2. Connect the bus signal PWFN to ground
3. Depress INST
4. Depress RST
   The 6 ms bits of the displayed word must be zero (i.e. word /ØØ..,/Ø1..,/Ø2.. or /Ø3..)

LKM (level 1)

1. Depress MCL
2. Fill mem address /1ØØ with /28Ø4 (=LKM)
3. Set program counter to /1ØØ
4. Depress INST
5. Depress RST
   The 6 ms bits of the displayed wod must be /Ø1 (i.e. word /Ø4..,/Ø5..,/Ø6.. or /Ø7..)

RTC (level 2)

1. Depress MCL
2. Switch RTC on (on both SOP and HHP)
3. Switch RTC off
4. Depress INST
5. Depress RST
   The 6 ms bits of the displayed word must be /Ø2 (i.e. word /Ø8..,/Ø9..,/ØA.. or /ØB..)

Control Panel Interrupt (level 3)

1. Depress MCL
2. Depress INT
3. Depress INST
4. Depress RST
   The 6 ms bits of the displayed word must be /Ø3 (i.e. word /ØC..,/ØD..,/ØE.. or /ØF..)

I/O Interrupts

- Disc, tape, floppy

1. Depress MCL
2. Load disc pack/tape/diskette
   A ready-interrupt will be generated.
3. Depress INST
4. Depress RST
   The 6 ms bits of the displayed word must contain the expected level. For floppy level 15 = /F the PSW starts with /3C..,/3D..,/3E.. or /3F..

- From other devices

From the short programs on the following pages, key in the program until an INR or OTR instruction is expected. The inhibit instruction (INH) must be replaced by a no-op instruction (=/5700). Execute the program inst-by-inst until I/O or a status interrupt is expected. The program counter displayed on the HHP will show the jump. Now depress RST. The 6 ms bits of the PSW indicate the interrupt level.

5.4 CHECK DEVICE ADDRESS

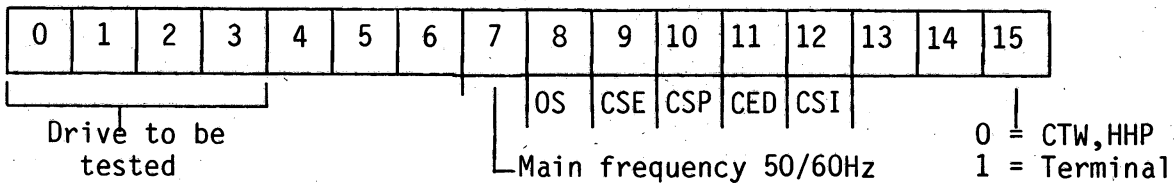
To check the device address whether it is available or not, use the following procedure:

1. Fill mem address /1ØØ with CIO halt:
   'Ø1ØØ ØØØ1 1Ø.. ....', where the 6 ls bits contain the device address.
2. Set program counter to /1ØØ
3. Depress MCL, INST
4. Depress RST
   Bit 6 and 7 of the displayed word must be 'Ø Ø' (i.e. word /.Ø..,/.4..,/.8.. or /.C..)
   Bit 6 and 7: '1 1' = address unknown
   'Ø 1' = not accepted
   'Ø Ø' = accepted

5.5 TEST PROGRAMS

- Program names starting with B.. are original P8ØØ versions. System parameters can be changed by Hand Held Panel. Console Type-Writer may be used.
- Program names starting with T.. are adapted program versions for PTS 8000. In this case, the system parameters can be changed on a terminal keyboard. Register A9 bit 15 = Ø indicates the program that output is on CTW (or no output),
  15 = 1 indicates the program that output is on a terminal.
- As only loading procedure and initial parameter setting are different, the P800 testprogram description is also used for PTS 8000 programs.

Testprogram Control - Selection with register A9.



Bit 0 = 1 Drive 0
Bit 1 = 1 Drive 1
Bit 2 = 1 Drive 2
Bit 3 = 1 Drive 3

- "One Shot" (OS)
  Bit 08 = 1: Stop in /5E0 (hexa) after the running of each check, before going to the next one. All there is to be done is depress the RUN button to carry on. PTS systems: depress SOP switch 9.

- "Clear Stop on Error" (CSE)
  Bit 09 = 1: Suppress the stop in /5F0 (hexa) in case of an error.

- "Clear Stop on Program" (CSP)
  Bit 10 = 1: Suppress the stop in /700 (hexa) after the program has been executed (loop again on test).

- "Clear Edition" (CED)
  Bit 11 = 1: Suppress the printing out of error and information messages:
  CSI at 0: stop in /5E0: Information code in A1.
  CSE at 0: stop in /5F0: Error code in A1.

- "Clear Stop on Information" (CSI)
  Bit 12 = 1: Suppress the stop in /5E0 (hexa).

- Main frequency
  Bit 7 = 0: 50Hz
  Bit 7 = 1: 60Hz
  In case of 50Hz, it is possible to set bit 7=1 that will increase by 20% all delays. This permits to determine if the problem is due to a critical timing or a real fault.

To run the testprograms refer to Short Description Testprograms in each chapter.

6 CONTROL PANELS

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6.1 INTRODUCTION P843-510/FRCP (FIGURE 6.1)

The FRCP provides the controls and indicators that enable a user to operate and monitor the system. The pushbuttons are in two groups: the left-side group is used to select system functions; the right-side group to select hexadecimal address and data digits. The left-side indicator is mainly used to display memory and register addresses, the right-side indicator to display memory and register data. The FRCP is intended for P854 and P859 computer systems.

6.1.1 PHYSICAL DESCRIPTION

The FRCP is available in two electronically identical but physically different versions:

- FRCP used in M4 Racks (P859) 12NC = 5111 199 6630X
- FRCP used with 6U cover plate (6U6 racks) 12NC = 5111 199 6629X
- FRCP used with 4U cover plate (6U12, RU22 racks) (X = modification level)

Note: Before a FRCP is disconnected from the system, the LOCK button must be on.

6.1.2 TECHNICAL DATA

PERFORMANCE DATA

Serial Data Interface: V24/28: Transmission Rate = 4.8K baud
Logic Levels : logical 0 = +12V
: logical 1 = -12V

POWER REQUIREMENTS

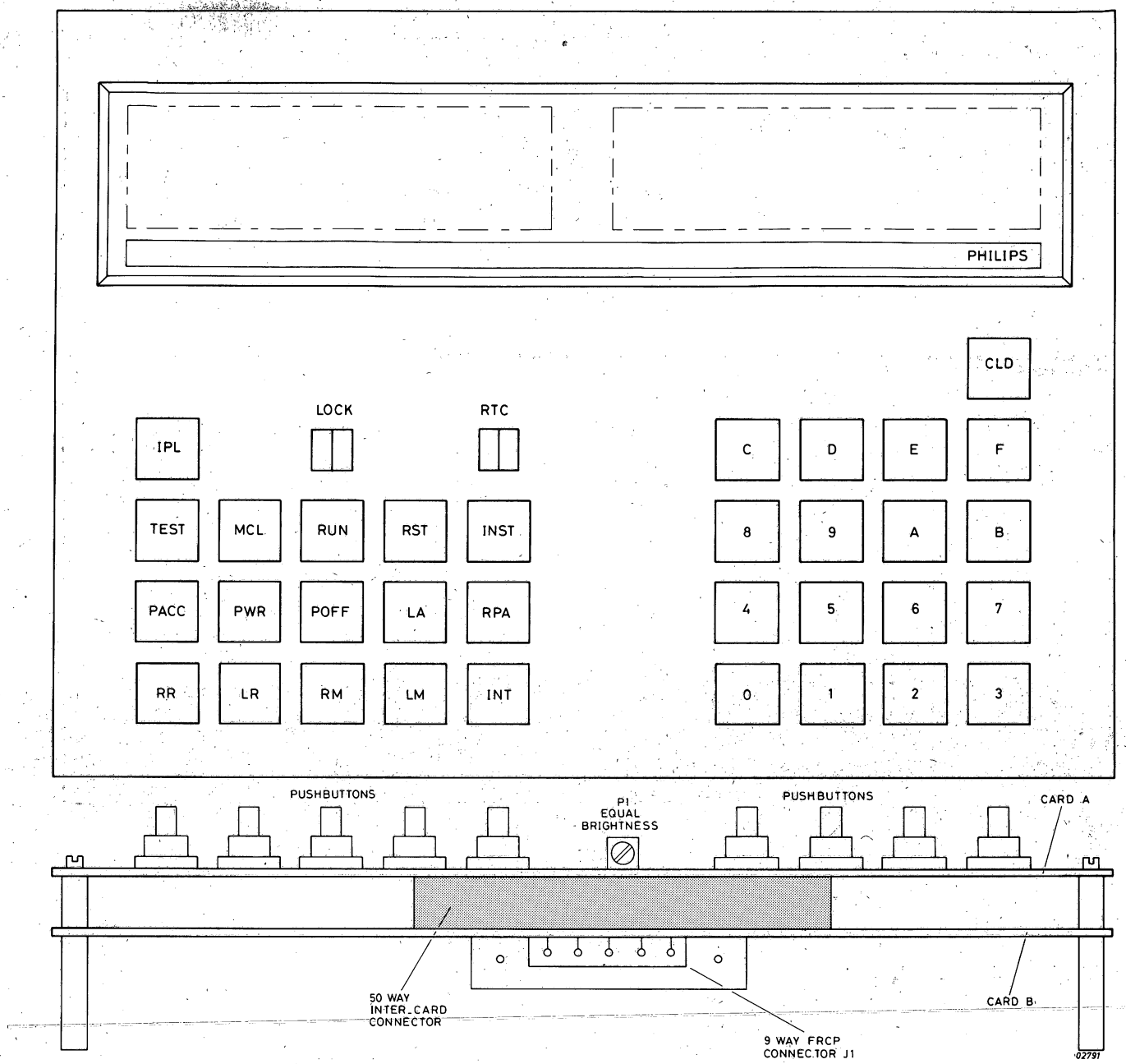
Voltage	: +5V ± 0.25V	+12V ± 1.2V	-12V ±1.2V
Current (max.)	: 800mA	150mA	20mA

PHYSICAL DIMENSIONS

local version = 180mm X 130mm x 55mm
remote version = (t.b.f.)

6.2 INTERFACE CONNECTOR FRCP

Pin No.	Signal	Function
J1-1	LOCK	When LOCK = 1, FRCP is inhibited except for INT
2	SDMP	Serial Data Master to Panel
3	OV(GND)	
4	+5V	(for remote version, down to +4V (V_{LINE})
5	+12V	Logic level 0 of serial data
6	SDPM	Serial Data Panel to Master
7	RTCE	Real Time Clock Enable (active at "1")
8	RESETN	Reset Not
9	-12V	Logic level 1 of serial data



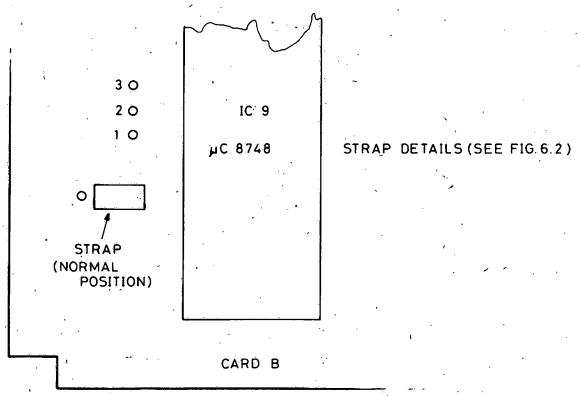


Figure 6.1 FRCP DETAILS

6.3 TRANSMISSION CODES FRCP

SWITCH SELECTION:	HEXADECIMAL CODE:
0 to F	Address: / Bx Bx Bx Bx Bx Bx (leading zeros are not keyed in) Reg Addr. / 3x Data: / 3x 3x 3x 3x (leading zeros are not keyed in) where x is the selected hex. digit in the range 0 to F.
MCL	/40
LR	/41
RR	/42
RST	/43
IPL	/44
LM(1)	/45
LM(2)	/55
INT	/46
RM(1)	/47
RM(2)	/57
LA	/48
INST	/49
RPA	/4A
RUN	/4B
PACC	/4C
PWR	/4D
POFF	/4F
TEST	/4E
Serial Data Panel-to-Master Codes	

Table 6.1 SDPM CODES FRCP

FUNCTION NAME	FUNCTION	HEXADECIMAL CODE
RUNZO	CPU mode changed from RUN to IDLE	/40
RUNZ1	CPU mode changed from IDLE to RUN	/41
TEST	Production testing only	/42

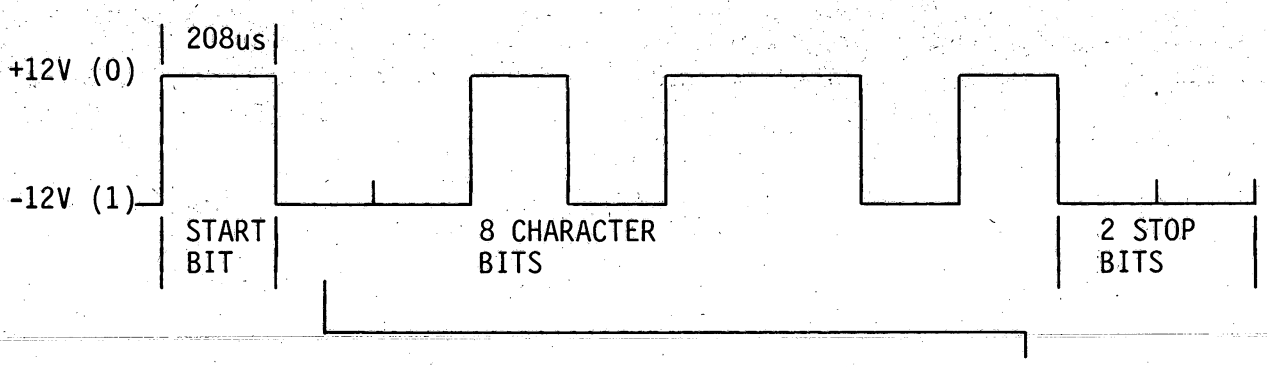
Serial Data Master-to-Panel Codes

Note: To distinguish between master-to-panel data and hand-entered data, the display of master -to-panel data is preceded by two small zeros e.g.: oo 1625.
When the preset stop-on-address function is operative, the display of master-to-panel data is preceded by 'P' and one small zero e.g.: Po 1625.

HEXADECIMAL CODE FORMAT

1 start bit, 8 character bits, 2 stop bits

EXAMPLE:



CHARACTER 'RUN' = $0100/1011_2$

= $4\ B_{16}$

Note that the least significant bit is transmitted first.

Table 6.2 SDMP CODES AND CODE FORMATS FRCP

6.4 FUNCTIONS FRCP (FIGURE 6.2)

The FRCP consists of a microcomputer and switch matrix which operate together to generate serial function and data codes for onward transmission to the CPU. The address and data displays can be energized with the appropriate information, via buffers, registers etc. The FRCP can also receive information from the CPU.

A 40KHz oscillator is used to derive an a.c. drive for the display filaments. The oscillator output is also used to derive a +24V d.c. supply, and a +5V supply (necessary if the line voltage of the remote version is less than +5V).

SWITCH	FUNCTION
0 to F	To select hexadecimal address and data digits.
LOCK	When this switch is pushed rightward, all FRCP functions except INT are inhibited. The automatic restarting facility is enabled.
RTCE	When this switch is pushed rightward, the system Real Time Clock is enabled.
CLD	Clears ADDRESS and DATA displays to all zeros.
IPL	Initial Program Loader: An initial bootstrap program that is located in a hardware read-only-memory is loaded into memory word locations 000 to 255.
TEST	When this switch is operated at the same time as the '0' switch and provided the system microdiagnostic routine is loaded, the CPU will execute the system microdiagnostic routine. When it is operated alone all the segments of the ADDRESS and DATA displays will be lit.
MCL	Master Clear: Clears or resets most hardware logic. Usually activates the bus CLEARN signal.
RUN	Sets the CPU to RUN mode and inhibits all FRCP functions except INST and INT. The word 'run' in small letters is displayed on the DATA display. If the Stop On Preset Address option is being used the letter 'P' will be displayed as the extreme right-hand character of the DATA display. The preset stop address will be displayed on the ADDRESS display.
RST	Read Status: The contents of the program status word are displayed on the DATA display.
INST	Instruction Step: Each time INST is pressed, the CPU performs the one instruction indicated by the program counter and then halts.
PACC	Preset Access: Stop when any memory operation accesses the address that was keyed in before selecting the PACC function.
PWR	Preset Write: Stop when a write memory operation accesses the address that was keyed in before selecting the PWR function.
POFF	Inhibit the preset-stop-on-address function.

Note: The preset-stop-on-address function is optional and is not available on some systems

Table 6.3 CONTROL PANEL SWITCHES FRCP

SWITCH	FUNCTION
LA	Load Address: When this switch is operated, the keyed-in address code is loaded into the Memory Address Register and will be displayed on the ADDRESS display. This address is incremented by successive RM or LM operations.
RPA	Read Preset Address: When this switch is operated, and provided the CPU is in IDLE mode, the preset address will be displayed on the ADDRESS display. When the CPU is in the RUN mode, the INST button should be pressed followed by the RPA button. The RUN button must be pressed to restart the program.
RR	Read Register: When this switch is operated, the keyed-in register no. is displayed on the ADDRESS display and the contents of the register is displayed on the DATA display.
LR	Load Register: When this switch is operated, the keyed-in data is displayed on the DATA display.
RM(1)	Read Memory: When this switch is operated with the '0' switch, the address pointed to by the program counter A0 is displayed on the ADDRESS display and the contents of the address is displayed on the DATA display.
RM(2)	Read Memory: When this switch is operated alone, the contents of the address pointed to by the Memory Address Register is displayed on the DATA display and the memory address +2 is displayed on the ADDRESS display. To read sequential memory locations RM is pushed as required.
LM(1)	Load Memory: When this switch is operated with the '0' switch, the address pointed to by the program counter A0 is displayed on the ADDRESS display and is loaded with the data that is displayed on the DATA display.
LM(2)	Load Memory: When this switch is operated alone, the memory address pointed to by the Memory Address Register and that is displayed on the ADDRESS display is loaded with the data that is displayed on the DATA display and the address is incremented by 2.
INT	Interrupt: When this switch is operated, the FRCP generates an operator's interrupt.
Note:	To distinguish between master-to-panel data and hand-entered data, the display of master-to-panel data is preceded by two small zeros e.g. 1625. When the preset-on-address function is operative, the display of master-to-panel data is preceded by 'P' and one small zero, e.g. P 1625.

Table 6.3 CONTROL PANEL SWITCHES FRCP (CONT'D)

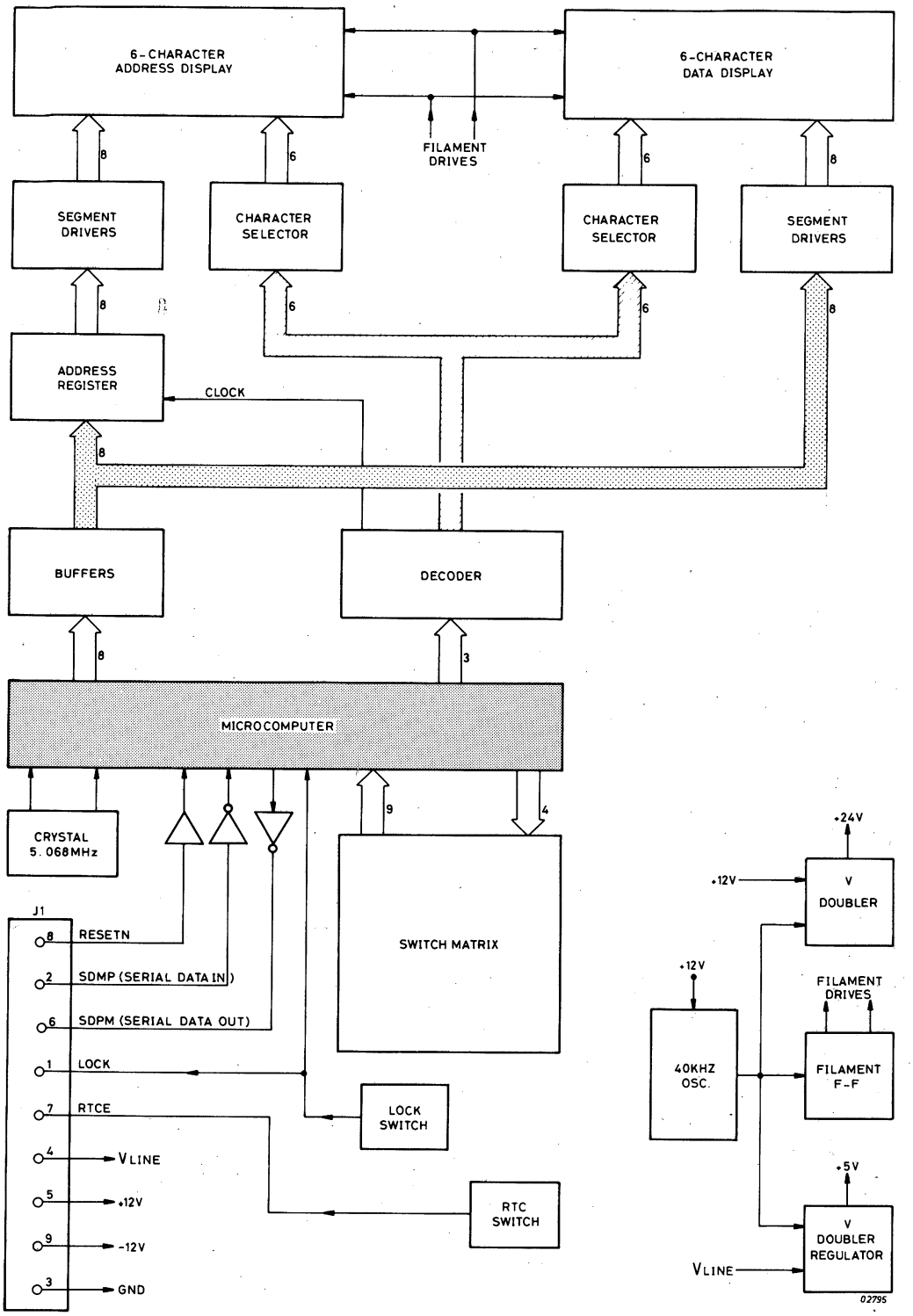
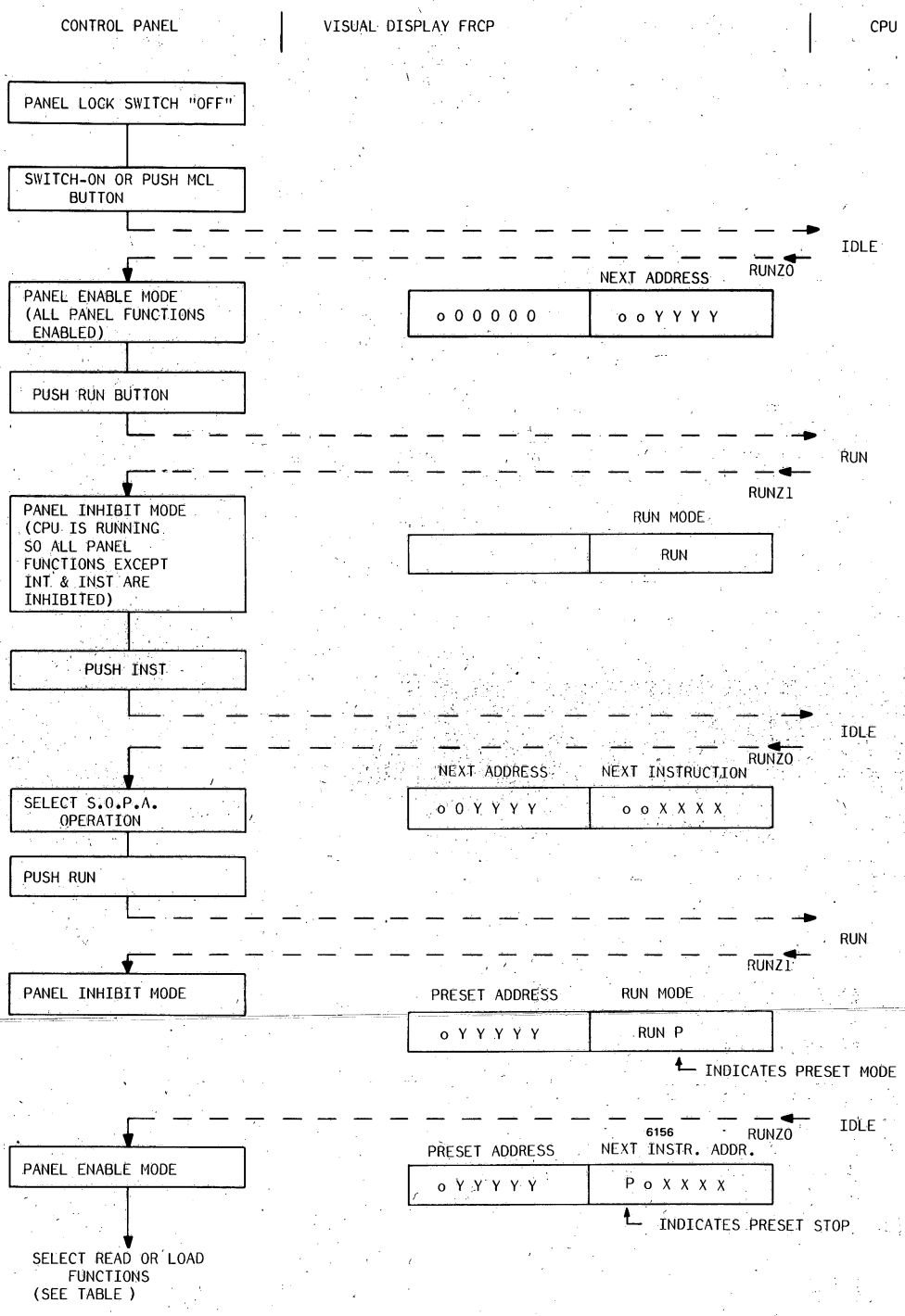


Figure 6.2 FRCP BLOCK DIAGRAM



NOTE: THE DOTTED LINES REPRESENT THE SERIAL DATA PATHS BETWEEN THE CPU AND CONTROL PANEL.

Figure 6.3 FRCP/P857E DIALOGUE

6.6 STOP ON PRESET ADDRESS PRINCIPLE

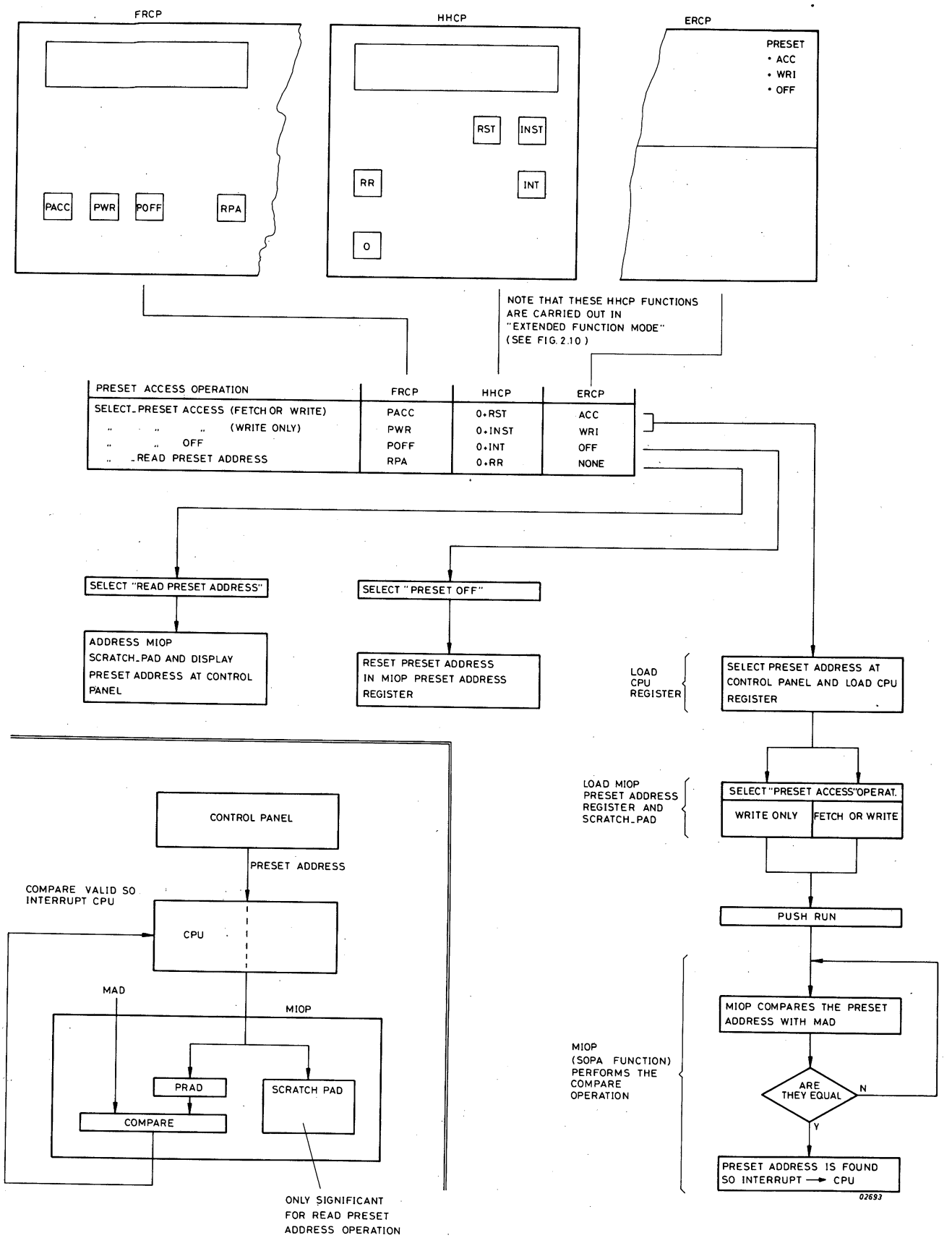


Figure 6.4 SOPA - PRINCIPLE OF OPERATION

6.7 INTRODUCTION P843-500/HHP (FIGURE 6.5)

The HHP is a hand held control panel enabling the user to communicate with the P853, P854 computer systems. The panel has similar facilities to the Full Control Panel. Data keys are code '0' - 'F' and the visual display shows 4 hexadecimal digits. Connection for some P800 configurations are shown in Figure 6.6. The panel is designed around an eight-bit microprocessor 8048 which performs all the major logic functions. These are:

. Reading the keyboard
. Displaying data
. Transmitting and receiving data or address and from the CPU

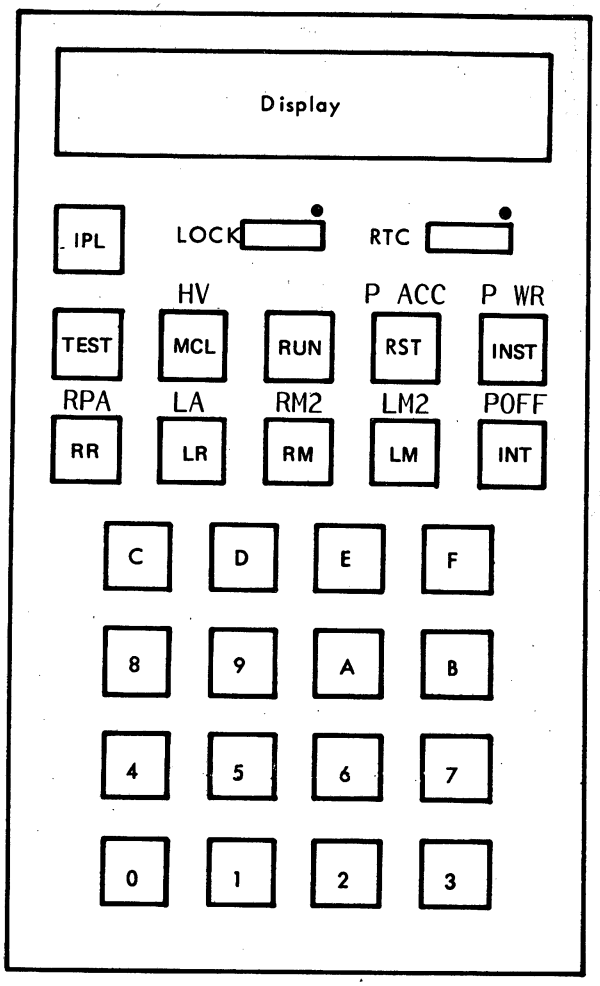
The asynchronous serial interface with the CPU complies with CCITT (V24) requirements. Successive characters of data/function are transmitted in the form: 1 start bit/8 data bits/2 stop bits.

SERIAL INTERFACE (V24/V28)

Bit serial data is input to or output from the HHP at +12/-12V. This is converted to or from +5V/0V by types 1489A input and 1488 output inverters compatible with the microprocessor (8251). Data transmission is 4800 bits/sec. The bit-serial data format for a single character is shown in figure 6.7. When no character is being exchanged, the line is in the 'one' state. Characters may be transferred end-to-end or may be separated by any amount of gap smaller than 1.5ms.

POWER REQUIREMENTS

See table 6.4



MCL	Master Clear	(MCL)	HV	High order digit visualisation
RTC	Enables Real Time Clock			
LOCK	Select Automatic Restart in case of power failure and lock all function buttons except INT.			
RUN	Start CPU			
INST	Execute next instruction only	(INST)	PWRITE	Preset Write
TEST	Test display	(TEST)	TEST	Initiate Diagnostic Test
RST	Read Program Statklus Word	(RST)	PACCESS	Preset Access (address
INT	Initiate Control Panel Interrupt	(INT	POFF	Preset Off
IPL	Initiate Program Load Routine			
LM	Load Memory (pointed by A0)	(LM)	LM2	Load Mem. (pointed by MAR)
LR	Load Register	(LR)	LA	Load Mem. Address reg.
RM	Read memory (pointed by A0)	(RM)	RM2	Read Mem. (pointed by MAR)
RR	Read Register	(RR)	RPA	Read preset Address
0-F	16 Data Keys	(....) : Hold datakey 0 down while pressing function....		

Figure 6.5 FRONT VIEW OF HHP

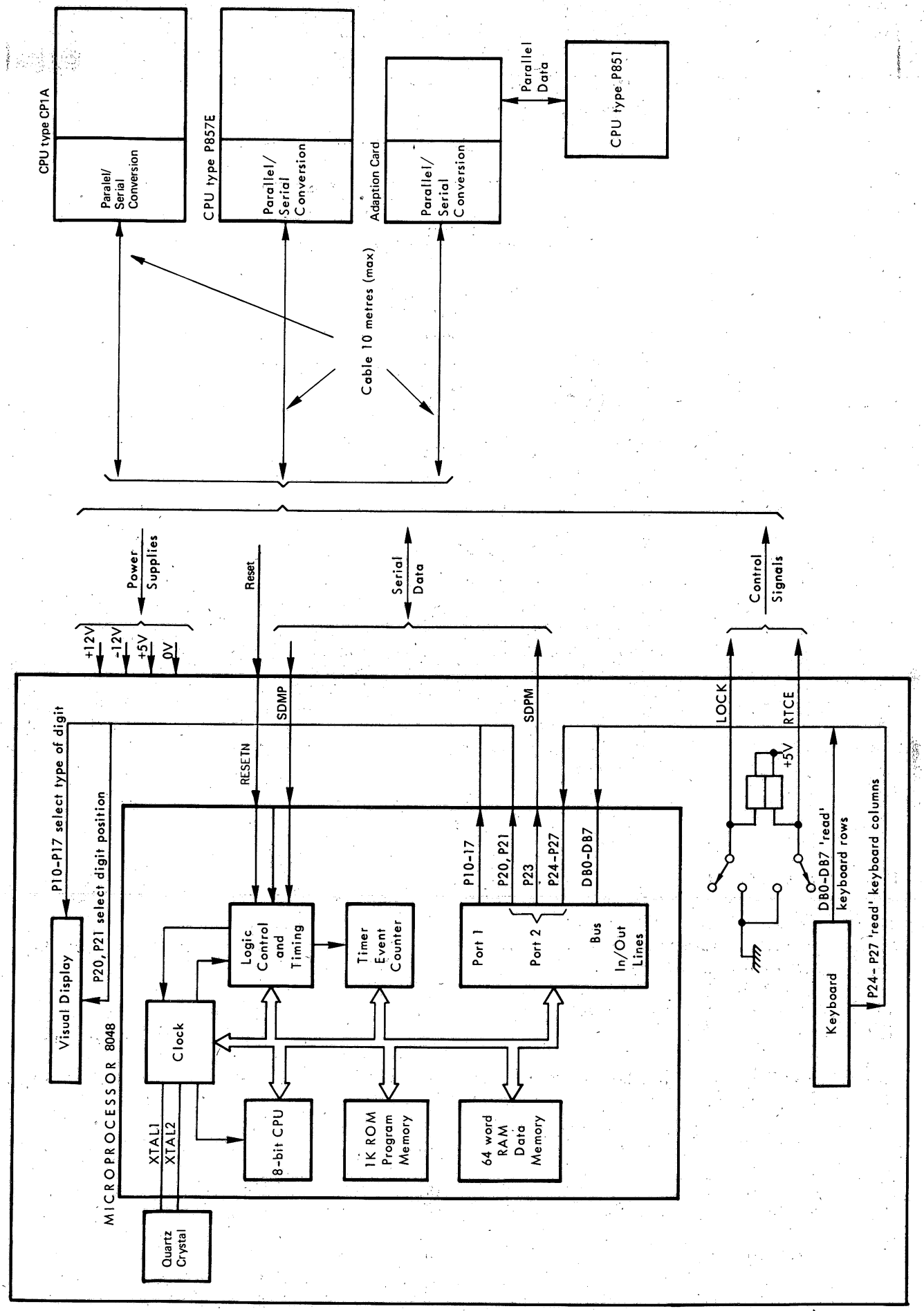


Figure 6.6 HHP IN P800 CONFIGURATIONS

6.8 INTERFACE CONNECTOR HHP

HHP CONNECTOR	SIGNAL	DESCRIPTION	POWER CONSUMPTION
5	+12V	Power supply for interface signals	170mA
9	-12V		23 mA
4	+5V	Logic power supply	500mA
3	Gnd	Ground	
2	SDMP	Serial Data input from CPU	
1	LOCK	Signal 'high' inhibits all panel functions, except INT	
8	RESETN	Reset signal (from power supply)	
7	RTCE	Signal 'high' enables real time clock in CPU	
6	SDMP	Serial Data output to CPU	

SDMP and SDPM conform to CCITT specifications

Table 6.4 INTERFACE SIGNALS HHP

SWITCH SELECTION:	HEXADECIMAL CODE:
0 to F	Address: / Bx Bx Bx Bx Bx (leading zeros are not keyed in) Reg Addr. / 3x Data: / 3x 3x 3x 3x (leading zeros are not keyed in) where x is the selected hex. digit in the range 0 to F.
MCL	/40
LR	/41
RR	/42
RST	/43
IPL	/44
LM(1)	/45
LM(2)	/55
INT	/46
RM(1)	/47
RM(2)	/57
LA	/48
INST	/49
RPA	/4A
RUN	/4B
PACC	/4C
PWR	/4D
POFF	/4F
TEST	/4E
Serial Data Panel-to-Master Codes	

Table 6.5 SDPM CODES HHP

FUNCTION NAME	FUNCTION	HEXADECIMAL CODE
RUNZO	CPU mode changed from RUN to IDLE	/40
RUNZ1	CPU mode changed from IDLE to RUN	/41
TEST	Production testing only	/42

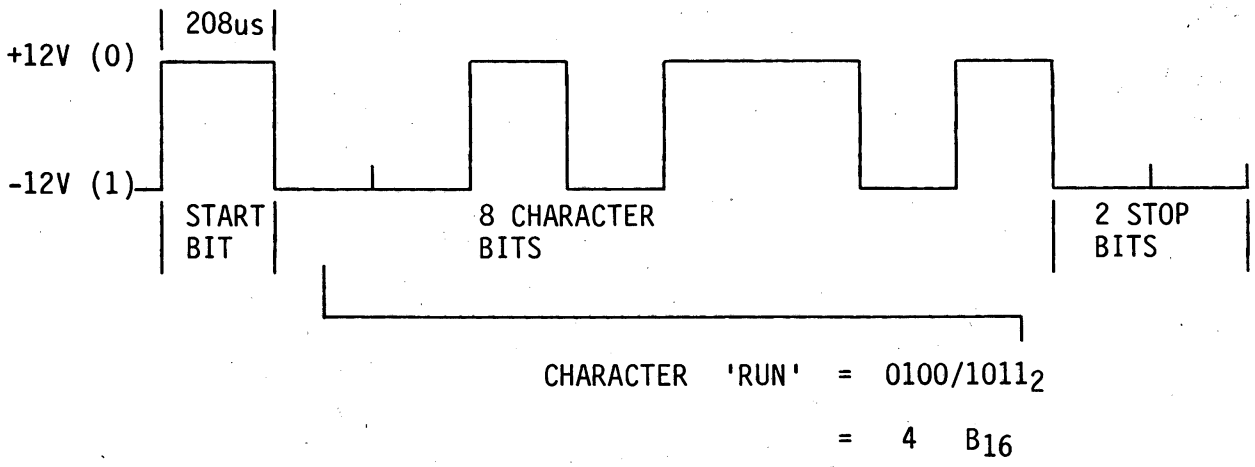
Serial Data Master-to-Panel Codes

Note: To distinguish between master-to-panel data and hand-entered data, the display of master -to-panel data is followed by a decimal point behind each digit e.g: 1.6.2.5.

HEXADECIMAL CODE FORMAT

1 start bit, 8 character bits, 2 stop bits

EXAMPLE:



Note that the least significant bit is transmitted first.

Table 6.6 SDMP CODES AND CODE FORMATS HHP

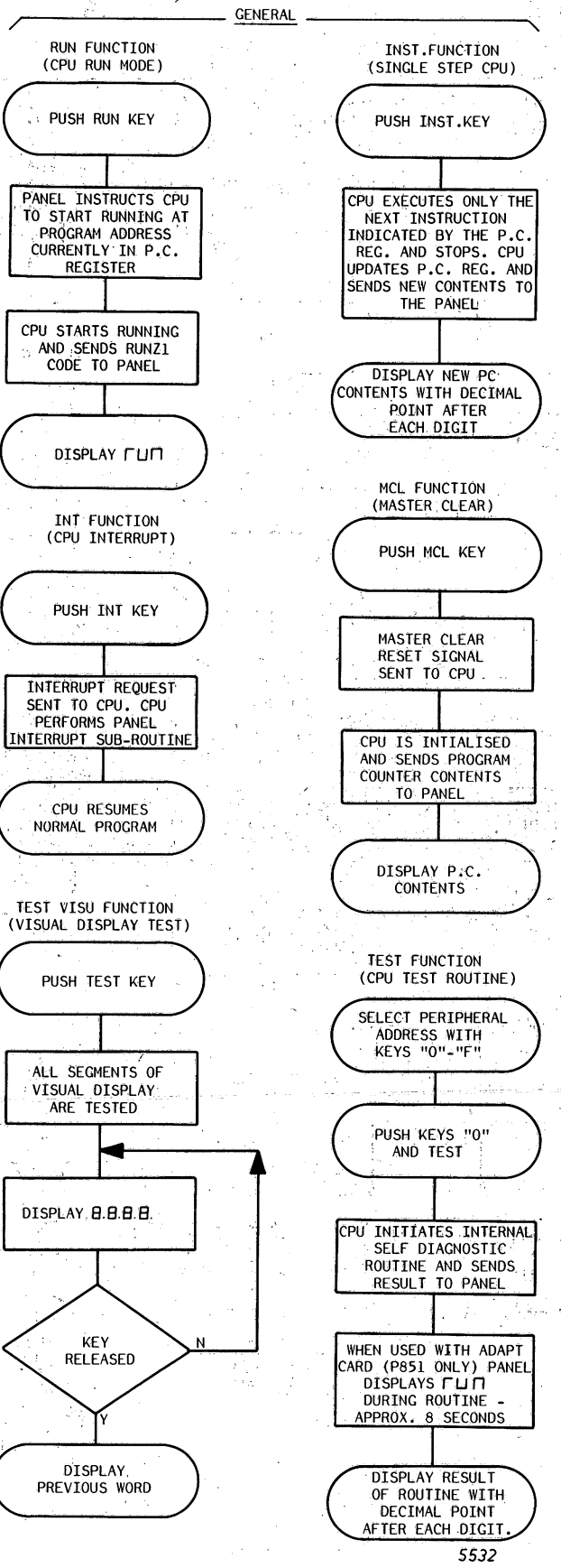


Figure 6.7 H.H.P. FUNCTIONS COMMON TO ALL CPU'S

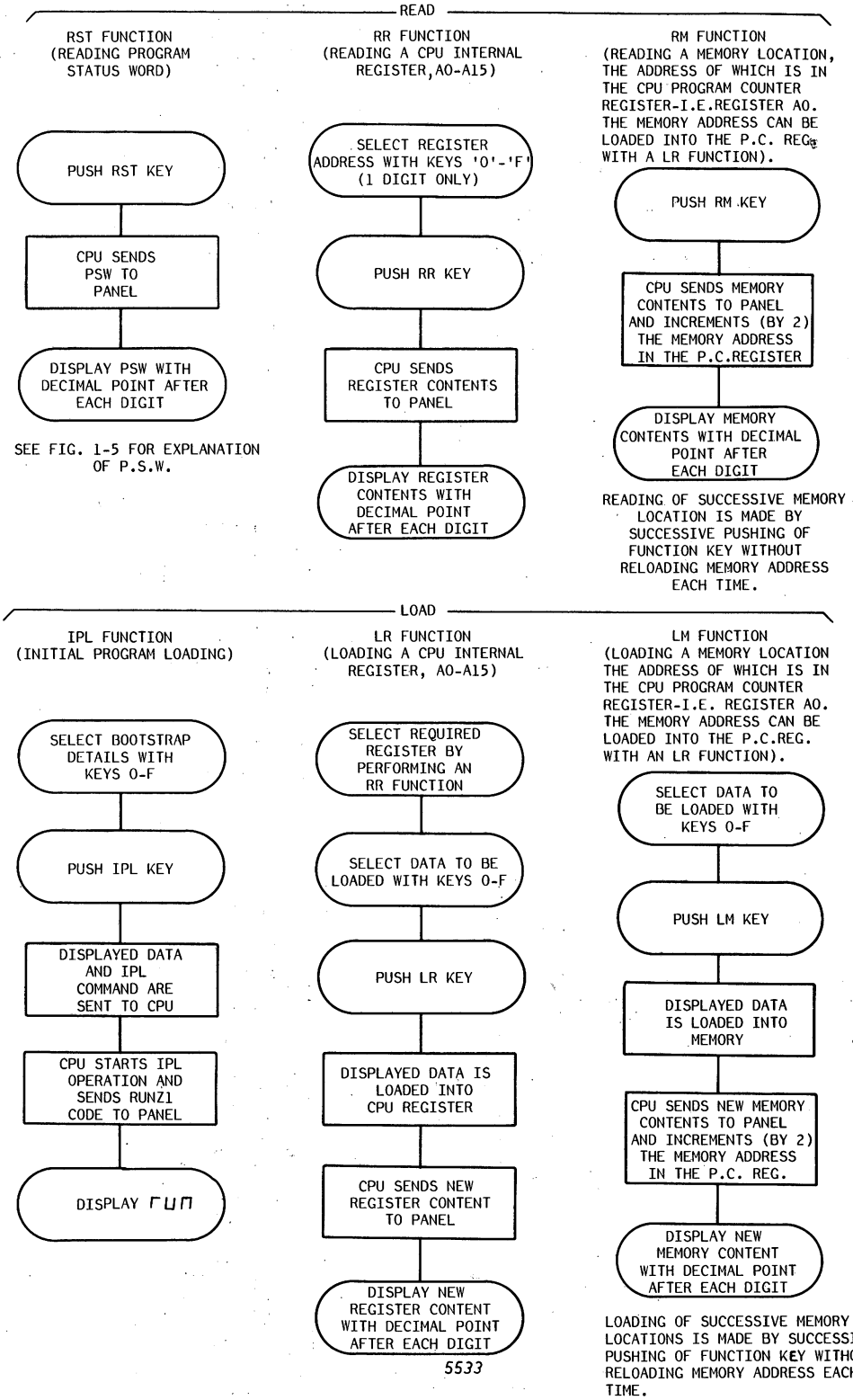


Figure 6.7 H.H.P. FUNCTIONS COMMON TO ALL CPU'S (CONT'D)

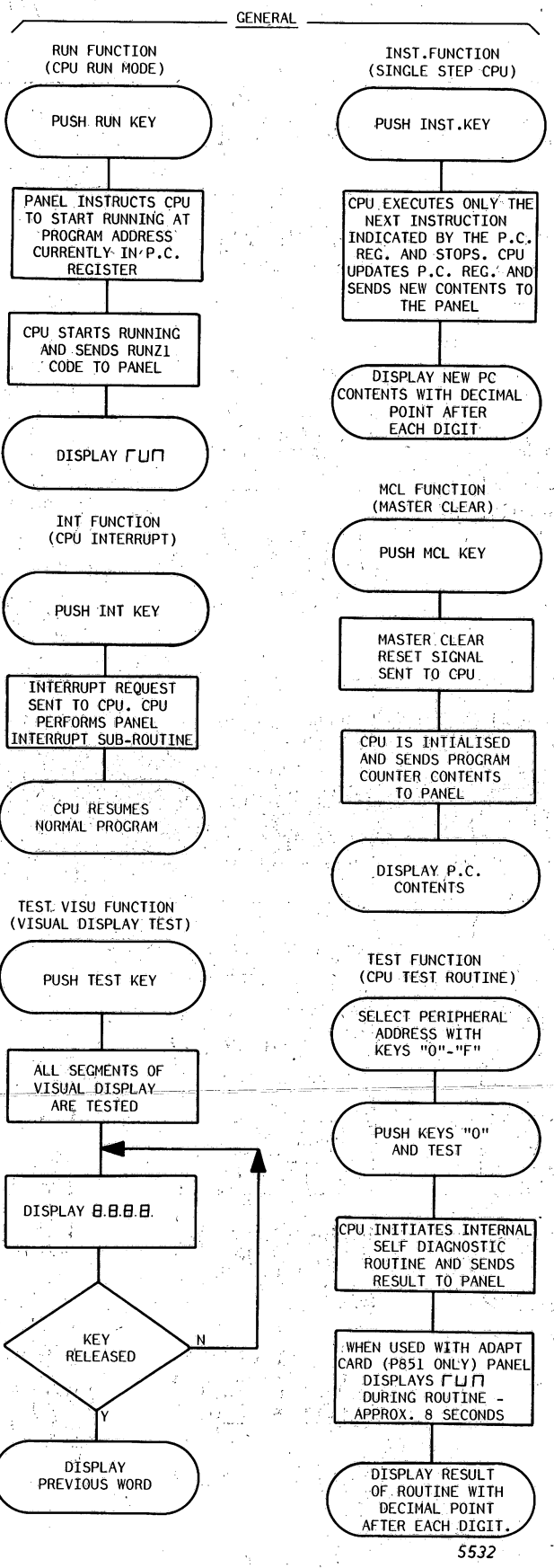


Figure 6.7 H.H.P. FUNCTIONS COMMON TO ALL CPU'S

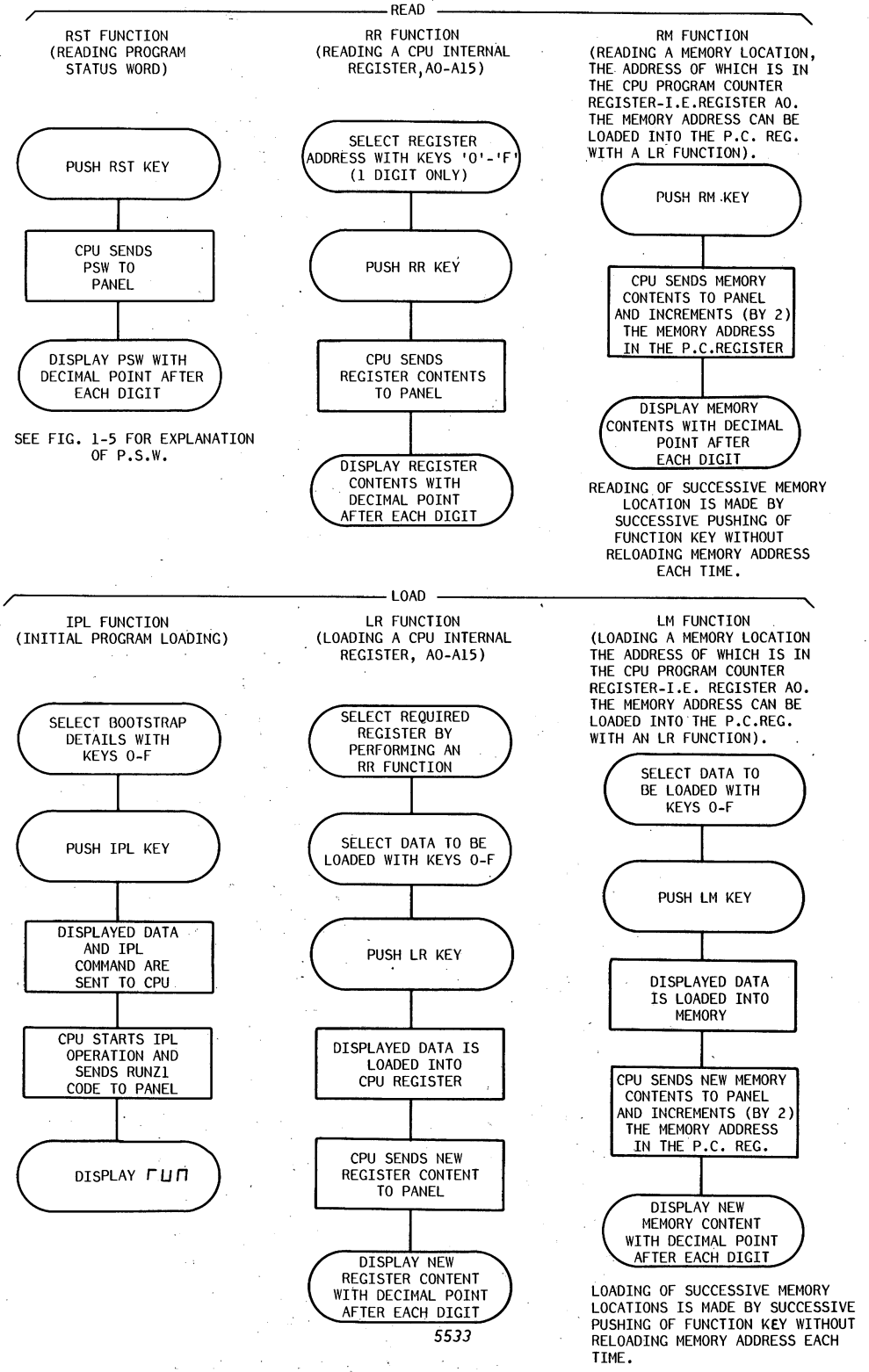


Figure 6.7 H.H.P. FUNCTIONS COMMON TO ALL CPU'S (CONT'D)

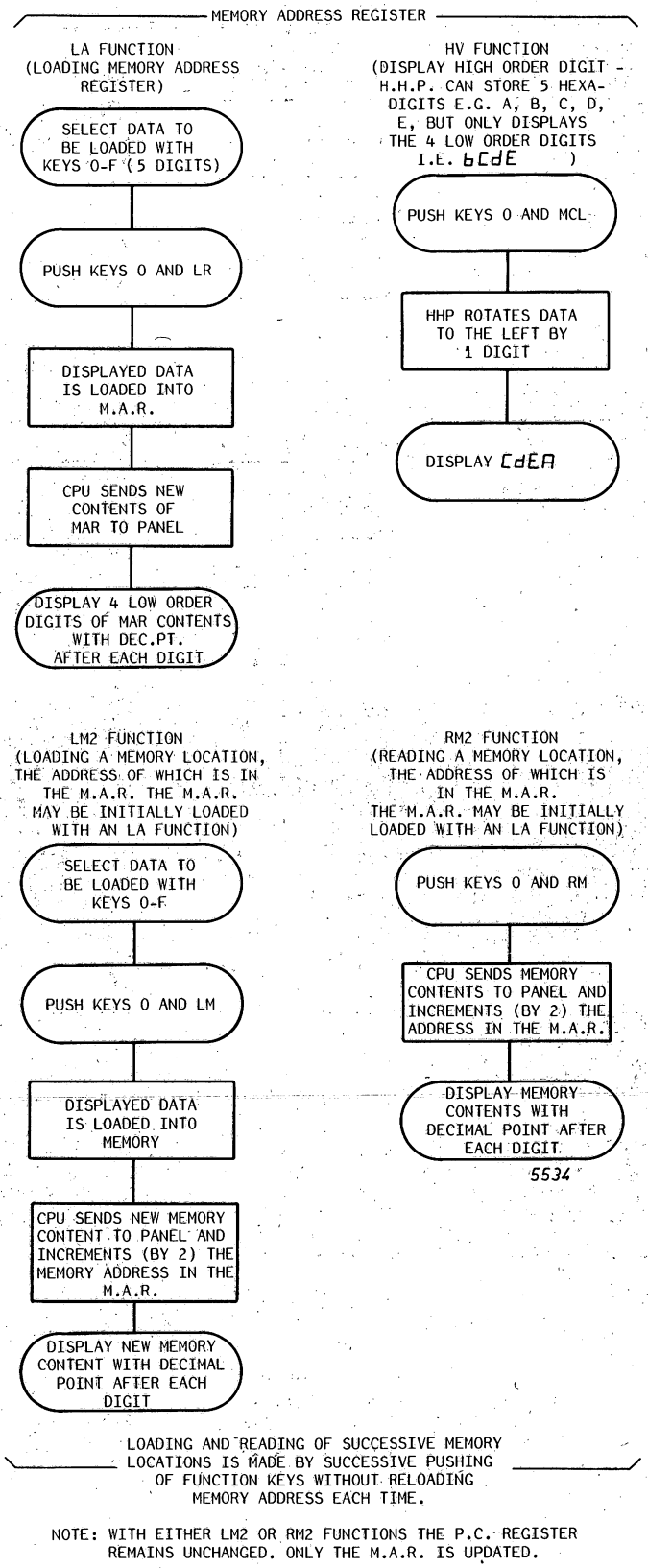


Figure 6.8 H.H.P. EXTENSION FUNCTIONS WITH P854 CPU

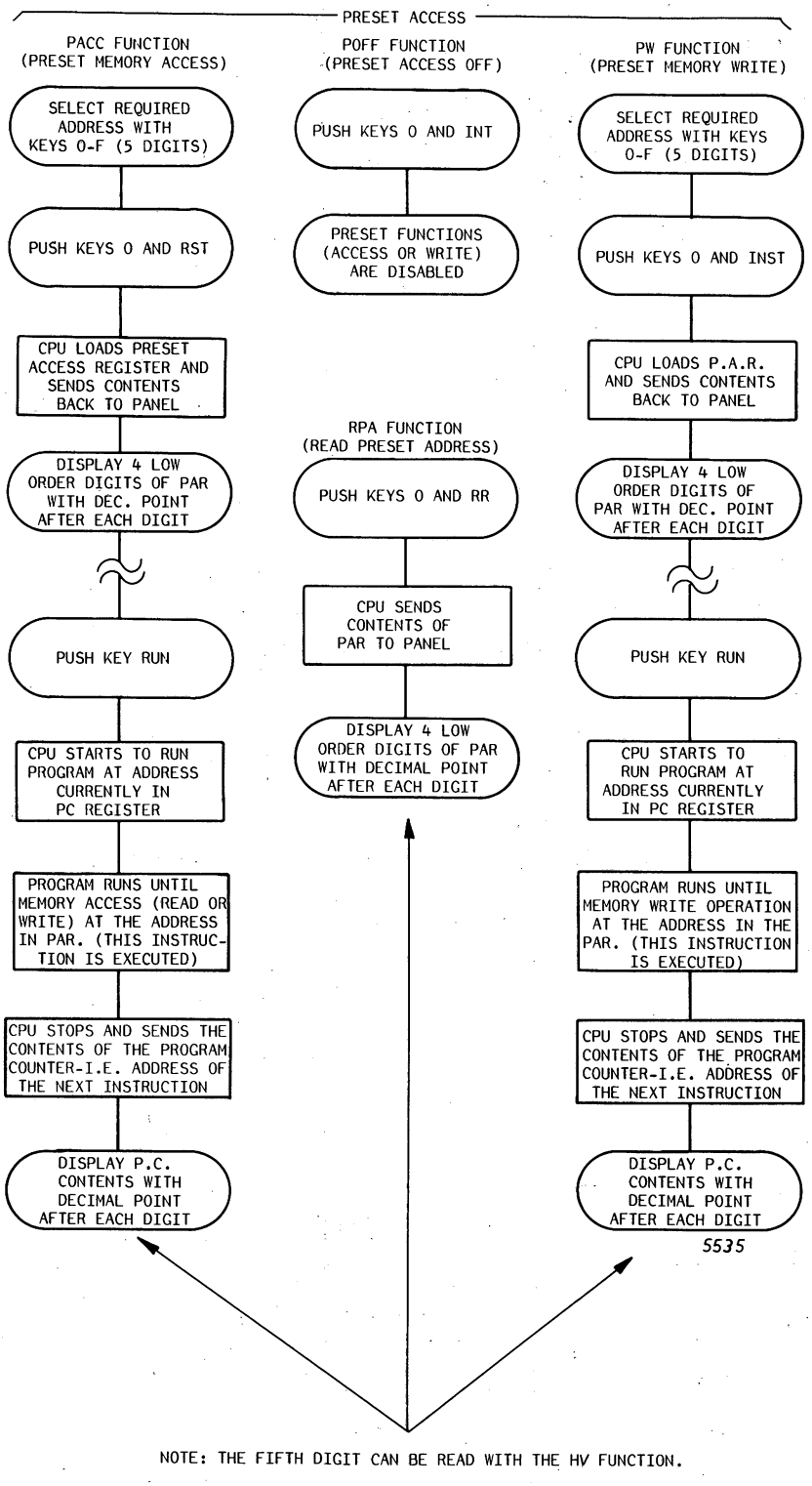


Figure 6.8 H.H.P. EXTENSION FUNCTIONS WITH P854 CPU (CONT'D)

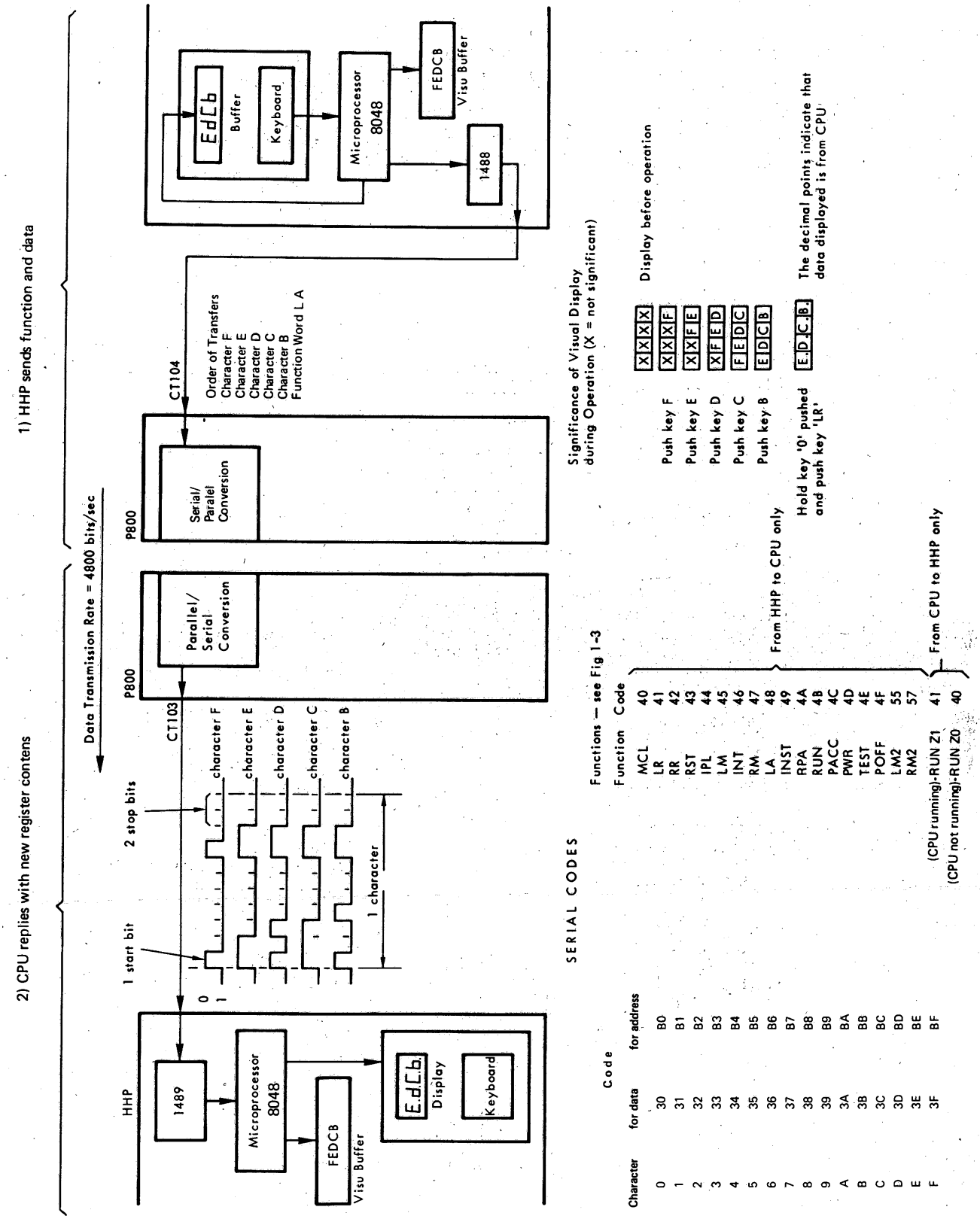


Figure 6.9 EXAMPLE OF INPUT/OUTPUT SEQUENCE - LOADING MEMORY ADDRESS REGISTER WITH CODE FEDCB

7 P853 CPU

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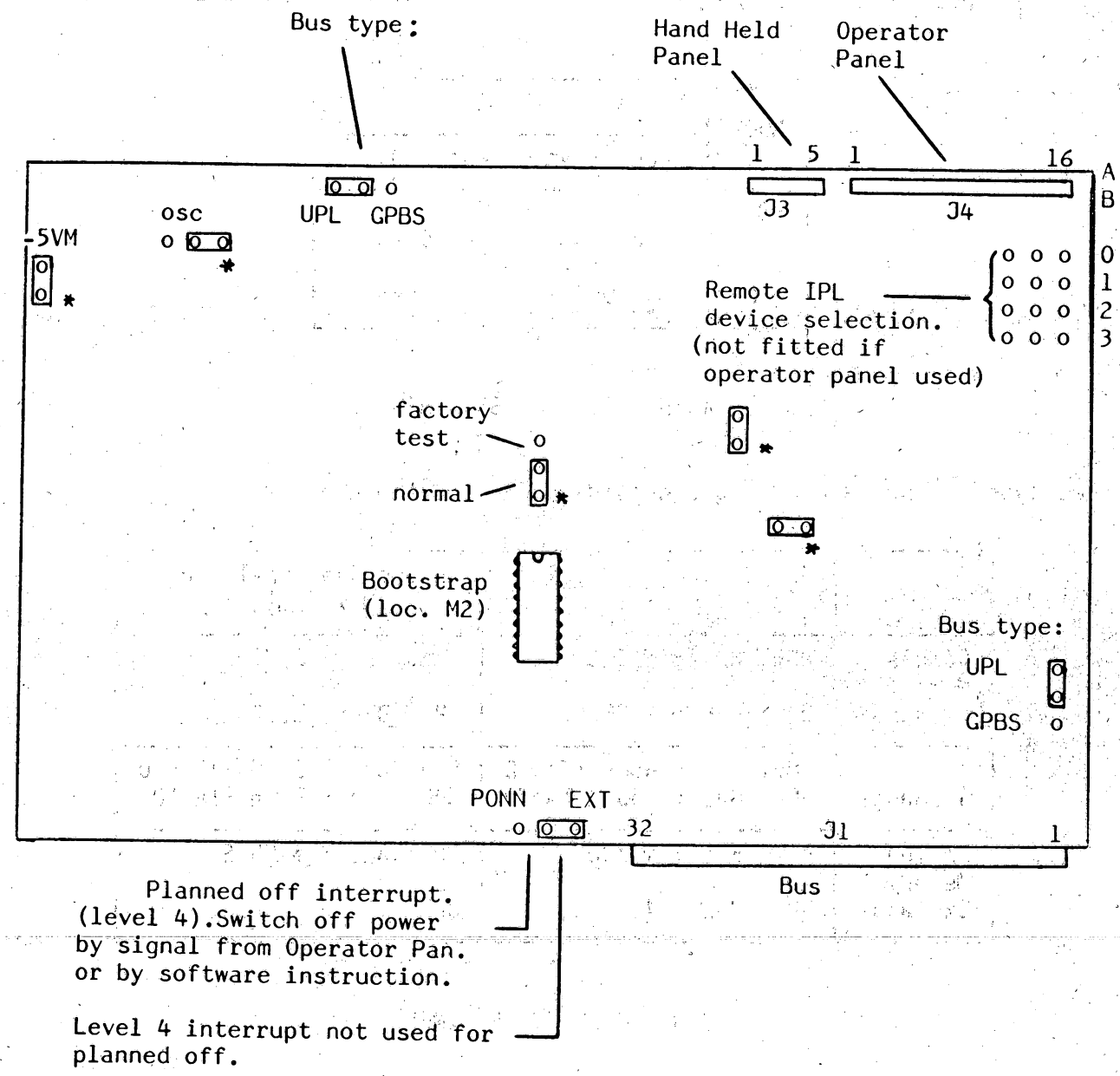
7.1 P853 CPU IDENTIFICATIONS

Type number	: See chapter 1 CPU board CP1A, without Serial Control Unit.	
Test program	: CPU - CP1A	
Power Consumption	: +5 VL, 2.8A	
	+12VL, 100mA	
	-12VL, 45mA	
	+ 5VM, 600mA	
	+12VM, 70mA	Standby
	420mA	Operating

Note: 12NC Code on sticker on the board P853 (CP1A) : 5111 199 6681X

X = modification level



* = must be fitted in shown position for normal operation

Figure 7.1 CPIA U-LINK SETTING

TIMING

A U-link enables the module to operate with either UPL or P851 timing.

Access time is defined as the time between the falling edge of the TMRN and the falling edge of the TSMN. Typical and maximum values for both modes are shown in the table below.

MODE	ACCESS TIME	
	Tacc (Typ)	Tacc (Max)
P851	575nS	654nS
UPL	670nS	749nS

Table 7.1 ACCESS TIMES

Three types of bus exchange are considered in the table below:

	Bus Occupation Timing (Typical)	Bus Occupation Timing (Maximum)
Single Memory Exchange	P851 Bus : 1.3uS UPL Bus : 1.25uS	P851 Bus : 1.79uS UPL Bus : 1.72uS
I/O Exchange	P851 : 688nS+TA+TD UPL Bus : 555nS+TA+TD	P851 Bus : 1.05uS+TA+TD UPL Bus : 890nS+TA+TD
Locked Memory Exchange	P851 Bus : 4.72uS UPL Bus : 4.67uS	P851 Bus : 5.59uS UPL Bus : 5.52uS

Table 7.2 CYCLE TIMES

Note: Locked Memory Exchange is only used during the execution of Test and Set, and Test and Reset instructions. During WRITE to memory instructions (and especially a WRITE character instruction) the operation is always preceeded by a READ, without locking the Bus between both operations.

Due to the Locked Memory Exchange and the refresh cycle for MOS memories, the Master with the highest priority must be able to wait for up to 6.3uS before getting access to the Bus.

TA = Access Time
TD = Delay Time

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1C01	+12VL	1B01	ERQN	1A01	-12VL
1C02	+5VM	1B02	BUSRN	1A02	+5VM
1C03	BCI	1B03	MSN	1A03	INCL
1C04	*IRAIN12	1B04	0V	1A04	IRALN14
1C05	*IRAKN13	1B05	BSYN	1A05	IRAMN15
1C06	0V	1B06	OKO	1A06	0V
1C07	PWFN	1B07	*RIPLN	1A07	RSLN
1C08	CLEARN	1B08	RTCN	1A08	ACN
1C09	0V	1B09	BAWOFN	1A09	0V
1C10	TMPN	1B10	STOPN	1A10	TSMN
1C11	TMEN	1B11	0V	1A11	TMRN
1C12	0V	1B12	MADE0	1A12	0V
1C13	MAD00	1B13	MADE1	1A13	MAD01
1C14	MAD02	1B14	0V	1A14	MAD03
1C15	MAD04	1B15	MADE2	1A15	MAD05
1C16	MAD06	1B16	MADE3	1A16	MAD07
1C17	MAD08	1B17	MADE4	1A17	MAD09
1C18	MAD10	1B18	MADE5	1A18	MAD11
1C19	MAD12	1B19	MADE6	1A19	MAD13
1C20	MAD14	1B20	MADE7	1A20	MAD15
1C21	CHA	1B21	0V	1A21	WRITE
1C22	0V	1B22	*IRAAN 4	1A22	0V
1C23	BI008N	1B23	*IRABN 5	1A23	BI000N
1C24	BI009N	1B24	*IRACN 6	1A24	BI001N
1C25	BI010N	1B25	*IRADN 7	1A25	BI002N
1C26	BI011N	1B26	0V	1A26	BI003N
1C27	BI012N	1B27	*IRAEN 8	1A27	BI004N
1C28	BI013N	1B28	*IRAFN 9	1A28	BI005N
1C29	BI014N	1B29	*IRAGN10	1A29	BI006N
1C30	BI015N	1B30	*IRAHN11	1A30	BI007N
1C31	+12VM	1B31	+5VL	1A31	+12VM
1C32	+5VL	1B32	+5VL	1A32	+5VL

* These signals are not connected to the back panel bus.

For the interrupt inputs IRAxN the interrupt level is written behind the signal name

Table 7.3 CONNECTOR PINNING UPL-BUS

This is a BERG 2 x 5 pin connector

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
3A01	SDPM	3B01	LOCK
3A02	RTCE	3B02	SDMP
3A03	RESETN	3B03	GND
3A04	-12V	3B04	+5V
3A05	Dummy Pin	3B05	+12V

Table 7.4 HANDHELD PANEL CONNECTOR

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
4A01	0V	4B01	RTCE
4A02	RUNN	4B02	0V
4A03	0V	4B03	SWOFN**
4A04	PONN	4B04	0V
4A05	0V	4B05	Blank*
4A06	ARE	4B06	SHEXN
4A07	0V	4B07	0V
4A08	LOCK	4B08	OUTCODEN7
4A09	0V	4B09	OUTCODEN6
4A10	INCODE 5	4B10	OUTCODEN5
4A11	INCODE 4	4B11	OUTCODEN4
4A12	INCODE 3	4B12	OUTCODEN3
4A13	INCODE 2	4B13	OUTCODEN2
4A14	INCODE 1	4B14	OUTCODEN1
4A15	INCODE 0	4B15	OUTCODEN0
4A16	0V	4B16	0V

* Not used at CP1A level.
** This signal is not on P853 machines.

Table 7.5 OPERATOR PANEL CONNECTOR

7.4 SHORT DESCRIPTION OF TESTPROGRAMS:

Test programs CPIA
mem. size 8kw
No output on CTW
No power fail. -or- RTC allowed

Procedure

. IPL
- Program stops on /0300 = restart address
- Press MCL, RUN
- program loops continuously. Address/024A contains the number of passes.
- Error: program stops. Halt address indicates faulty instruction in listing. One complete CPU test lasts 6 seconds.

8 P854 CPU CENTRAL PROCESSOR UNIT

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8.1 P854 CPU IDENTIFICATIONS

Type no.	P854-300 (6U12 Rack)	
	P854-400 (RU22 Rack)	
Test Programs	CPU	- CP57RE
	MIOP	- see Chapter: - 9 (IOP command words)
		- 11 (MMU)
	Intergr. CU:	
	ASR/PER31ØØ	- BBSER1
	VDU	- BBDISP
Devices	PER31ØØ	- P842-ØØ1
	VDU	- P817-ØØ2

Power consumption:	+5VL	+12VL	-12VL
C7E1	4A		
C7E2	2.5A	5ØmA	5ØmA
MIOP	2.6A		

12NC code on the sticker on the board:

C7E1A	5111 199	6377x	(5322 216 25725)
C7E2A	5111 199	6376x	(5322 216 25724)
MIOPA	5111 199	6375x	(5322 216 25723)
C7E1B	5111 199	6198x	(5322 216 21Ø81)
C7E2B	5111 199	6199x	(5322 216 21Ø82)
MIOPB	5111 199	62ØØx	(5322 216 21Ø83)

x = modification level

8.2 INSTALLATION DETAILS

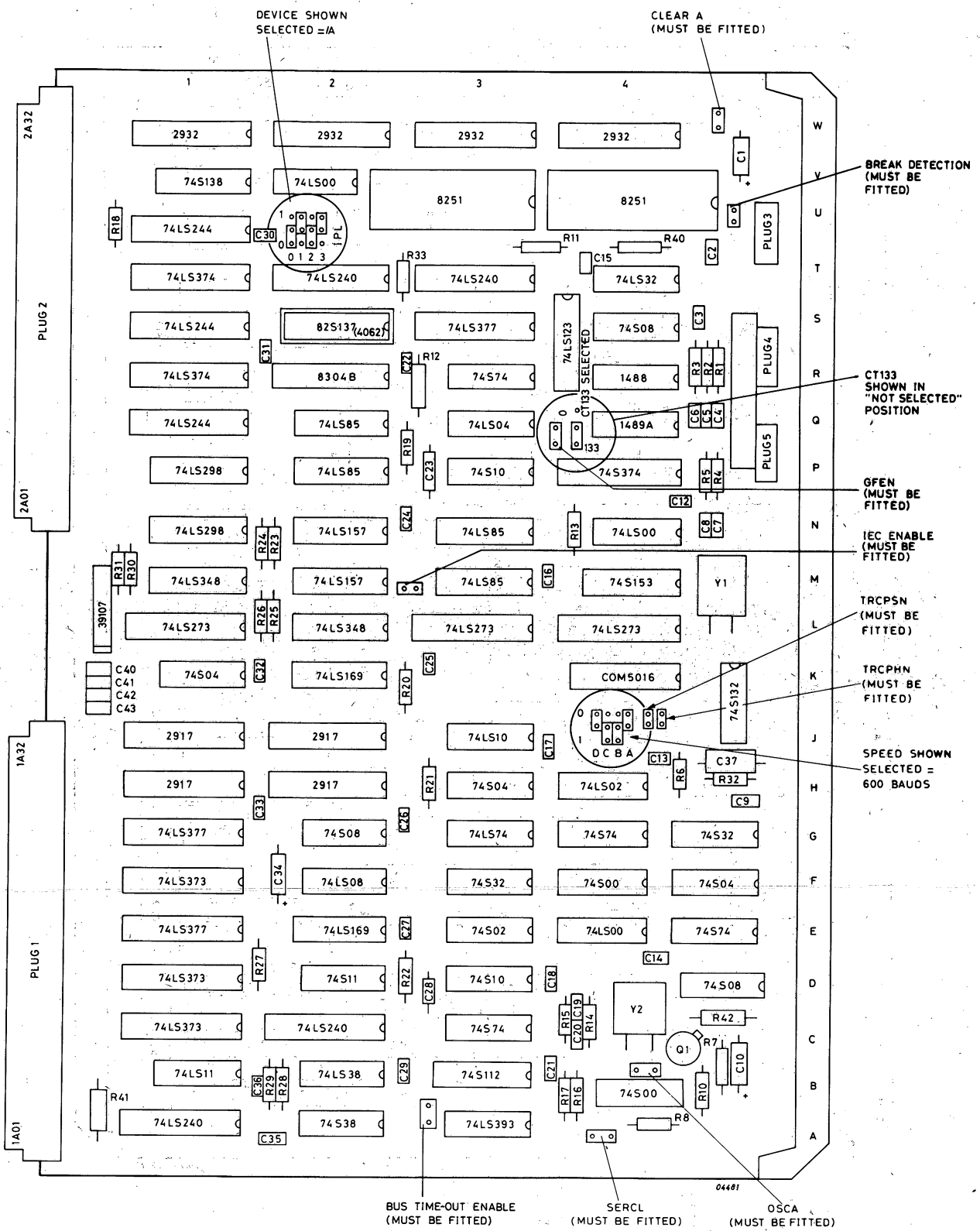


Figure 8.1 C7E2B COMPONENT LAYOUT AND LINKS

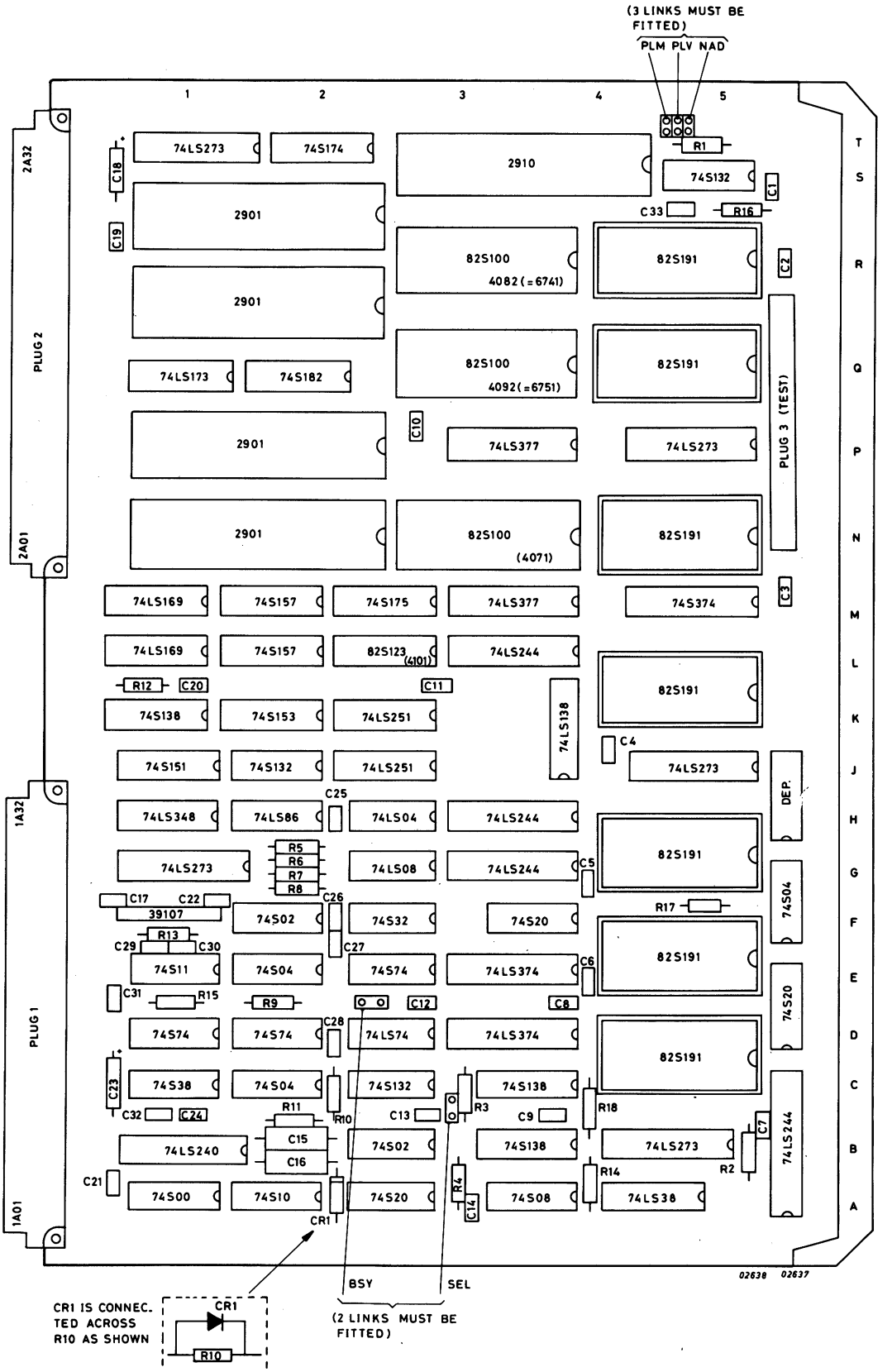


Figure 8.2 C7E1B COMPONENT LAYOUT AND LINKS

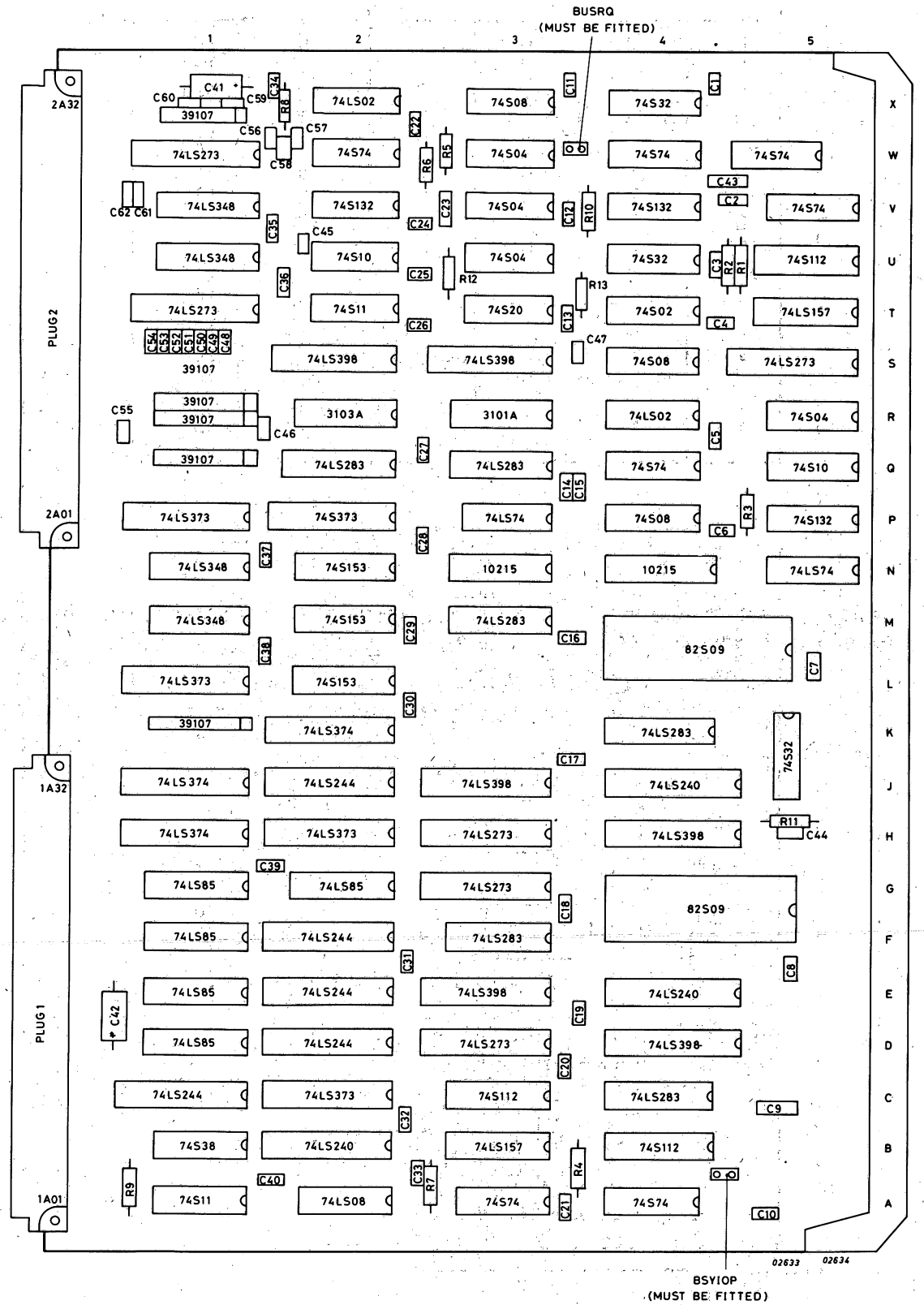
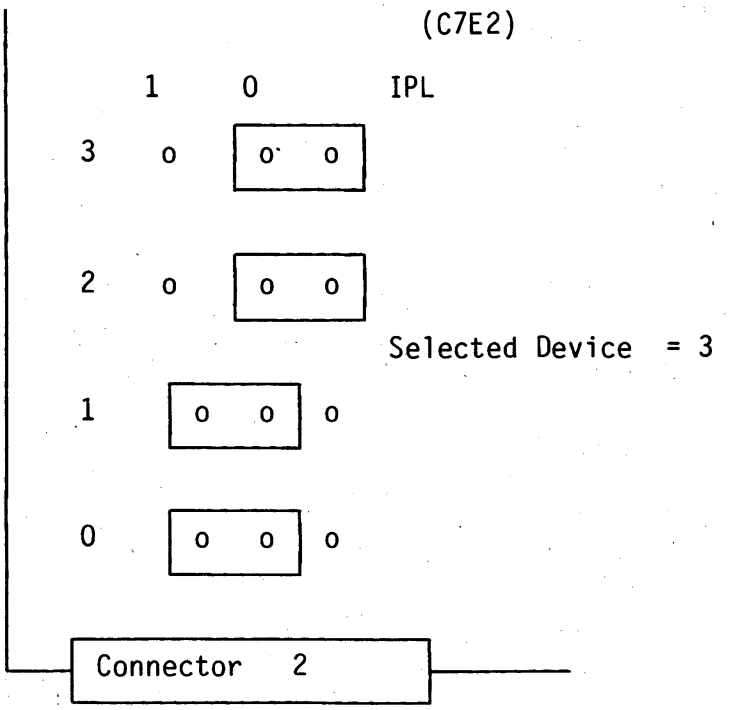


Figure 8.3 MIOPB LAYOUT AND LINKS

3	2	1	0		MEMORY ADDRESS
OPS3N	OPS2N	OPS1N	OPSON	WORD	HEX
0	0	0	0	0	1FE
0	0	0	1	1	1FC
0	0	1	0	2	1FA
0	0	1	1	3	1F8
0	1	0	0	4	1F6
0	1	0	1	5	1F4
0	1	1	0	6	1F2
0	1	1	1	7	1F0
1	0	0	0	8	1EE
1	0	0	1	9	1EC
1	0	1	0	10	1EA
1	0	1	1	11	1E8
1	1	0	0	12	1E6
1	1	0	1	13	1E4
1	1	1	0	14	1E2
1	1	1	1	15	1E0

Table 8.1 SELECT-IPL (REMOTE LOAD)

The following diagram shows the identification that is silkscreened on the card and an example of word selection.

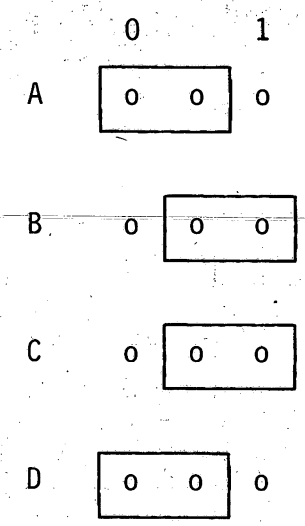


Transmit/Receive U Link Positions				Baud Rate
D	C	B	A	
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134,5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1.200
1	0	0	0	1.800
1	0	0	1	2.000
1	0	1	0	2.400
1	0	1	1	3.600
1	1	0	0	4.800
1	1	0	1	7.200
1	1	1	0	9.600
1	1	1	1	19.200

shown

Table 8.2 V24 - PERIPHERAL INTERFACE - SPEED SELECTION

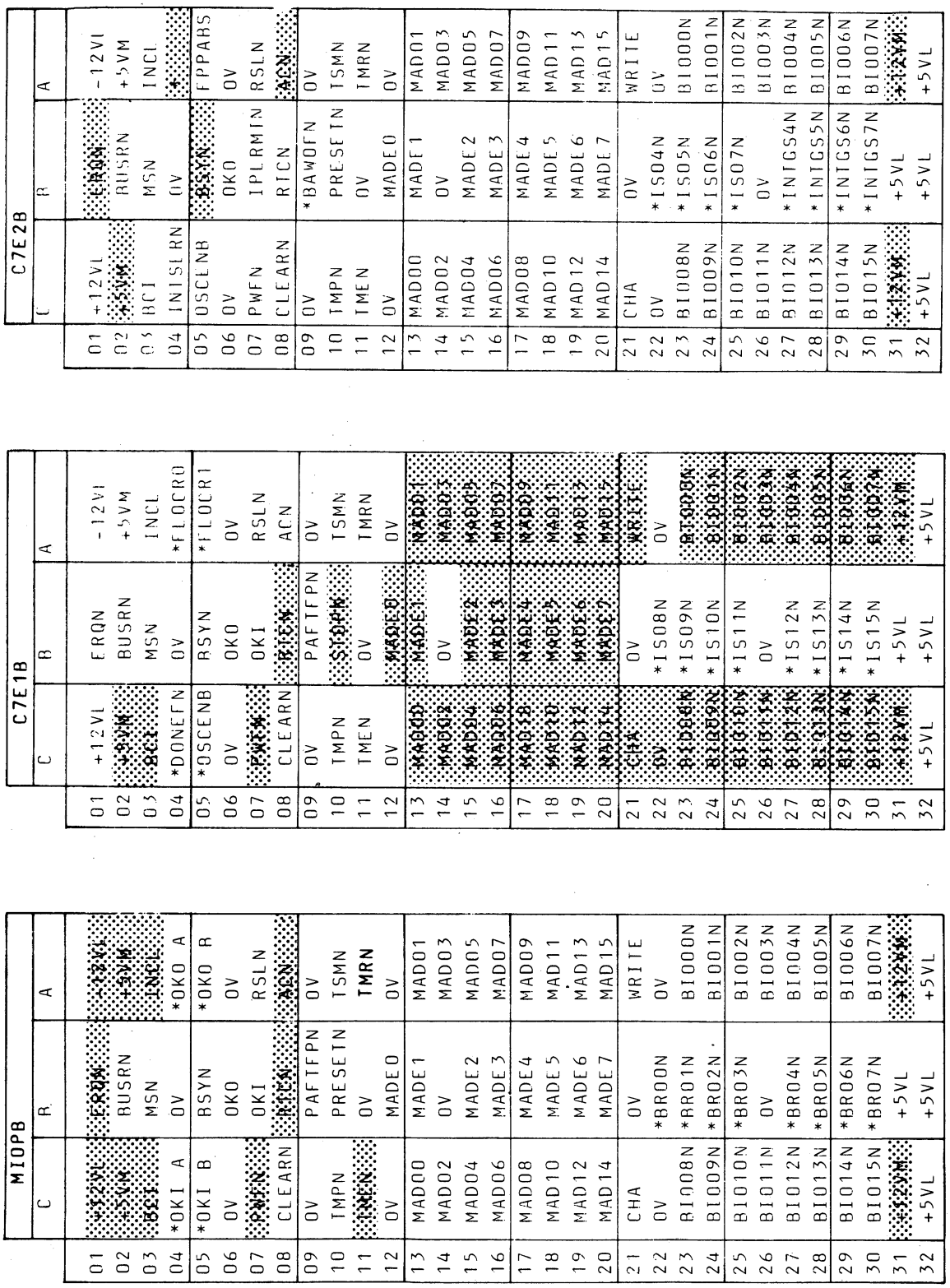
The following diagram shows an identification that is silkscreened on the card, and an example of speed selection:



(C7E2)

Selected speed is 600 bauds (PER 3100)

8.3 INTERFACE CONNECTIONS



MIOPB			
C	R	A	
+12VL	ERQN	-12VL	01
+5VM	BUSRN	+5VM	02
BCI	MSN	INCL	03
*OKI A	0V	*OKO A	04
*OKI B	BSYN	*OKO B	05
0V	OKO	0V	06
PWFN	OKI	RSLN	07
CLEARN	RTCN	ACN	08
0V	PAFTFPN	0V	09
TMPN	PRESETN	TSMN	10
TMEN	0V	TMRN	11
0V	MADE0	0V	12
MAD00	MADE1	MAD01	13
MAD02	0V	MAD03	14
MAD04	MADE2	MAD05	15
MAD06	MADE3	MAD07	16
MAD08	MADE4	MAD09	17
MAD10	MADE5	MAD11	18
MAD12	MADE6	MAD13	19
MAD14	MADE7	MAD15	20
CHA	0V	WRITE	21
0V	*BR00N	0V	22
BI008N	*RR01N	BI000N	23
BI009N	*BR02N	BI001N	24
BI010N	*BR03N	BI002N	25
BI011N	0V	BI003N	26
BI012N	*BR04N	BI004N	27
BI013N	*BR05N	BI005N	28
BI014N	*BR06N	BI006N	29
BI015N	*BR07N	BI007N	30
+12VM	+5VL	+12VM	31
+5VL	+5VL	+5VL	32

C7E1B			
C	B	A	
+12VL	ERQN	-12VL	01
+5VM	BUSRN	+5VM	02
BCI	MSN	INCL	03
*DONEFN	0V	*FLOCRO	04
*OSCENB	RSYN	*FLOCRI	05
0V	OKO	0V	06
PWFN	OKI	RSLN	07
CLEARN	RTCN	ACN	08
0V	PAFTFPN	0V	09
TMPN	STOPN	TSMN	10
TMEN	0V	TMRN	11
0V	MADE0	0V	12
MAD00	MADE1	MAD01	13
MAD02	0V	MAD03	14
MAD04	MADE2	MAD05	15
MAD06	MADE3	MAD07	16
MAD08	MADE4	MAD09	17
MAD10	MADE5	MAD11	18
MAD12	MADE6	MAD13	19
MAD14	MADE7	MAD15	20
CHA	0V	WRITE	21
0V	*IS08N	0V	22
BI008N	*IS09N	BI000N	23
BI009N	*IS10N	BI001N	24
BI010N	*IS11N	BI002N	25
BI011N	0V	BI003N	26
BI012N	*IS12N	BI004N	27
BI013N	*IS13N	BI005N	28
BI014N	*IS14N	BI006N	29
BI015N	*IS15N	BI007N	30
+12VM	+5VL	+12VM	31
+5VL	+5VL	+5VL	32

C7E2B			
C	B	A	
+12VL	ERQN	-12VL	01
+5VM	BUSRN	+5VM	02
BCI	MSN	INCL	03
INISLRN	0V	*	04
OSCLNB	BSYN	FPPABS	05
0V	OKO	0V	06
PWFN	IPLRMIN	RSLN	07
CLEARN	RTCN	ACN	08
0V	*BAWOFN	0V	09
IMPN	PRESETN	TSMN	10
IMEN	0V	IMRN	11
0V	MADE0	0V	12
MAD00	MADE1	MAD01	13
MAD02	0V	MAD03	14
MAD04	MADE2	MAD05	15
MAD06	MADE3	MAD07	16
MAD08	MADE4	MAD09	17
MAD10	MADE5	MAD11	18
MAD12	MADE6	MAD13	19
MAD14	MADE7	MAD15	20
CHA	0V	WRITE	21
0V	*IS04N	0V	22
BI008N	*IS05N	BI000N	23
BI009N	*IS06N	BI001N	24
BI010N	*IS07N	BI002N	25
BI011N	0V	BI003N	26
BI012N	*INIGS4N	BI004N	27
BI013N	*INIGS5N	BI005N	28
BI014N	*INIGS6N	BI006N	29
BI015N	*INIGS7N	BI007N	30
+12VM	+5VL	+12VM	31
+5VL	+5VL	+5VL	32

Figure 8.4 CONNECTOR 1 LEVEL - C7E2, C7E1, MIOP

Figure 8.5 CONNECTOR 2 LEVEL - C7E2, C7E1, MIOP

	MIOPB		
	C	B	A
01	APN	BRO8N	OSC
02	GPRESETN	BRO9N	MADSOO
03	BSYCPUEXN	BR10N	MADSO1
04	BSYCPUN	BR11N	MADSO2
05	TMRENB	BR12N	MADSO3
06		BR13N	OV
07	OV	BR14N	ALU10
08	DOO	BR15N	ALU11
09	DO1	ALUO4	ALU12
10	DO2	PRESETN	ALU13
11	DO3		ALU14
12	DO4		ALU15
13	DO5	ALUCIN	
14	DO6	IS16N	SELR2
15	DO7	IS17N	OKMMU
16	DO8	IS18N	FLAGCW3N
17	DO9	IS19N	BIORECN
18	D10	IS20N	PAFN
19	D11	IS21N	SELSPBUFN
20	D12	IS22N	
21	D13	IS23N	IEC3
22	D14	IS24N	IEC4
23	D15	IS25N	IEC5
24	ENBIOP	IS26N	INTGS2N
25	FUN	IS27N	INTGS3N
26	IOPN	OV	GPSPN
27		IS28N	INTE3N
28		IS29N	INTE1N
29		IS30N	RUNN
30	+5V **	IS31N	GFETCH
31		BSYCN	WAIT
32	WRITEM		M1OPABS

** NOTE: SI P854-M-022 MIOP **A**

	C7E1B		
	C	B	A
01	APN	DONEFCPN	GPCHAN
02	GPRESETN	GPLRLDN	
03	BSYCPUEXN	ALUOO	GPMADN
04	BSYCPUN	ALUO1	SELIPLN
05	TMRENB	ALUO2	TMFN
06	FPPABS	ALUO3	IRUNA
07	FEN	ALUO4	ALU10
08	DOO	ALUO5	ALU11
09	DO1	ALUO6	ALU12
10	DO2	ALUO7	ALU13
11	DO3	ALUO8	ALU14
12	DO4	ALUO9	ALU15
13	DO5	ALUCIN	PUPF
14	DO6	ALUI1	SELR2
15	DO7	ALUI7	OKMMU
16	DO8	ALUMADP1	GROUND (Back Panel)
17	DO9	CRO	FLOACT
18	D10	CR1	PAFN
19	D11	NADO3	SELSPBUFN
20	D12		RUNIRN
21	D13	NADO8	IEC3
22	D14	NADO9	IEC4
23	D15	NAD10	IEC5
24	ENBIOP	SELCDNSIN	INTEON
25	FUN	BSYCN	GPSPN
26	PCI3	DENB	INTGS1N
27	PCI2	BOFFN	SEL825IN
28	PCI1	TIMEOUT	INTE1N
29	PCIO	TMRZON	MIOPABS
30	PCCI	SELD2	GFETCH
31	LOADSN	SELD1	SEQCPU1
32	WRITEM	SELDO	SEQCPUO

	C7E2B		
	C	B	A
01	APN	DONEFCPN	OSC
02	GPCHAN	GPLRLDN	MADSOO
03	BYSCPUEXN	ALUOO	MADSO1
04	BSYCPUN	ALUO1	MADSO2
05	GPMADN	ALUO2	MADSO3
06	OV	ALUO3	IRUNA
07	FEN	ALUO4	ALU10
08	DOO	ALUO5	ALU11
09	DO1	ALUO6	ALU12
10	DO2	ALUO7	ALU13
11	DO3	ALUO8	ALU14
12	DO4	ALUO9	ALU15
13	DO5	ALUCIN	PUPF
14	DO6	ALUI1	SELIPLN
15	DO7	ALUI7	OKMMU
16	DO8	ALUMAIP1	FLAGCW3N
17	DO9	CRO	BIORECN
18	D10	CR1	PAFN
19	D11	NADO3	SELSPBUFN
20	D12	IOPN	RUNIRN
21	D13	NADO8	IEC3
22	D14	NADO9	IEC4
23	D15	NAD10	IEC5
24	ENBIOP	SELCDNSIN	INTGS2N
25	FUN	SELOICN	INTGS3N
26	PCI3	DENB	INTGS1N
27	PCI2	BOFFN	INTEON
28	PCI1	TIMEOUT	SEL825IN
29	PCIO	TMRZON	RUNN
30	PCCI	SELD2	WAIT
31	LOADSN	SELD1	SEQCPU1
32	WRITEM	SELDO	SEQCPUO

C7E2B Pin No.	Signal Name	Description	Source	Destination
3B03	OPSON	Address Lines from a Remote Device to address the last 16 words of the Bootstrap Key position	Remote Device	C7E2/F
3B02	OPS1N			
3B04	OPS2N			
3B01	OPS3N			
3A05	not connected			
3A01-04	0V			
3B05	0V			

Table 8.3 IPL REMOTE LOAD INTERFACE - CONNECTOR 3

C7E2B Pin No.	Signal Name	Description	Source	Destination
4B01	LOCK	= 0 Control Panel functions are enabled. = 1 Control Panel functions (except INT) are inhibited.	FRCP	C7E2/A
4B03	0V			
4A01	SDPM	Serial Data (CT104)	FRCP	C7E2/A
4B02	SDMP	Serial Data (CT103)	C7E2/A	FRCP
4A02	RTCE	= 0 inhibit Real Time Clock = 1 enable Real Time Clock	FRCP	C7E2/F
4A03	RESETN	Master Reset	C7E2/A	FRCP
4B04	+5V			
4A04	-12V			
4A05	not connected	Key Position		
4B05	+12V			

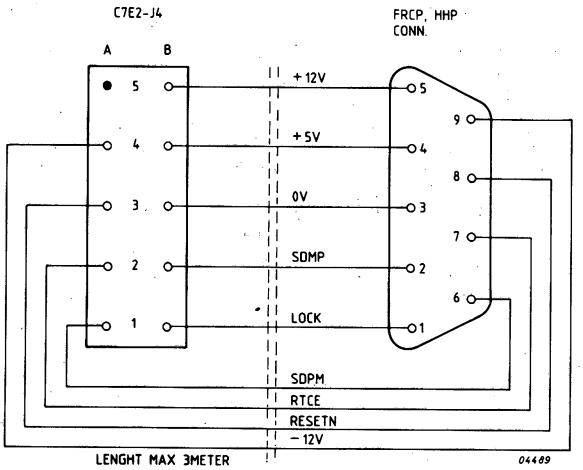
Table 8.4 CONTROL PANEL INTERFACE (FRCP) - CONNECTOR 4

C7E2B	Signal Name	Description	Source	Destination
5B02	CT103	Serial Data	C7E2/A	D.T.E.
5A01	CT104	Serial Data	D.T.E.	C7E2/A
5A02	CT107	Modem Ready	D.T.E.	C7E2/A
5B03	CT108	Connect Modem to Line	C7E2/A	D.T.E.
5A03	CT133	Ready for Receiving	D.T.E.	CP7E2/A
5B01	0V			
5A04	0V			
5A05	0V			
5B04	0V			
5B05	not connected	key position		

Table 8.5 V24 PERIPHERAL INTERFACE - CONNECTOR 5

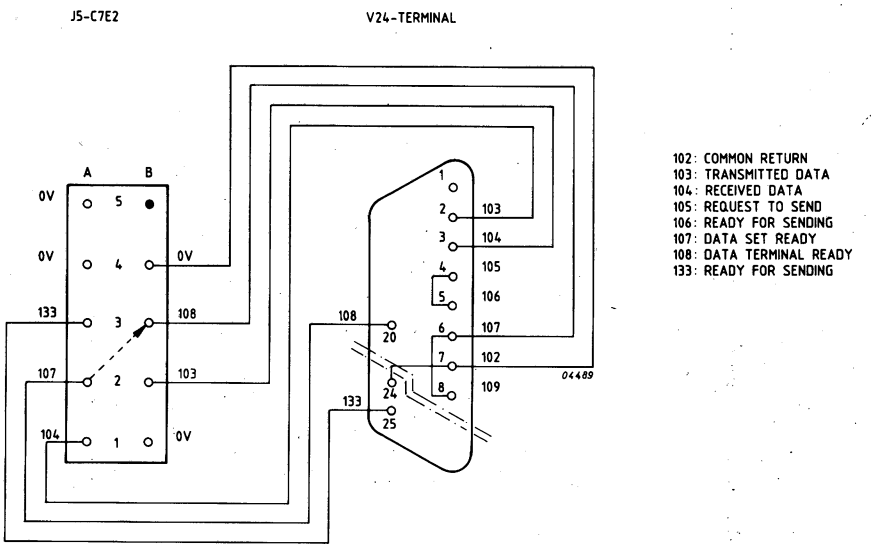
Pin	Signal Name	Description
3A01	ROMAD08	Microprogram ROM Address Lines, note that only 9 of the 11 lines are available here, for ROMAD09 and 10 see pins 3B17 and 3B18 (C7E1/B).
02	07	
03	06	
04	05	
05	04	
06	03	
07	02	
08	01	
09	ROMAD00	
10		
11	BSYCPU	Indicates CPU busy with Bus (C7E1/E).
12	TMPN	Indicates Transfer Master to Peripheral (C7E1/E).
13	TMRN	Indicates Transfer Master to Memory (C7E1/E).
14	OSCENB	Enables the internal clock (C7E1/D).
15		Not used
16		Not used
17	RSLAN	Simulates RSLN from the Power Supply (C7E1/E).
18	APTEST	Enables an external test of the CPU Sequensor signal AP (C7E1/D).
19	5V	
20	5V	
3B01	D00	3-state internal CPU Bus (C7E1/B).
02	01	
03	02	
04	03	
05	04	
06	05	
07	06	
08	07	
09	08	
10	09	
11	10	
12	11	
13	12	
14	13	
15	14	
16	D15	
17	ROMAD10	See pin nos. 3A01-3A09.
18	ROMAD09	
19	0V	
20	0V	

Table 8.6 TEST CONNECTOR FOR TESTTOOL (CARD C7E1B)



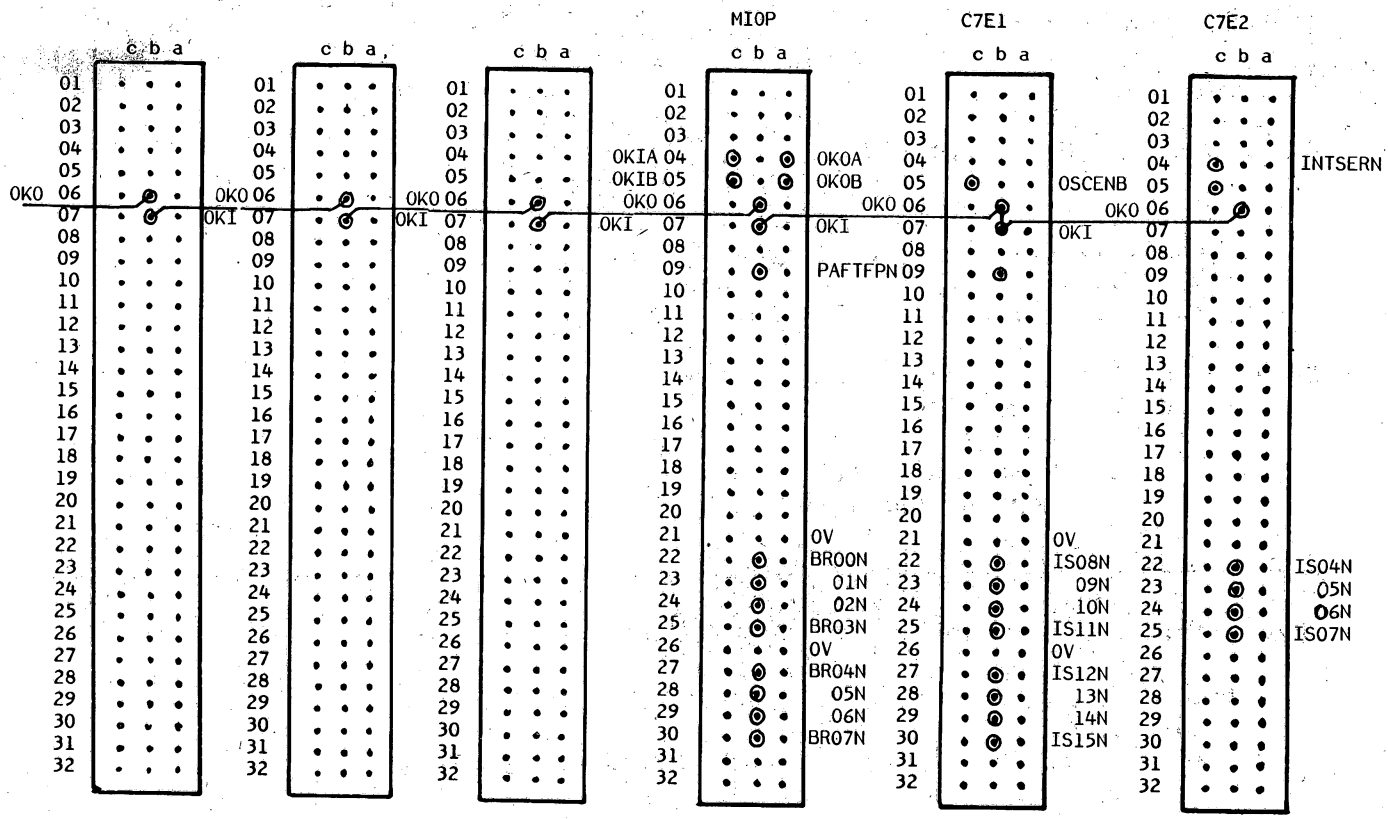
* SDPM= SERIAL DATA PANEL TO MASTER
RTCE= REAL TIME CLOCK ENABLE
RESETN= RESET FOR PANEL (RSLN LINE FROM POWER SUPPLY)
** SDMP= SERIAL DATA MASTER TO PANEL
LOCK= INHIBIT CONTROL PANEL FUNCTIONS EXCEPT "INT"
* SDPM: 1 STARTBIT 8 DATABITS 1 STOPBIT } 4800 BAUD
** SDMP: 1 STARTBIT 8 DATABITS 2 STOPBITS }

Figure 8.6 CABLE PANEL INTERFACE



102: COMMON RETURN
103: TRANSMITTED DATA
104: RECEIVED DATA
105: REQUEST TO SEND
106: READY FOR SENDING
107: DATA SET READY
108: DATA TERMINAL READY
133: READY FOR SENDING

Figure 8.7 CABLE V24 INTERFACE



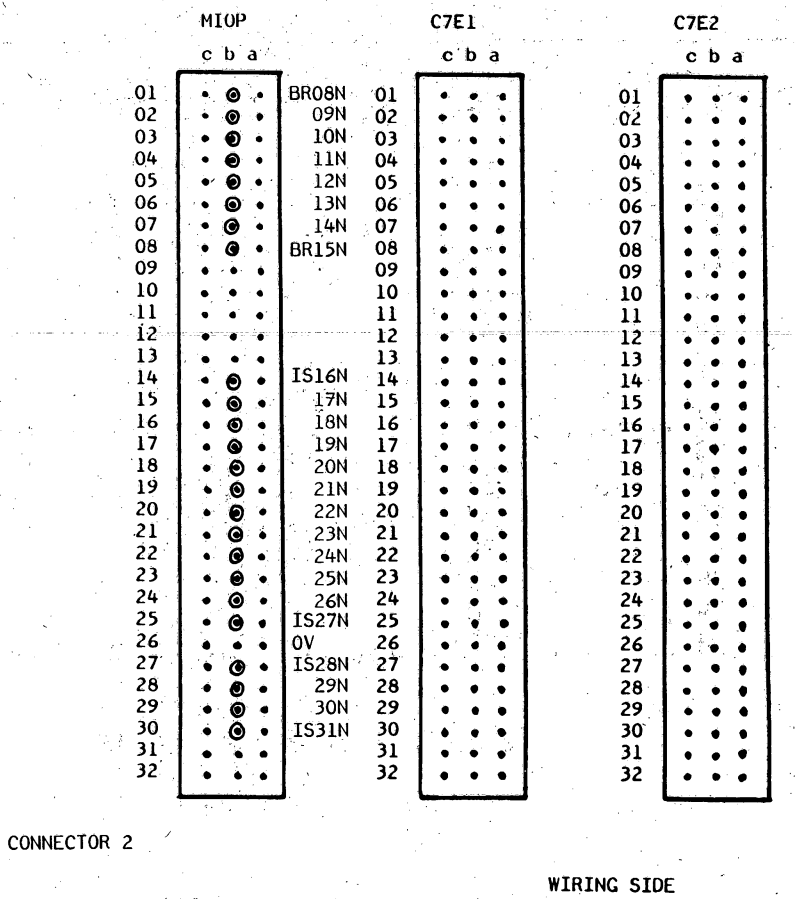


Figure 8.8 BREAK AND INTERRUPT WIRING PINS

INTERRUPT AND BREAK WIRING

Interrupt wiring: Break wiring:

CP7E2 pin:	CU	int. level:	Loc:	Pin:
1B22	.....	4	...	....
23	.....	5	...	....
24	.....	6	...	....
25	.....	7	...	....

Note: Fixed (internal) interrupts are:
level Ø - power fail/auto restart
1 - program int.
2 - Real Time Clock
3 - control panel

CP7E1 pin:	CU	int. level:	Loc.	Pin:
1B22	.....	8	...	....
23	.....	9	...	....
24	.....	1Ø	...	....
25	.....	11	...	....
27	.....	12	...	....
28	.....	13	...	....
29	.....	14	...	....
30	.....	15	...	....

MIOP pin:	CU	int. level:	Loc.	Pin:	pin:	CU	break level:	Loc	Pin
2B14	.....	16	...	....	1B22	.....	Ø (=A-Ø)	...	....
15	.....	17	...	....	23	.....	1 1	...	....
16	.....	18	...	....	24	.....	2 2	...	....
17	.....	19	...	....	25	.....	3 3	...	....
18	.....	2Ø	...	....	27	.....	4 4	...	....
19	.....	21	...	....	28	.....	5 5	...	....
2Ø	.....	22	...	....	29	.....	6 6	...	....
21	.....	23	...	....	3Ø	.....	7 7	...	....
22	.....	24	...	....	2BØ1	.....	8 (=B-Ø)	...	....
23	.....	25	...	....	2	.....	9 1	...	....
24	.....	26	...	....	3	.....	1Ø 2	...	....
25	.....	27	...	....	4	.....	11 3	...	....
27	.....	28	...	....	5	.....	12 4	...	....
28	.....	29	...	....	6	.....	13 5	...	....
29	.....	3Ø	...	....	7	.....	14 6	...	....
3Ø	.....	31	...	....	8	.....	15 7	...	....

Table 8.7 INTERRUPT AND BREAK WIRING LIST

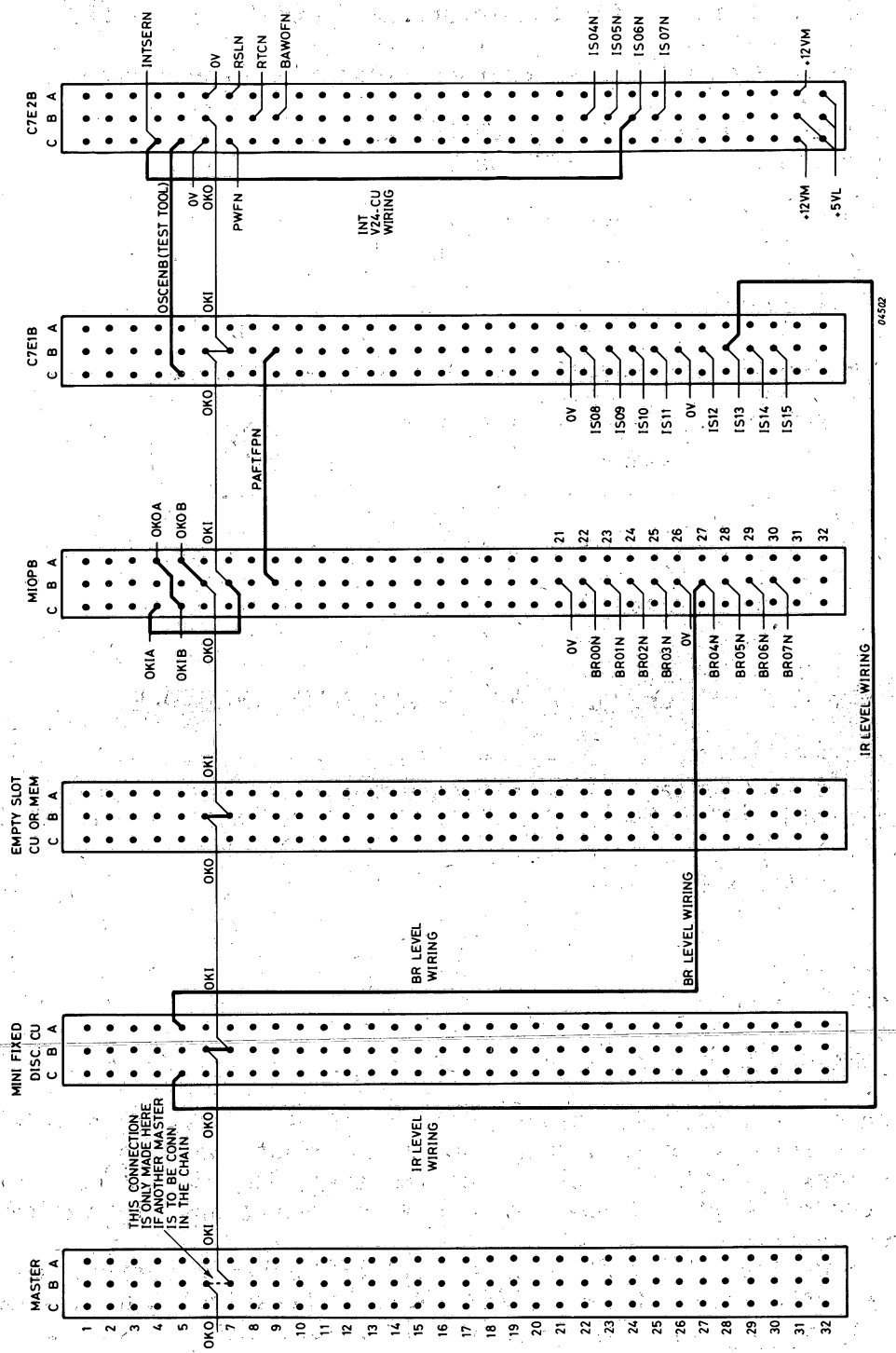


Figure 8.9 EXAMPLE OF BREAK, INTERRUPT, OKO-OKI WIRING

8.4 V24 CONTROL UNIT

8.4.1 GENERAL

An USART 8251 is used as interface between Console Typewriter and CU.
The type 8251 is also used for the interface Control Panel - CPU.

USART : Universal Synchronous Asynchronous Receiver Transmitter.

CTW : Selectable baudrate : 50 - 19.200 baud.
Panel : Fixed baudrate : 4800 baud.

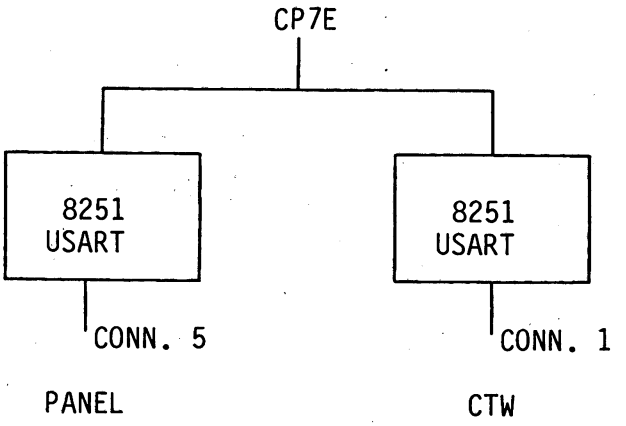


Figure 8.10 V24 CU AND PANEL INTERFACE

Straps : 5 straps total (baudrate and CT133)
CU address : /10 (fixed)
Int level : 6
HSi : see section 8.4.4

8.4.2 FACILITIES

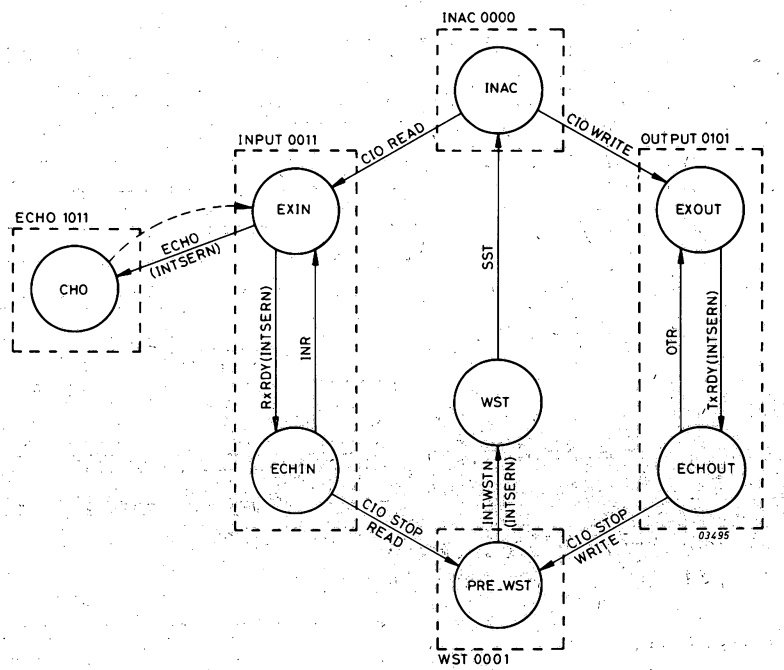
I/O DEVICE INTERFACE

* Connection to an I/O device having V24/28 interface according CCITT.
* Programmed channel with or without using interrupt handling.
* The CU is working in half duplex mode. However, the line to an I/O device may be a so called 4 wire connection. 4 Wire line connection allows echo mode (software selection).
* The V24 line 'Ready For Receiving' CT133/CT119 may control the throughput during the output mode. (Used by PER3100). To be selected by a strap.
* Used V24 lines: CT101, 102, 103, 104, 107, 108, 109, 133. CT 107/108 must be controlled by CU/CTW.
* Break detection in order to set control panel interrupt.
* Transfer rate 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 19.200 bits/sec.
* Character of line composed of:
  - 1 Start bit, rec. 1 or 2 Stop bits, trx. 2 Stop bits (normally).
  - 8 Data bits (no parity), or 7 data bits (with parity bit).
  - Software selectable (parity bit) (number of stop bits).
  - Device address /10 (non selectable)

PANEL INTERFACE

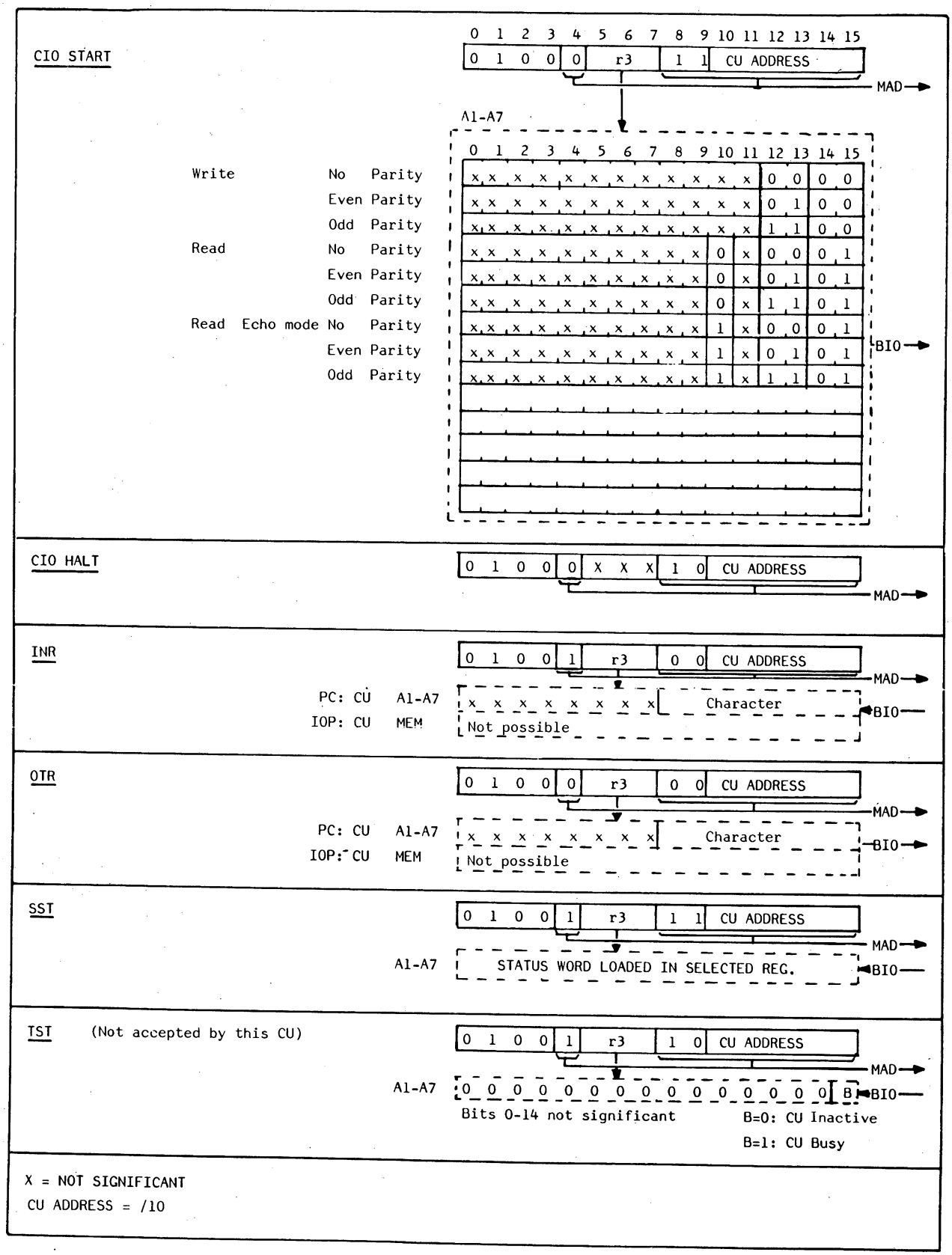
* A-synchronous interface according CCITT V28 for serial transmission and reception.
* Transfer rate 4800 bits/sec.
* Character on line composed of:
  - 1 Start bit, (at least) 2 Stop bits.
  - 8 Data bits
  - (no parity)

8.4.3 CONTROL UNIT STATES



Note: The states of the V24 Interface have a different significance at CPU level. Only ECHO, OUTPUT, INPUT are read by the V24 Status Indicators. When these bits are all zero, the CU is in the Inactive State.

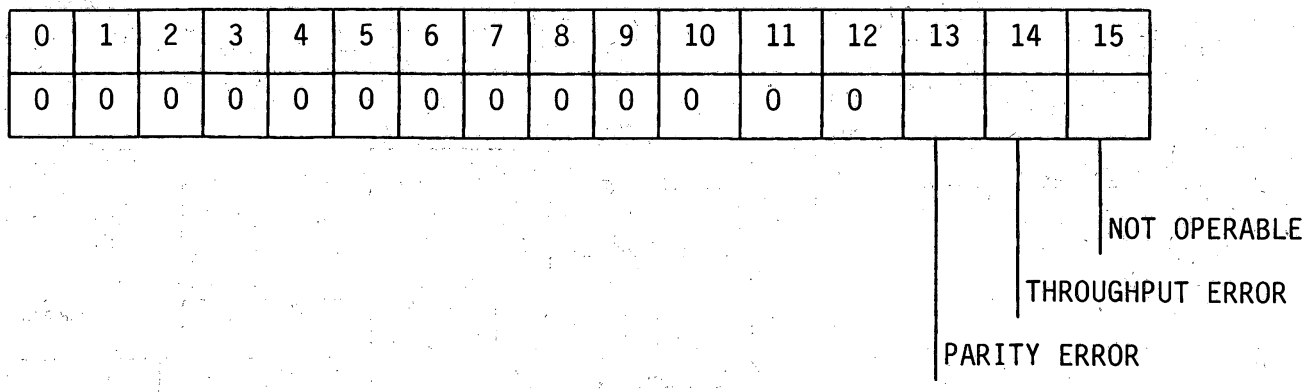
Figure 8.11 V24 INTERFACE STATES



Note: * Bit 14 = 1: only one stop bit (necessary if terminal operates with one stop bit)

Figure 8.12 INSTRUCTION-/COMMAND-WORD FORMATS

8.4.4.1 STATUS WORD



NOT OPERABLE

Bit 15 is set if the device is not connected or not operable.

THROUGHPUT ERROR

Bit 14 is set during input mode, if the interrupt is not yet answered by the CPU (INR) and the next input character arrives.

PARITY ERROR

Bit 13 is set when during input mode the received character has incorrect parity

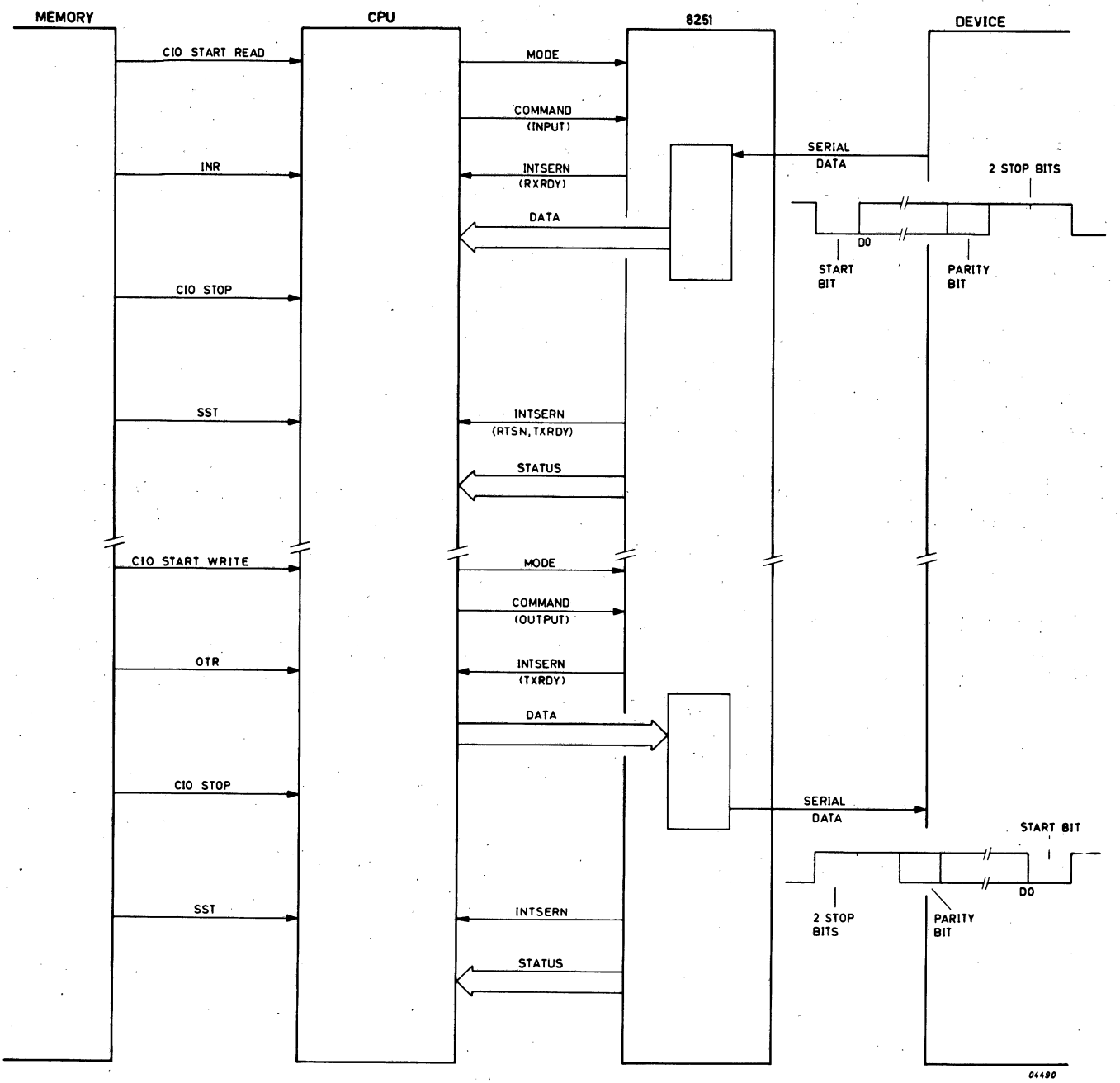


Figure 8.13 V24 PERIPHERAL INTERFACE DIALOGUES

8.5 CPU ARCHITECTURE CP7E (FIGURE 8.14)

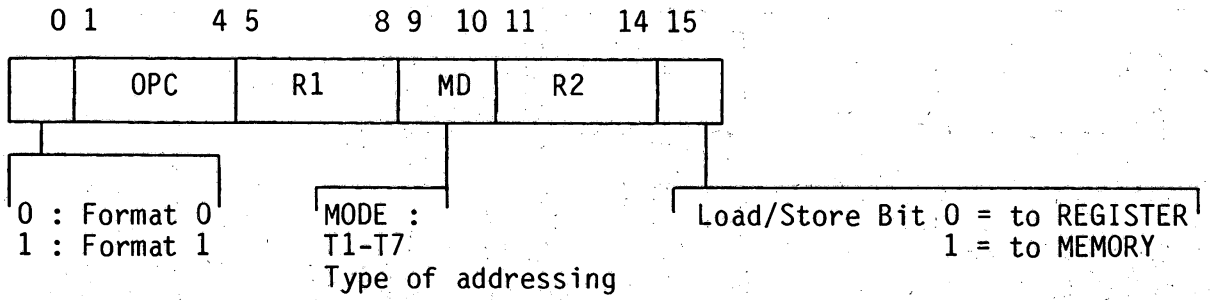
The CPU consists of three microprocessors linked together via internal busses, multiplexers etc. and by the microprogram.

4x MP 2901A: 4 bits microprocessor specially used for arithmetic operations. Contains SCRATCHPAD registers: A1-A15 (reg. 0 for internal use in microprogram).
Q register: used for SHIFT instructions.

4x MP 2932 : 4 bits microprocessor used for PROGRAM COUNTER, AO register.

1x MP 2910 : Used for microprogram control. Contains MICROPROGRAM COUNTER.
RTC COUNTER: for creating delay times, repeating certain actions a number of times.

Instruction format (on "D" bus and in K register):



MADE : MAD Extension 8 bits
PLACR : Programmable Logic Array controlling Condition Register
PSW : PLR Program Level Register
CR Condition Register
GF General Field
ALUX : 16-Bits Register (2x 8 bits)
Exchange of two bytes in one word: e.g. Character Exchange Instruction
PLAMAP : Decoding of instruction types and format 0 OPC's
PLAVEC : Decoding format 1 instructions : OPERATION CODE

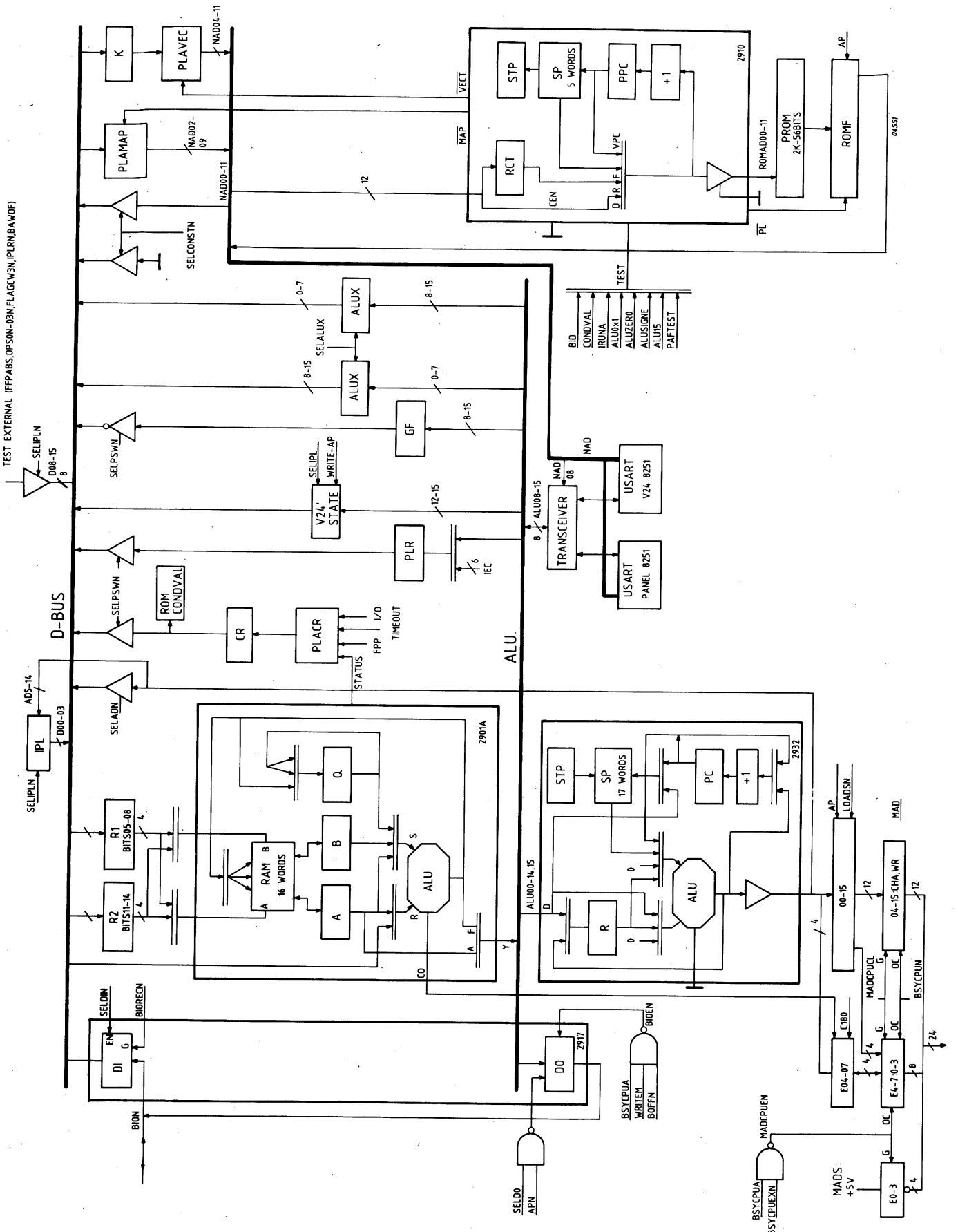
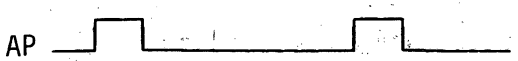


Figure 8.14 CPU BLOCKDIAGRAM

8.6 CPU TIMING

CPU TIMING

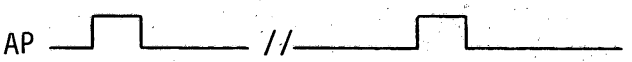


The sequensor has 3 fixed cycle lengths and a wait cycle.

CY 225 : 225 n/sec.
CY 270 : 270 n/sec.
CY 360 : 360 n/sec.

WAIT CYCLE

If a WAIT cycle is ordered the time between 2 AP pulses is undefined. This wait cycle is only effective when dealing with a bus transfer e.g. waiting for signal TSM which starts sequencer again.



WAIT CYCLE (max. 11.5 uS)

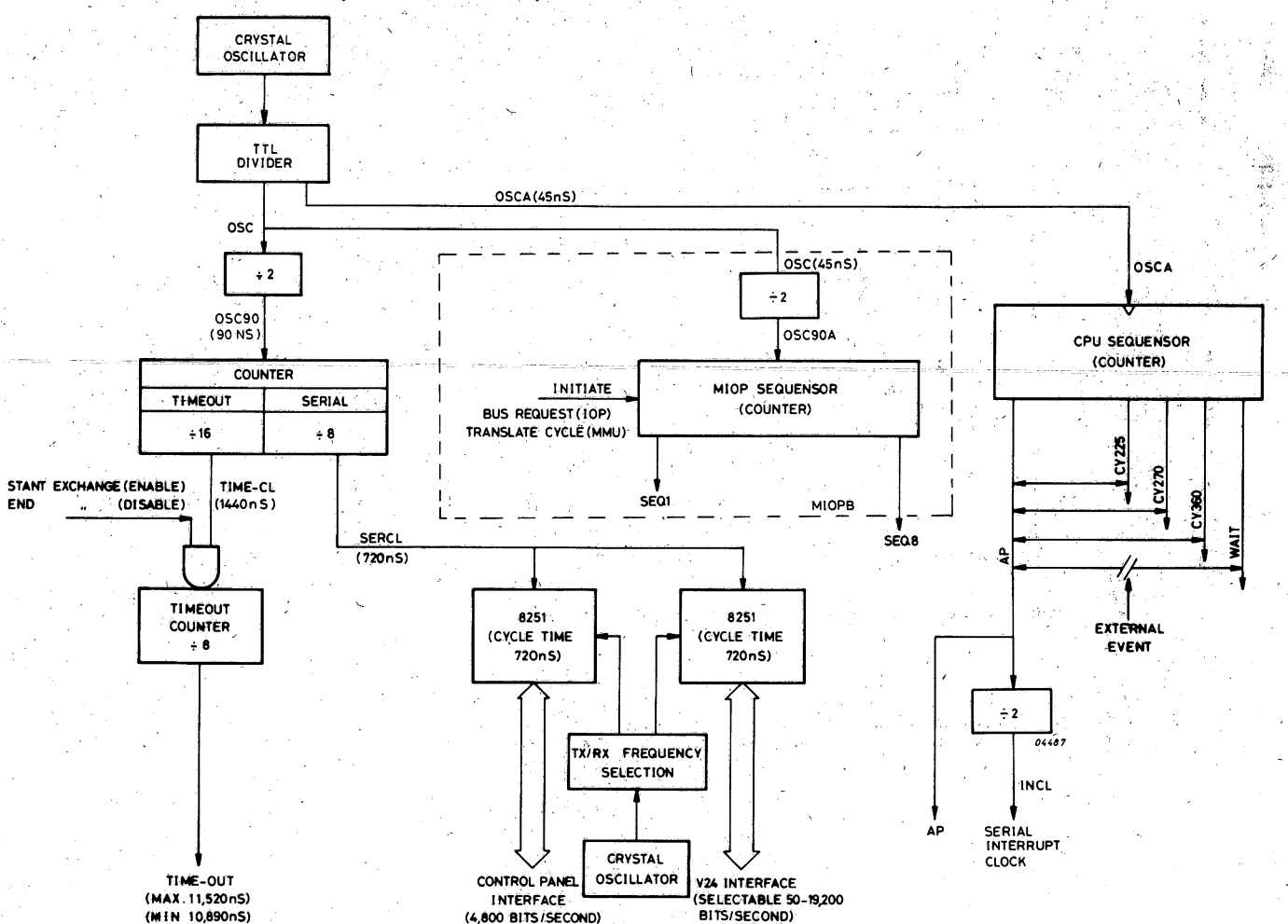


Figure 8.15 P857E SYSTEM CLOCKS

8.7 POWER SWITCH ON AND TEST

At switch-on a sequence of events takes place before the system is ready to go. This sequence of events may be considered as three separate phases.

. Phase 1 Automatic Test
. Phase 2 Microdiagnostic Test (only necessary if problems are expected)
. Phase 3 Load IPL (Initial Program Loader)

The hexadecimal codes of the HHCP and FRCP that are displayed after an event are indicated in the following flowcharts.

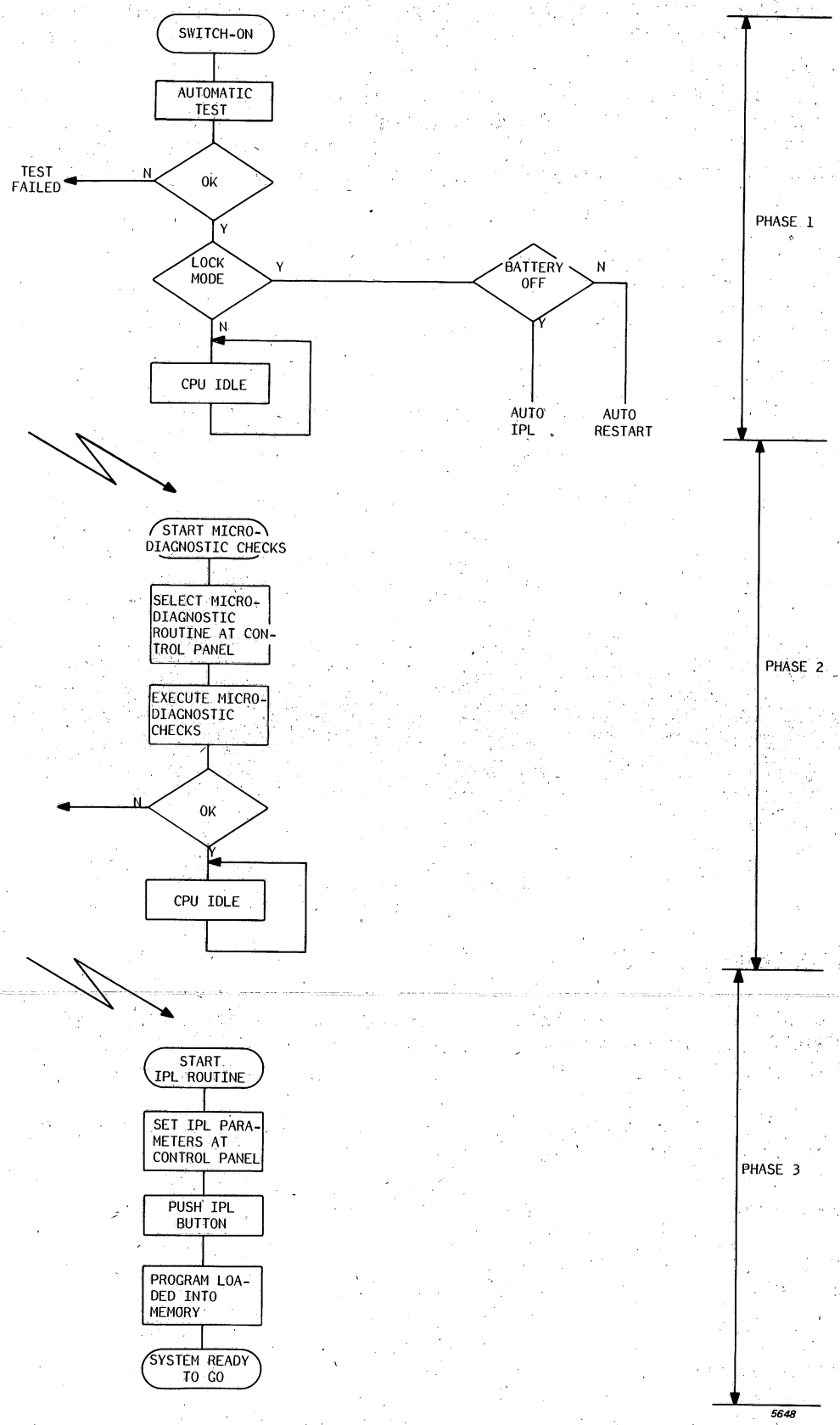


Figure 8.16 START PROCEDURE

8.7.1 AUTOMATIC TEST

An automatic test is executed at the power-on time. It tests the major part of the C.P.U., the Control Panel Interface, a part of the Control Panel itself and its cable. This test is terminated by displaying a code (FFFC) if the panel was not in LOCK state and if the test was O.K.

This automatic part of the test is of "go-no go" type. If the expected code is not displayed it is not possible to distinguish if the problem is due to the C.P.U., to the Control Panel or its cable and it is not possible to run further tests.

But if this first phase runs well and if displaying is possible and correct, in the second phase the C.P.U., C.U. and Memory failures could be distinguished from one another.

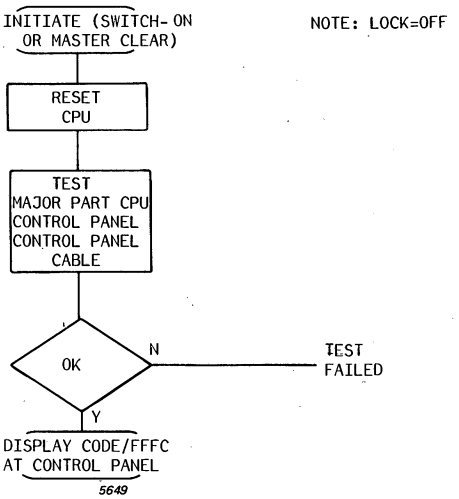


Figure 8.17 AUTOMATIC TEST

8.7.2 MICRODIAGNOSTIC TEST

The second phase is initialized by pressing the Ø and TEST push buttons on the Control Panel and it consists of the end of the C.P.U. test, RAM test (up to 32K), CPU-CU V24 (Address /10) dialogue test and MMU/IOP (MIOP) test.

At the end of this second phase, another code is displayed meaning either the correct end of test or an error.

These codes are:

C.P.U. error : Code 0001
BUS or CU error : Code 0002 or YY02
BUS or RAM error : Code XX03
O.K. : Code YY04
MIOP error or absent : Code YY10

XX = Most significant 8 bits of the memory address causing the error.
YY = Most significant 8 bits of the last memory address.

The operator can read the address causing the error in A1, and the contents of this address read by the CPU in A2.

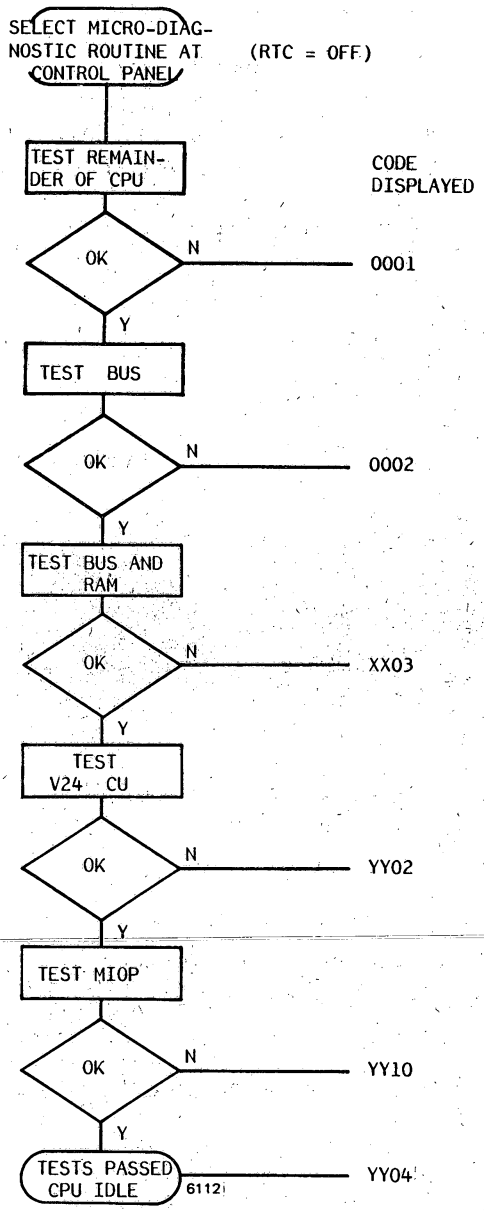


Figure 8.18 MICRODIAGNOSTIC TEST

8.8 SHORT DESCRIPTION OF TESTPROGRAMS

Testprogram CP 57 RE

Mem. size 8 Kw.
No output on CTW.
No power failure - or - RTC allowed.

Procedure:

. IPL

- Program stops on /0300 = restart address
- MCL, RUN
- Program loops continuously. Address /024A contains the number of passes.
- Error: program stops. Halt address indicates faulty instruction in listing.

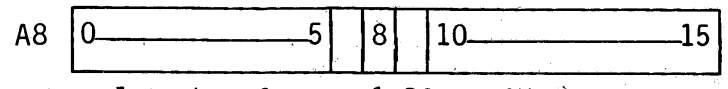
One complete CPU test lasts 2 - 4 seconds.

1. IPL

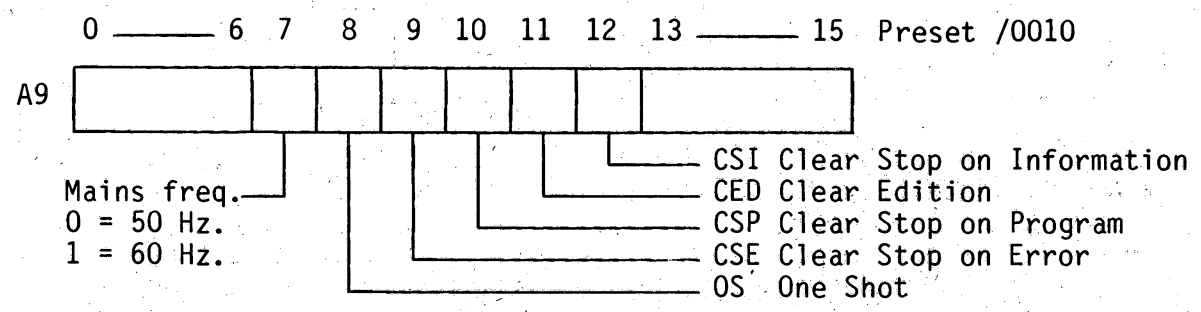
   Program stops at /700 = restart address and normal end.

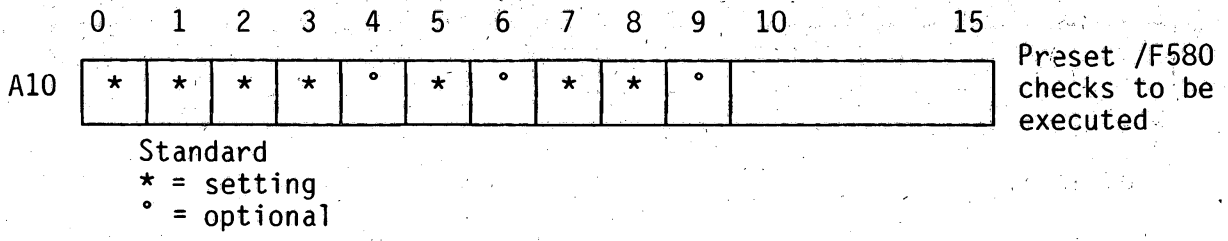
2. Switch on RTC (PF/AR also possible).

3.



Standard Levels
P854
/1890
DA /10
INT.L. /6





4. Clear bit 11 of A9 (check no written on DA/10).
   Depress MC, RUN
   Interrupts return to address /700
   Error stop /5F0
   Restart after power off /6EE

   Special operator actions:
   IF0001 type in a character within 10 seconds
   IF0003 type in characters begin with LF, CR, end with $
   IF0005 type in 2 characters within 3 seconds

For more information see official description of testprogram.

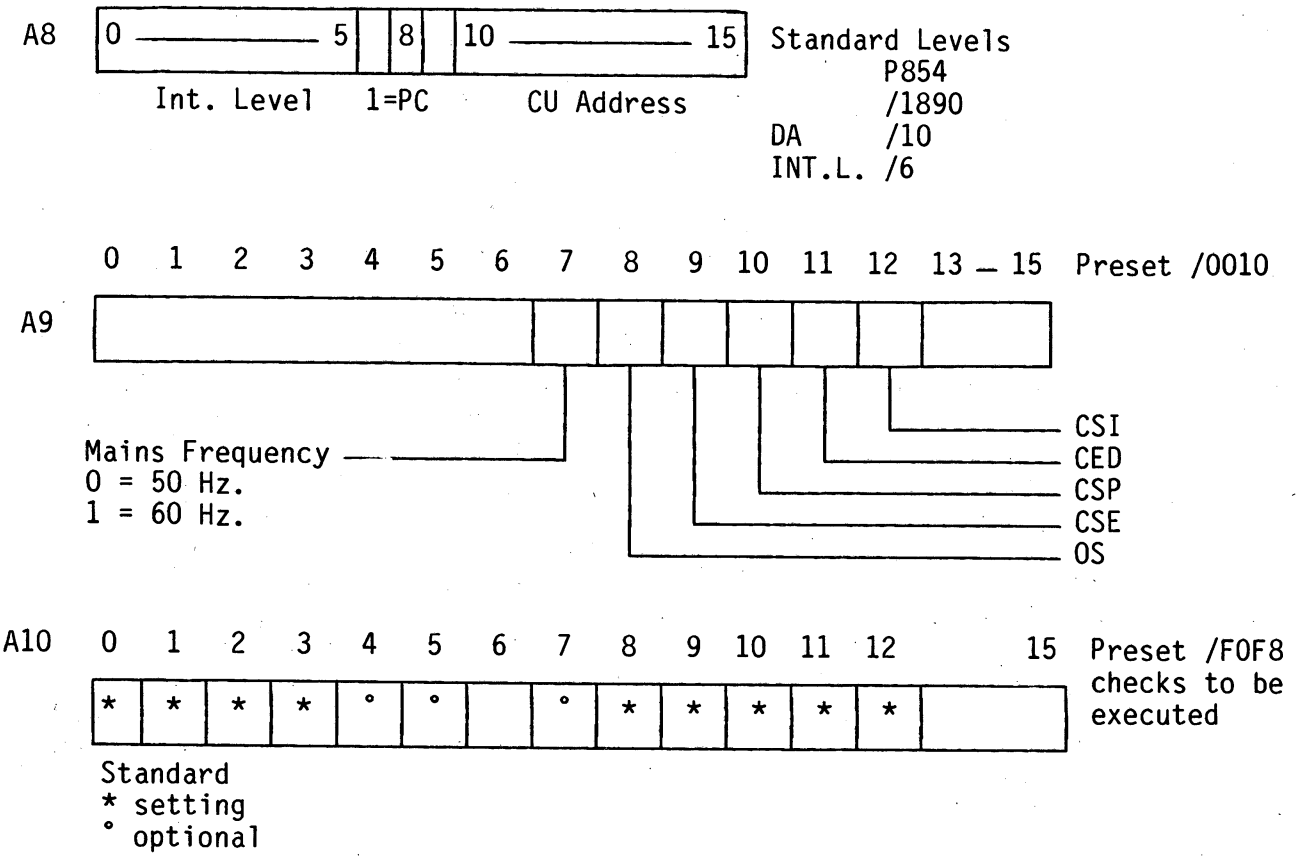
TEST PROGRAM BBDISP 8K for P817

1. IPL

   Program stops at /700 = restart address and normal end.

2. Switch on RTC (PF/AR also possible).

3.



4. Clear bit 11 of A9 (check no written on DA/10).
   Depress MC, RUN

   Error stop /5F0
   Restart after power off /6EE
   Interrupts return to /700
   Special operator actions:
   IF0001 type in a character within 10 seconds
   IF0003 type in characters begin with LF, CR, end with $.

For more information see official description of testprogram.

8.9 SHORT ROUTINES

ASR, PTS 3100 AND DISPLAY

These peripherals and their CU's can be checked with the aid of two small programs called Line, and Echo, if the standard test program either cannot be loaded or if it will not run.

PROGRAM LINE

MEMORY ADDRESS	DATE	PROGRAM INSTRUCTION		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	START	HLT	
0086	20BF		INH	
0088	0200		LDK	A2, 0
008A	4BD0		SST	A3,/10
008C	42D0		CIO	A2,1,/10
008E	5C04		RB(NA)	* -2
0090	8520	OUTCR	LDKL	A5,/0A0D
0092	0A0D			
0094	4510	OUT	OTR	A5,0,/10
0096	5C04		RB(NA)	* -2
0098	3D68		SRL	A5,8
009A	5C08		RB(NZ)	OUT
009C	4610	OUTCH	OTR	A6,0,/10
009E	5C04		RB(NA)	* -2
00A0	1201		ADK	A2,1
00A2	EA1C		CWR	A2,A7
00A4	5C0A		RB(NE)	OUTCH
00A6	0200		LDK	A2,0
00A8	5F1A		RB	OUTCR

* Load the ASCII character in register A6
* Load the number of times you wish the character to be repeated into register 7
* Load the start address of the program into register A0 (/0086).
* Push the MCL and RUN button

PROGRAM ECHO

MEMORY ADDRESS	DATA	PROGRAM INSTRUCTIONS		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	START	HLT	
0086	20BF		INH	
0088	0221	IN	LDK	A2,/21
008A	42D0		CIO	A2,1,/10
008C	5C04		RB(NA)	* -2
008E	4B10		INR	A3,0,/10
0090	5C04		RB(NA)	* -2
0092	4290		CIO	A2,0,/10
0094	4CD0		SST	A4,/10
0096	5C04		RB(NA)	* -2
0098	0200		LDK	A2,0
009A	42D0		CIO	A2,1,/10
009C	5C04		RB(NA)	* -2
009E	4310		OTR	A3,0,/10
00A0	5C04		RB(NA)	* -2
00A2	4290		CIO	A2,0,/10
00A4	4CD0		SST	A4,/10
00A6	5C04		RB)NA)	* -2
00A8	5F24		RB	IN

Program Echo:

Once loaded and started any input character from the keyboard will be printed, displayed or executed on the device.

9 INPUT/OUTPUT PROCESSOR P843-120 (IOPZR) P857E (MIOP)

SECTION	9.1	IOP IDENTIFICATION	PAGE 9-2
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	9.3	INTERFACE CONNECTIONS IOPZR	9-4
	9.4	HARDWARE-SOFTWARE INTERFACE DETAILS	9-5

LIST OF ILLUSTRATIONS

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9.1 IOP IDENTIFICATIONS

- Type No.: P843-120 (IOPZR)
  P857E (MIOP, see also CPU chapter 8)

- Power Consumption: +5Volt
  IOPZR : 2.75Amp.

- 12NC code on the sticker on the board.
  IOPZR: 5111 199 6670x (5322 216 25446)
  X = modification level.

9.2 INSTALLATION DETAILS IOPZR

U-links on IOPZR card to select:
- IOP address (MIOP card, if present, always is IOP address 0 and 1 for IOP-A and B).
- First or second level of priority for individual CU break requests (signal ERQN)
- Time delay for timing signal TSMN.

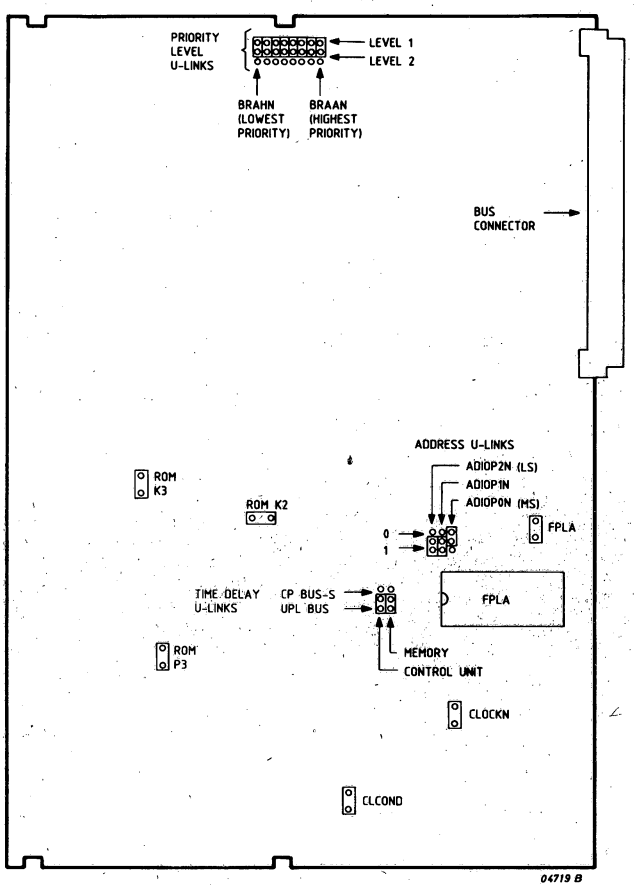


Figure 9.1 U-LINK SETTING IOPZR

Priority level U-links shown for all CU's at level 1. Address U-links shown for IOP address 3.
Test U-links (ROM K3, ROM K2, ROM P3, FPLA, CLOCKN, CLCOND) must be fitted when IOP is under normal operation.
- If both types of CU's (UPL and GP) are used with IOP, the CU-strap must be set in GP position (simular for memory strap).

9.3 INTERFACE CONNECTIONS IOPZR

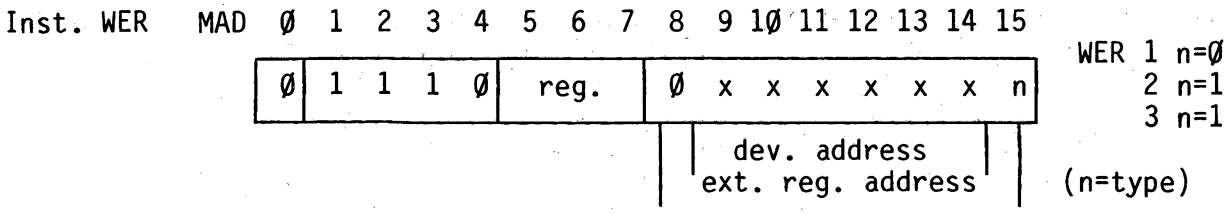
The IOP communicates with the rest of the system via the UPL-bus. Break connections from the individual CU's are made by jump leads on the backpanel.
For master selection on the bus, OKO-OKI wiring must be present on the backpanel.

UPL backpanel Signal:	Pin:
OKI	1BØ7
OKO	1BØ6
BRØØN	1B22
BRØ1N	1B23
BRØ2N	1B24
BRØ3N	1B25
BRØ4N	1B27
BRØ5N	1B28
BRØ6N	1B29
BRØ7N	1B3Ø

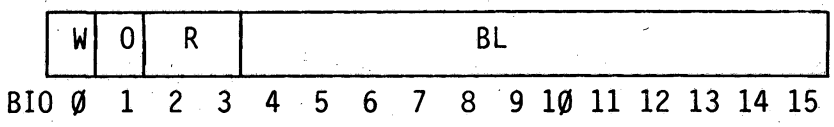
BUS signal ERQN (Pin 1B01) is used for second level Break Priorities, only on IOPZR and not on MIOP. (see chapter 1; BUS ALLOCATION).

9.4 HARDWARE-SOFTWARE INTERFACE DETAILS

IOP Instructions: (MIOP, IOPZR):

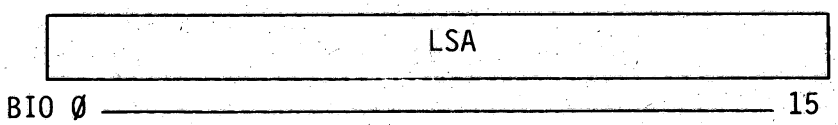


The 3 WER instructions must be programmed in a fixed sequence, the 3 following parameters being always sent in the same order:
Parameter 1: (WER 1 type Ø)



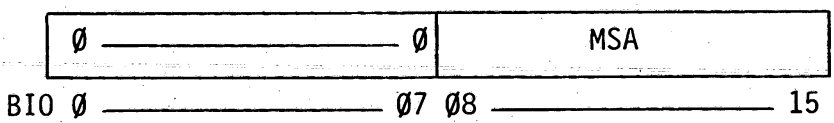
W : Word transfer indicator - if zero the transfer is 8 bit character oriented.
O : Output mode. When 1 the exchange is in output mode from the memory to the Control Unit.
R : Address bits for MADE 6,7 if no 3rd WER (memory not bigger than 256 kbytes).
BL: 12 bit length. Depending on the W indicator value, the block length is expressed either in number of words or in number of characters. If BL=Ø the effective length is 2^{12} words (or bytes).

Parameter 2: (WER 2 type 1)

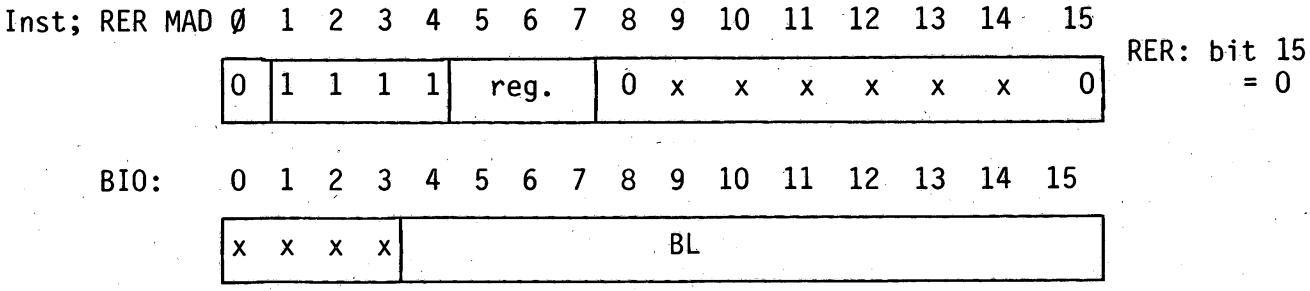


LSA: Least significant bits of the memory start address of the block to be read or written (to MAD Ø-15). A block can start at any byte boundary.

Parameter 3: (WER 3 type 1)



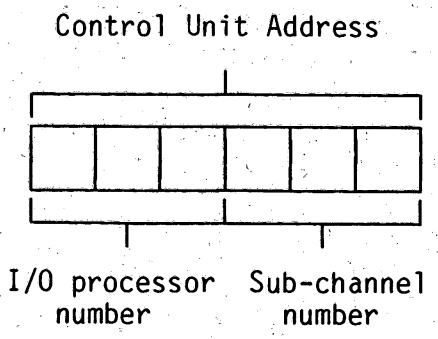
MSA: Most significant bits of the memory start address of the block (to MADE Ø-7). Only necessary if memory bigger than 256K bytes.



The remaining blocklength is sent to the specified register. RER is only allowed when the I/O transfer is finished.

RELATIONSHIP BETWEEN BREAK SIGNAL AND CONTROL UNIT ADDRESS

An I/O processor is coded with a 3-bit number which may range from 0 to 7 (coded by straps on the I/O processor) and each of the 8 subchannels associated with an I/O processor is also coded with a 3-bit number from 0 to 7.
The combined 6-bit number gives the address of the peripheral control unit as shown below:



This address is used by the WER instruction to load the 3 control words into the working register of the I/O processor.

The 8 incoming break request signals BR00 to BR07 to each I/O processor corresponds to each subchannel in the I/O processor as follows:

BR00N corresponds to subchannel 0
BR07N corresponds to subchannel 7

BR00N has the highest priority and BR07N lowest.

10 MEMORY MODULES

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10.1 P851-004/005 MOS MEMORY

10.1.1 IDENTIFICATIONS

- Type number : P851-004 (4K16)
  P851-005 (8K16)
- Testprogram : BRAM (from 4KW-16KW)

- Power consumption: (both types)

	OPERATING		NON OPERATING	
	P851 - 004		P851-005	
+5VL	0.4A	0.4A	0.4A	0.4A
+5VM	0.4A	0.4A	0.4A	0.4A
+12VM	0.3A	0.05A	0.3A	0.07A

Table 10.1 POWER CONSUMPTION P851-004/005

- 12NC code one the sticker on the board
  P851-004: 5111 199 7296x (5322 216 25123)
  P851-005: 5111 199 7297x (5322 216 25124)

X - modification level

- Performance Data

Max access time;

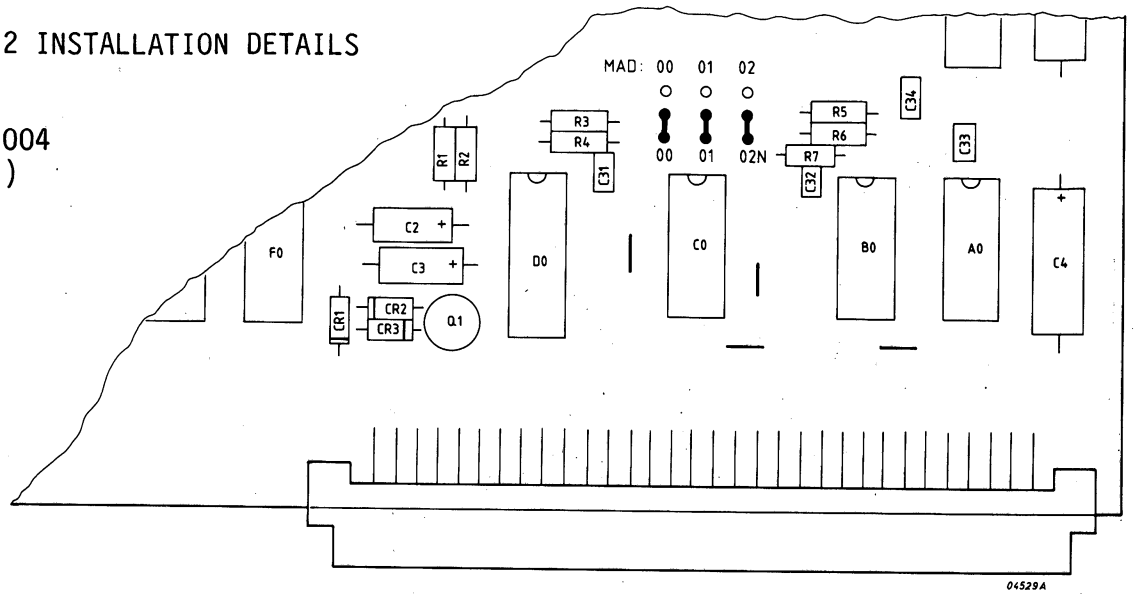
P851-004: 540 nSec (GPBS)
P851-005: 480 nSec (GPBS)

To be used on P851 and P853 systems.

WARNING
Take care of MOS HANDLING PROCEDURE

10.1.2 INSTALLATION DETAILS

P851-004
(4K16)



P851-005
(8K16)

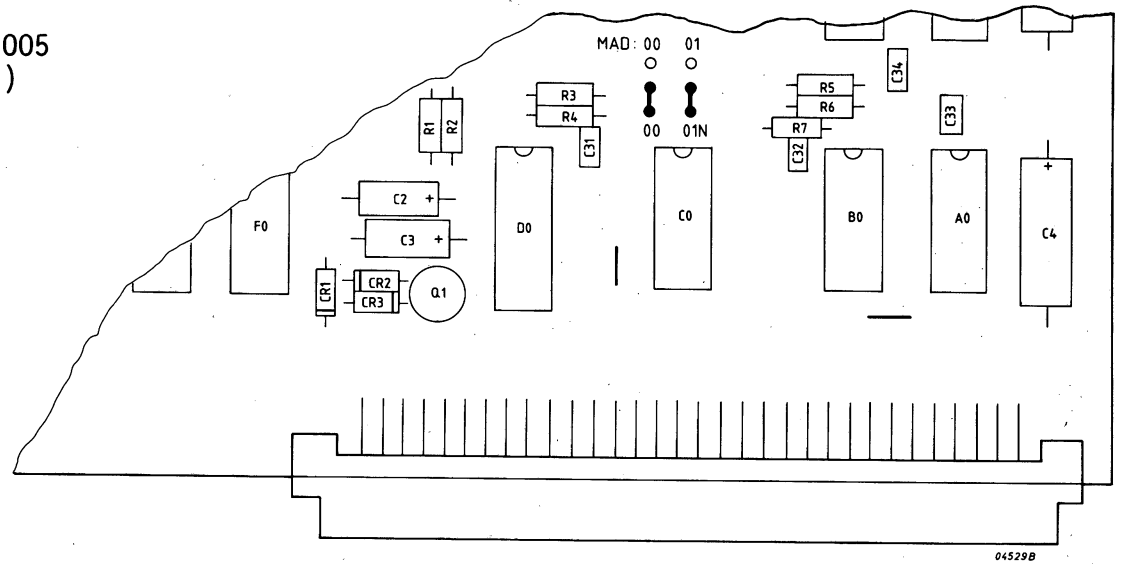


Figure 10.1 U-LINK SETTINNG P851-004/005

	4K MODULE								8K MODULE			
No of Words	MAD00 M00	M00N	MAD01 M01	M01N	MAD02 M02	M02N	MAD00 M00	M00N	MAD00 M00	M00N	MAD01 M01	M01N
0-4K		X		X		X						
4-8K		X		X	X							
8-12K		X	X			X						
12-16K		X	X		X							
16-20K	X			X		X						
20-24K	X			X	X							
24-28K	X		X			X						
28-32K	X		X		X							
0- 8K										X		X
8-16K										X	X	
16-24K									X			X
24-32K									X		X	

Table 10.2 U-LINK SETTING P851-004/005

10.2 P844-004/016 CMOS MEMORY (CM8)

10.2.1 IDENTIFICATIONS

- Type number : P844-004 (2K16)
  P844-016 (8K16)

- Testprogram : BRAM (from 4KW-32KW)

- Power consumption:

	2K	8K
+5VL	1.1A (typ)	1.25A (typ)
+5VM	0.03A (typ)	0.03A (typ)
+12VM	0.25mA (max)	1mA (max)

Table 10.3 POWER CONSUMPTION P844-004/016

-12NC code on the sticker on the board:

P844-004: 5111 199 6387x
P844-016: 5111 199 6788x

X = modification level

- Performance Data

The minimum cycle time of the Memory is = less than 750nS.
For UPL Mode the access time is 580nS (typ), 640nS (max).

- Facilities

The CM8 (CMOS Memory 8K) is a 16-bit RAM Memory Module intended to be used as the main memory for GPBS (P851) or UPL Bus (P853) System. The principle facilities available with this card are as follows:

- Two operating cycles, read and write.
  Word or character mode for both read and write cycles.
- The card may be depopulated so that the user has a memory module of either 2K, 4K or 8K words.
- Data retention to enable a memory card to be transferred from one computer to another. This facility is enabled with the SAVE Switch.
- Rechargeable battery mounted on the card.
- Memory protection in the event of a power failure.

WARNING
Take care of MOS HANDLING PROCEDURE

10.2.2 INSTALLATION DETAILS

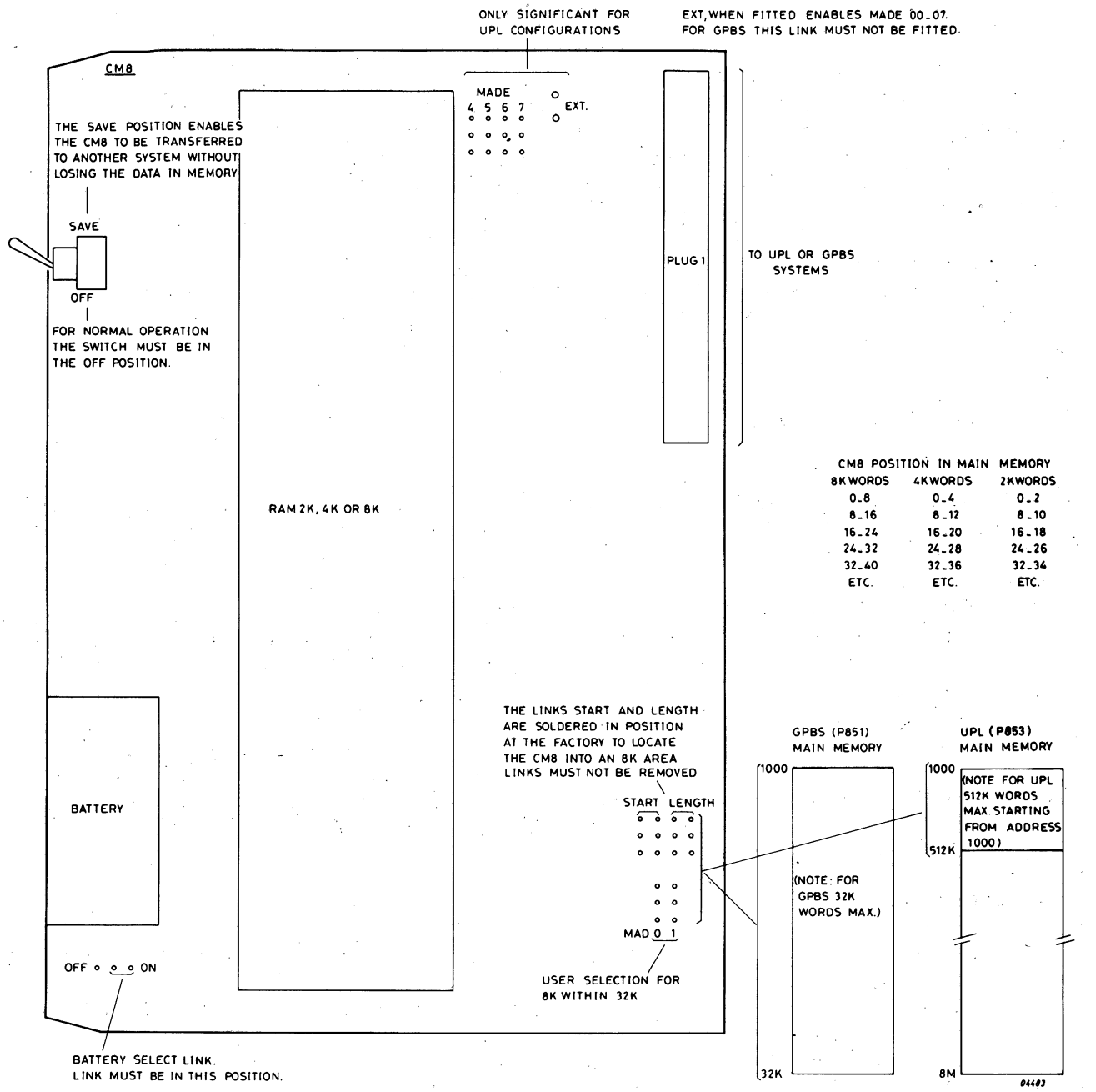


Figure 10.2 U-LINK SETTING P844-004/016

U-LINK SETTINGS

The location of the U-links is shown in Figure 10.2 and their function is as follows:

- BAT - There are 2 positions for this link: ON connects the Battery to the Memory and OFF disconnects the Battery.
- MAD 00, 01 and MADE4, E5, E6, E7 - These links are used to position the CM8 in the System Memory. (MADE not significant for GPBS or P853).
- START, LENGTH - These links are not selectable by the user; they are soldered in position at the factory and must not be removed.
- EXT - When fitted enables MADE 0-7 to be taken into account by the CM8 logic; when not fitted MADE 0-7 are inhibited (only fitted for UPL configurations with MMU).

A two position battery switch enables the user to select either SAVE or OFF. In the SAVE position the card may be transferred to another system without loosing the data. For normal operation the Switch must be in the OFF position.

BATTERY CHARACTERISTICS

Nominal voltage	- 2.4V
Capacity	- 100 mA/H
Permanent charging current (max)	- 3mA at 0°C
Permanent charging current (max)	- 5mA between 10 to 50°C
Retention Time	- After a complete charge at +20°C: 2KW memory: 17 days 8KW memory: 5 days
Charging time	- Less than 48 hours

Table 10.4 BATTERY CHARACTERISTICS P844-004/016

10.3 P851-010 PROM/EPROM MEMORY (PRO16)

10.3.1 IDENTIFICATIONS

- Type number: P851-010
- Power consumption:

	Module	Voltage	Power Consumption Standby	Operating TYPICAL	tolerance
	ØK	+5V	700mA	700mA	+5%
EPROM 2716	8KB	"	760mA	860mA	"
	16KB	"	820mA	920mA	"
	24KB	"	880mA	980mA	"
	32KB	"	940mA	1 040mA	"
PROM 82S191	8KB	"	1 220mA	1 220mA	+5%
	16KB	"	1 740mA	1 740mA	"
	24KB	"	2 260mA	2 260mA	"
	32KB	"	2 780mA	2 780mA	"

Table 10.5 POWER CONSUMPTION P851-010

An extra +25V generated on the program tool is needed during programming mode. EPROM and PROM devices can not be mixed on the same module, because of pin incompatibility.

- 12NC code on the sticker on the board:
  P851-010: 5111 199 6814x

X = modification level (board without PROM's)

- Performance Data

The capacity of the module is 16K words. The capacity can be reduced to 12-8-4k words.

The module can be used in a 32k word system (P851 system), or in a 8M word system (UPL).
In the latter case the preselection done by U-links is limited to the first 1M byte area of the memory.

Cycle time:

		Tcycle (typ) in ns.	Tcycle (Max) in ns.
P 851 Mode	EPROM (2716)	760 ns.	910 ns.
	PROM 82S191	360 ns.	510 ns.
UPL Mode	EPROM (2716)	810 ns.	970 ns.
	PROM 82S191	410 ns.	570 ns.

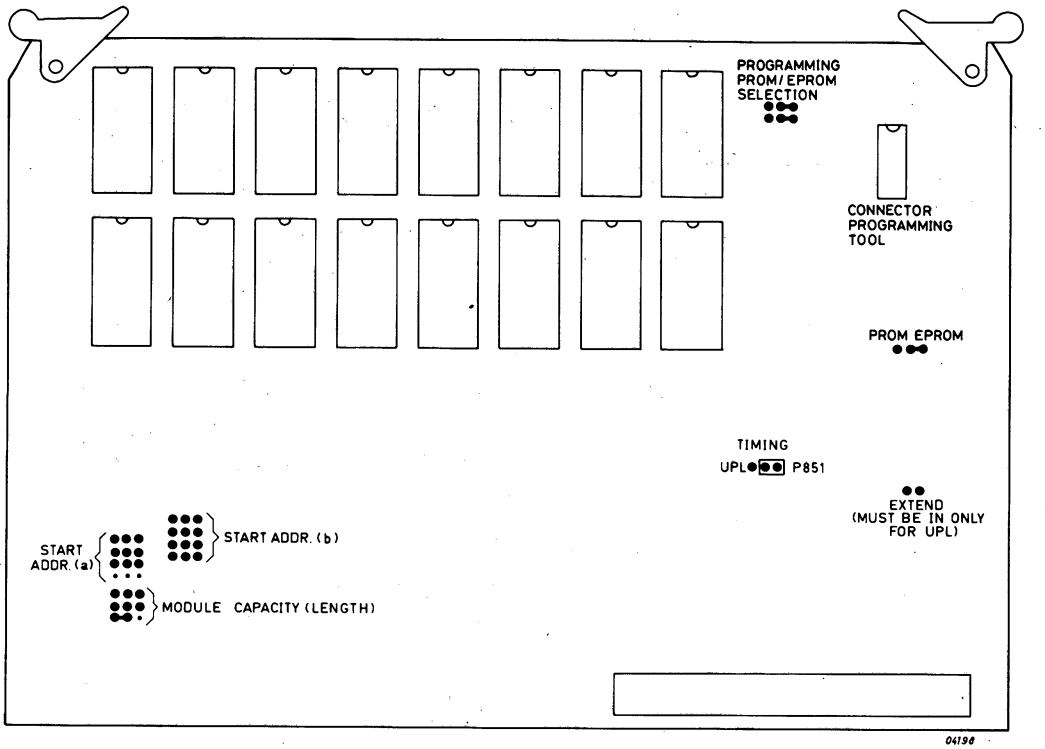
Table 10.6 CYCLE TIME P851-010

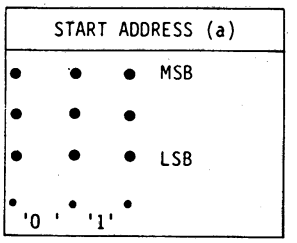
Access time:

		Tacc (typ) in ns.	Tacc (Max) in ns.
P 851 Mode	EPROM (2716)	650 ns.	765 ns.
	PROM 82S191	250 ns.	365 ns.
UPL Mode	EPROM (2716)	710 ns.	825 ns.
	PROM 82S191	310 ns.	425 ns.

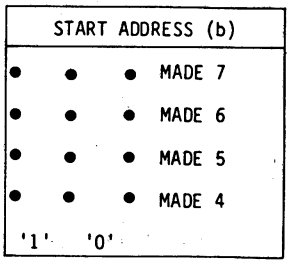
Table 10.7 ACCESS TIME P851-010

10.3.2 INSTALLATION DETAILS



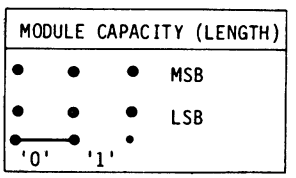


START ADDRESS (a)	
MSB → LSB	MEM. ADDR.
0 0 0	/0 0 0 0
0 0 1	/1 0 0 0
0 1 0	/2 0 0 0
0 1 1	/3 0 0 0
1 0 0	/4 0 0 0
1 0 1	/8 0 0 0
1 1 0	/A 0 0 0
1 1 1	/C 0 0 0



NOTE: NOT USED ON P851

START ADDRESS (b)	
MADE4→MADE7	MEM. ADDR.
0 0 0 0	/0 0 0 0 0
0 0 0 1	/1 0 0 0 0
0 0 1 0	/2 0 0 0 0
0 0 1 1	/3 0 0 0 0
0 1 0 0	/4 0 0 0 0
0 1 0 1	/5 0 0 0 0
0 1 1 0	/6 0 0 0 0
0 1 1 1	/7 0 0 0 0
1 0 0 0	/8 0 0 0 0
1 0 0 1	/9 0 0 0 0
1 0 1 0	/A 0 0 0 0
1 0 1 1	/B 0 0 0 0
1 1 0 0	/C 0 0 0 0
1 1 0 1	/D 0 0 0 0
1 1 1 0	/E 0 0 0 0
1 1 1 1	/F 0 0 0 0



MODULE CAPACITY (LENGTH)	
MSB → LSB	LENGTH IN K WORDS
0 0	4
0 1	8
1 0	12
1 1	16

FIELD SELECTION: START ADDR. (A + B) (FOR P851 B = 0 ALWAYS)

Figure 10.3 U-LINK SETTING P851-010

10.3.3 APLLICATION NOTES

PROGRAMMING TOOL (P843-012)

Programming of the EPROM modules can be done on the system with the programming tool. The Slave Control Unit Programming Tool has to be placed between the system BUS and the EPROM module. A small cable is connected for the +25V and the transfer of certain commands.

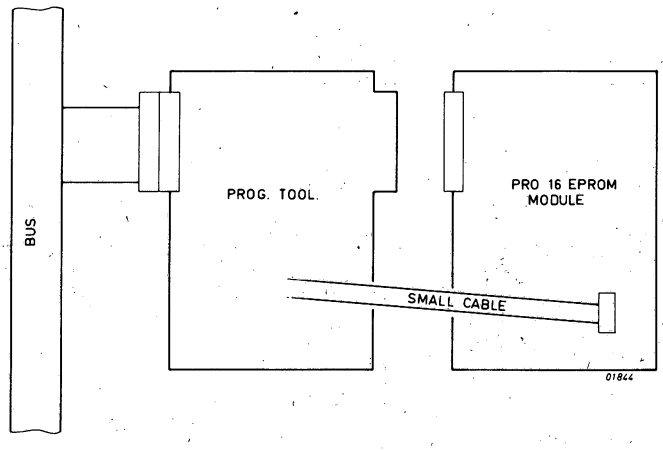


Figure 10.4 PROGRAMMING TOOL CONNECTION

Pin number	Signal name	Pin number	Signal name
01	0V	08	0V
02	DEVEN	09	DEVEN
03	IPGMEN	10	IPGMEN
04	OE-N	11	OE-N
05		12	
06	25V	13	25V
07		14	

DEVEN Level "0" Enables the BIO Gates for input from the Bus.

IPGMEN Level "1" Enables selection of the proper pair of EPROM's to program.

OE-N Level "0" Inhibits output of the EPROM during programming.

Table 10.8 PRGRAMMING TOOL CONNECTOR (14 PIN SOCKET)

10.4 P851-016/017 GMB1 MOS MEMORY

10.4.1 IDENTIFICATIONS

- Type number: P851-016 (16K16)
  P851-017 (32K16)

- Test programs: BRAM (from 4KW-32KW)
  : BRAM (from 32KW-512KW)

- Power consumption:

Memory Module	Voltage	Power Supply Operational Typical	Max	Battery Back-up Stand-by Typical	Max	Tolerance
16K	+5VL	430mA	530mA	0	0	+5%
32K		430mA	530mA	0	0	
16K	+5VM	400mA	500mA	400mA	500mA	+5%
32K		400mA	500mA	400mA	500mA	
16K	+12VM	340mA	510mA	60mA	90mA	+10%
32K		360mA	550mA	90mA	130mA	

Table 10.9 POWER CONSUMPTION P851-016/017

- 12 NC code on the sticker on the board:

  P851-016 : 5122 194 2396x (5322 216 25412)
  P851-017 : 5122 194 2394x (5322 216 25413)

X = modification level

Performance

	Cycle time:		Access time:	
	Tcycle (typ)	Tcycle (Max)	Tacc (typ)	Tacc (Max)
P851 Mode	in nS	in nS	in nS	in nS
UPL Mode	531	565	495	555
	595	630	575	645

Table 10.10 CYCLE, ACCESS TIME P851-016/017

WARNING
Take care of MOS HANDLING PROCEDURE

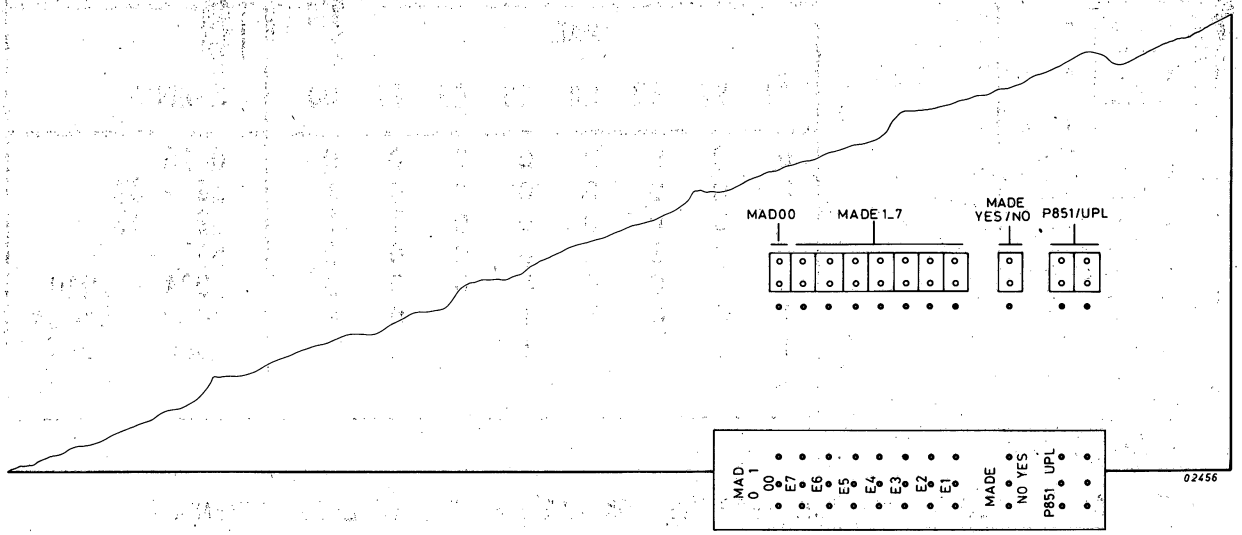
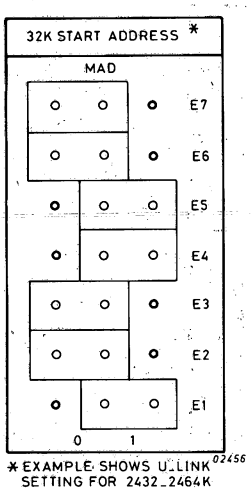


Figure 10.5 U-LINK SETTING P851-016/017

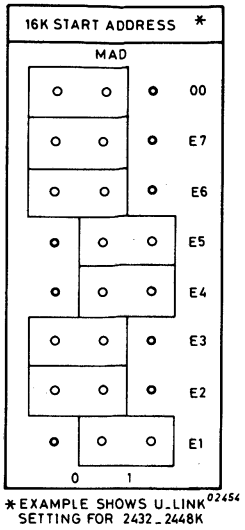
Next U-link settings only important when more than 1 memory card connected to the system (Multi Card Link: Yes)

32K START ADDRESS*



EXAMPLES OF START ADDRESSES							
MAD							
E1	E2	E3	E4	E5	E6	E7	K-WORD
0	0	0	0	0	0	0	0 - 32
0	0	0	0	0	0	1	32 - 64
0	0	1	0	0	0	0	512 - 544
0	1	0	0	0	0	0	1024 - 1056
1	0	0	1	1	0	0	2432 - 2464*
1	1	1	1	1	1	1	4064 - 4096
MSB						LSB	

Figure 10.6 U-LINK SETTING 32K MODULE-MULTIPLE CARD MEMORY



EXAMPLES OF START ADDRESSES								
MAD								
E1	E2	E3	E4	E5	E6	E7	00	K-WORD
0	0	0	0	0	0	0	0	0 16
0	0	0	0	0	0	0	1	16 - 32
0	0	0	0	0	0	1	1	32 - 48
0	0	1	0	0	0	0	0	512 - 528
0	1	0	0	0	0	0	0	1024 - 1040
1	0	0	1	1	0	0	0	2432 - 2448*
1	1	1	1	1	1	1	1	4080 - 4096
MSB							LSB	

Figure 10.7 U-LINK SETTING 16K MODULE-MULTIPLE CARD MEMORY

10.5 P844-061/128, MASTER/SLAVE MEMORY

10.5.1 IDENTIFICATIONS

- Type numbers : P844-061 WMC1 (control card)
  P844-128 WMB1 (64K Words)
- Test programs : BRAM (4KW-32KW)
  BBRAM (32KW-512KW)
- Power consumption:

	Voltage	Max. Average Current		
		Operating	Stand By	Battery
WMC1	+ 5 VL + 5 VM	2.7 1.2	2.7 1.2	Ø 1.2
WMB1	+ 5 VL + 5 VM +12 VM	Ø.4 Ø.165 Ø.65	Ø.4 Ø.15 Ø.25	Ø Ø.15 Ø.25

Table 10.11 POWER CONSUMPTION P844-061/128

- 12NC code on the sticker on the board: (High speed versions)
  P844-061 (WMC1) : 5122 194 3399X (5322 216 25543)
  P844-128 (WMBI) : 5122 194 3398X (5322 216 25542)

X = Modification level

- Performance Data

Capacity: The capacity of one WMB1 is 128 kbytes (64 k words). One word consists of 16 bits plus 5 bits for internal error correction.
Read/Write is possible for 16 or 8 bits per exchange.
WMB1 (slaves) have to be used with one WMC1 (master) containing the bus control logic, refresh logic, etc.
WMC1 may drive up to 8 slaves with a total capacity of 1M bytes.

Access Time over UPL-bus:		Cycle Time over UPL-bus:	
	typ		typ
TSMN: Read cycle, no error	445ns	Read no error	565ns
Read cycle, error detected	6Ø7	Read, error detected	727
Write cycle, word or char.	173	Write word	546
ACN : Read or Write cycle	173	Write character	1Ø34

WARNING

Take care of MOS HANDLING PROCEDURE

10.5.2 INSTALLATION DETAILS

Straps: (WMC1 only)

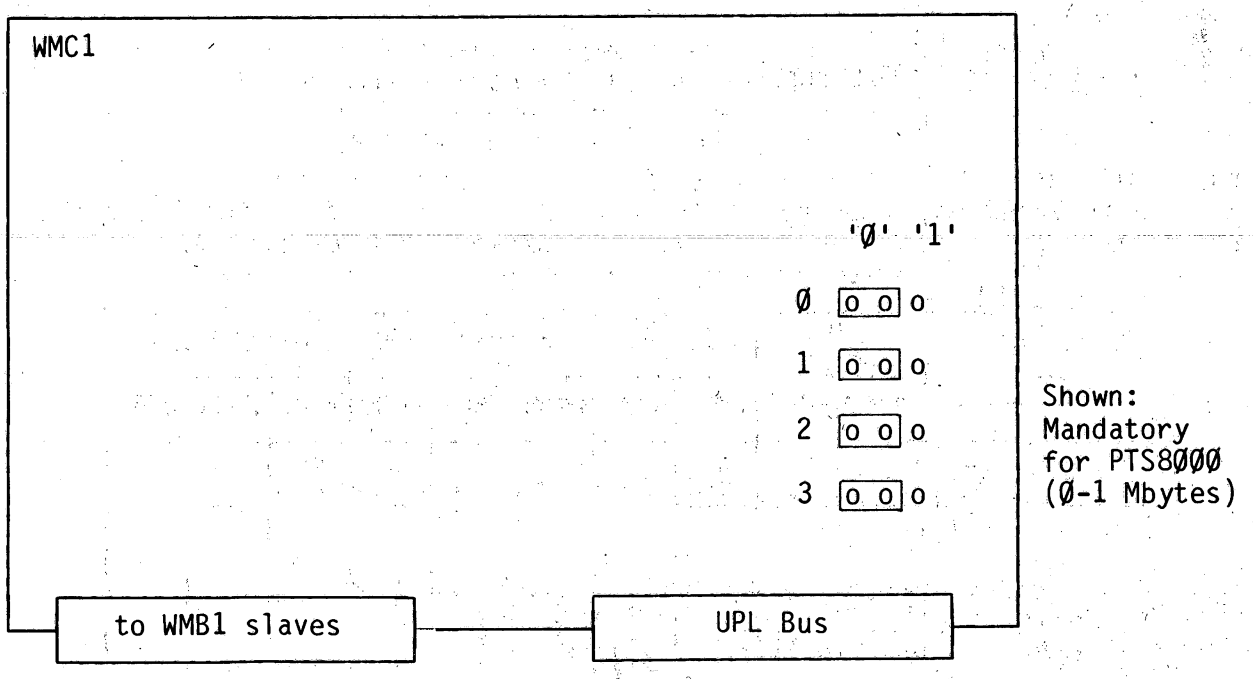


Figure 10.8 U-LINK SETTING P844-061

Capacity (KB)	Hours
128	3h45
256	2h45
384	2h15
512	1h45
64Ø	1h3Ø
768	1h15
896	1h.
1Ø24	45min.

Table 10.12 MEMORY BACK-UP TIME

		Memory Size (K bytes)							
Mode	Supply	128	256	384	512	64Ø	768	896	1Ø24
Operating	+5 VL	3.1	3.5	3.9	4.3	4.7	5.1	5.5	5.9
	+5 VM	1.36	1.53	1.7	1.86	2.Ø3	2.19	2.36	2.52
	+12VM	Ø.65	Ø.9	1.15	1.4	1.65	1.9	2.15	2.4
Standby	+5 VL	3.1	3.5	3.9	4.3	4.7	5.1	5.5	5.9
	+5 VM	1.35	1.5	1.65	1.8	1.95	2.1	2.25	2.4
	+12VM	Ø.25	Ø.5	Ø.75	1.Ø	1.25	1.5	1.75	2
Battery	+5 VL	-	-	-	-	-	-	-	-
	+5 VM	1.35	1.5	1.65	1.8	1.95	2.1	2.25	2.4
	+12VM	Ø.25	Ø.5	Ø.75	1.Ø	1.25	1.5	1.75	2

Table 10.13 POWER SUPPLY CURRENT FOR FULL MEMORY P844-061/128

Board Locations
For a required memory capacity the cards must be inserted in the backpanel as given in the table below (the table shows a complete UPL bus system).

Backpanel Loc.	n	n+1	n+2	n+3	n+4	n+5	n+6	n+7	n+8
Card Type	WMB1	WMB1	WMB1	WMB1	WMC1	WMB1	WMB1	WMB1	WMB1
Card Select No.	7	5	3	1		Ø	2	4	6
Mem. size (byte)									
Ø - 128K					x	x			
Ø - 256				x	x	x			
Ø - 384				x	x	x	x		
Ø - 512			x	x	x	x	x		
Ø - 64Ø			x	x	x	x	x	x	
Ø - 768		x	x	x	x	x	x	x	
Ø - 896		x	x	x	x	x	x	x	x
Ø - 1M	x	x	x	x	x	x	x	x	x

Table 10.14 COMPLETE MASTER/SLAVE CONFIGURATION

From a hardware point of view it is not necessary to have the memory slave cards ranked together. In this case gaps in the memory area of at least 128K bytes will occur. These gaps may be filled with other memory card e.g. 2x64kbyte memory cards.

10.5.3 INTERFACE CONNECTIONS

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
1CØ1		1BØ1		1AØ1	
1CØ2	+5VM	1BØ2		1AØ2	+5VM
1CØ3		1BØ3		1AØ3	
1CØ4		1BØ4	ØV	1AØ4	
1CØ5		1BØ5		1AØ5	
1CØ6	ØV	1BØ6	OKO	1AØ6	ØV
1CØ7		1BØ7	OKI	1AØ7	RSLN
1CØ8		1BØ8		1AØ8	ACN
1CØ9	ØV	1BØ9		1AØ9	ØV
1C1Ø		1B1Ø		1A1Ø	TSMN
1C11		1B11	ØV	1A11	TMRN
1C12	ØV	1B12	MADEØ	1A12	ØV
1C13	MADØØ	1B13	MADE1	1A13	MADØ1
1C14	MADØ2	1B14	ØV	1A14	MADØ3
1C15	MADØ4	1B15	MADE2	1A15	MADØ5
1C16	MADØ6	1B16	MADE3	1A16	MADØ7
1C17	MADØ8	1B17	MADE4	1A17	MADØ9
1C18	MAD1Ø	1B18	MADE5	1A18	MAD11
1C19	MAD12	1B19	MADE6	1A19	MAD13
1C2Ø	MAD14	1B2Ø	MADE7	1A2Ø	MAD15
1C21	CHA	1B21	ØV	1A21	WRITE
1C22	ØV	1B22		1A22	ØV
1C23	BIOØ8N	1B23		1A23	BIOØØN
1C24	BIOØ9N	1B24		1A24	BIOØ1N
1C25	BIO1ØN	1B25		1A25	BIOØ2N
1C26	BIO11N	1B26		1A26	BIOØ3N
1C27	BIO12N	1B27		1A27	BIOØ4N
1C28	BIO13N	1B28		1A28	BIOØ5N
1C29	BIO14N	1B29		1A29	BIOØ6N
1C3Ø	BIO15N	1B3Ø		1A3Ø	BIOØ7N
1C31	+12VM	1B31	+5VL	1A31	+12VM
1C32	+5VL	1B32	+5VL	1A32	+5VL

Table 10.15 UPL BUS, CONNECTOR J1, BOARD WMC1

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
1CØ1		1BØ1		1AØ1	
1CØ2	+5VM	1BØ2		1AØ2	+5VM
1CØ3		1BØ3		1AØ3	
1CØ4		1BØ4	ØV	1AØ4	
1CØ5		1BØ5		1AØ5	
1CØ6	ØV	1BØ6	OKO	1AØ6	ØV
1CØ7		1BØ7	OKI	1AØ7	
1CØ8		1BØ8		1AØ8	
1CØ9	ØV	1BØ9		1AØ9	ØV
1C1Ø		1B1Ø		1A1Ø	
1C11		1B11		1A11	
1C12	ØV	1B12		1A12	
1C13		1B13		1A13	
1C14		1B14	ØV	1A14	
1C15		1B15		1A15	
1C16		1B16		1A16	
1C17		1B17		1A17	
1C18		1B18		1A18	
1C19		1B19		1A19	
1C2Ø		1B2Ø		1A2Ø	
1C21		1B21	ØV	1A21	
1C22	ØV	1B22		1A22	ØV
1C23		1B23		1A23	
1C24		1B24		1A24	
1C25		1B25		1A25	
1C26		1B26		1A26	
1C27		1B27		1A27	
1C28		1B28		1A28	
1C29		1B29		1A29	
1C3Ø		1B3Ø		1A3Ø	
1C31	+12VM	1B31	+5VL	1A31	+12VM
1C32	+5VL	1B32	+5VL	1A32	+5VL

Table 10.16 UPL BUS, CONNECTOR J1, BOARD WMB1

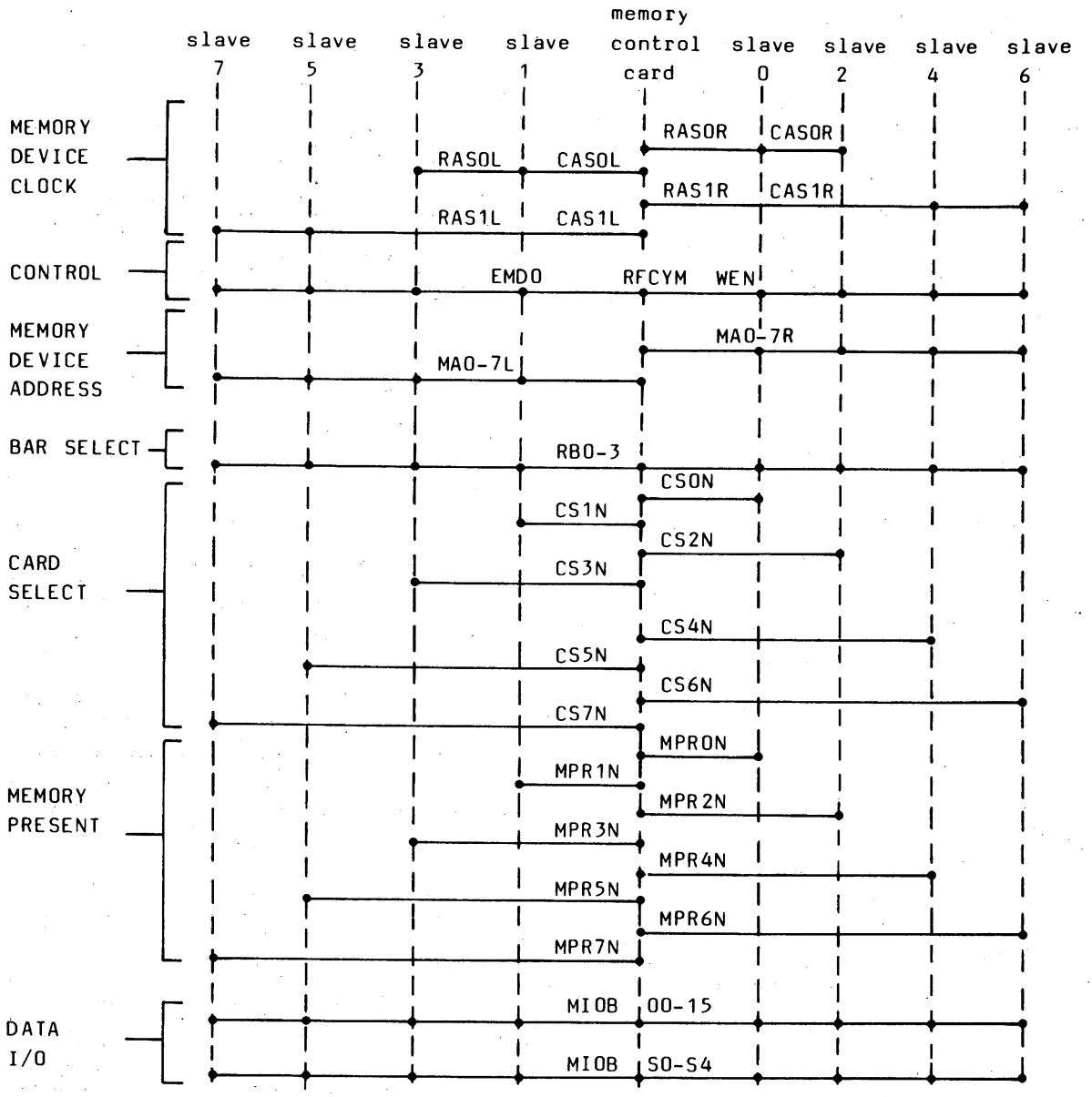
PIN NUMBERS WMC1

	A	B	C
32	CS3N	0V	CS0N
31	CS1N	CS2N	CS7N
30	0V	CS4N	0V
29	CS6N	CS5N	MPR6N
28	MPR7N	0V	MPR4N
27	MPR3N	MPR5N	MPR2N
26	0V	MPR0N	0V
25	MPR1N	CAS0R	CAS1R
24	CAS0L	0V	RAS0R
23	CAS1L	RAS0L	RAS1R
22	0V	RAS1L	0V
21	RB0	RB3	TBLECN
20	RB2	0V	RB1
19	TBLRF		WEN
18	0V	EMD0	0V
17	MA0L	MA0R	RFCYM
16	MA4L	0V	MA4R
15	MA7L	MA8L	MA3R
14	0V	MA7R	0V
13	MA2L	MA2R	MA6R
12	MA6L	0V	MA5R
11	MA5L	MA1L	MA1R
10	0V	MIOBS0	0V
9	MIOBS4	MIOBS1	MIOBS2
8	MIOB02	0V	MIOBS3
7	MIOB04	MIOB15	MIOB06
6	0V	MIOB14	0V
5	MIOB10	MIOB09	MIOB05
4	MIOB01	0V	MIOB03
3	0V	MIOB08	0V
2	MIOB00	MIOB12	MIOB13
1	MIOB07		MIOB11

PIN NUMBERS WMB1

	A	B	C
32	CSN		MPRN
31	CAS		TVBB
30	0V		0V
29			RAS
28			
27	RB0		RB3
26	0V		0V
25	RB2		RB1
24			WEN
23	EMD0		RFCYM
22	0V		0V
21	MA0		MA4
20	MA3		MA7
19	MA2		MA6
18	0V		0V
17	MA5		MA1
16	MIOBS0		
15	MIOBS4		MIOBS2
14	0V		0V
13			MIOBS1
12			
11	MIOB02		MIOB15
10	0V		0V
9	MIOB14		MIOB09
8	MIOB08		MIOB12
7	MIOB04		MIOB06
6	0V		0V
5	MIOB10		MIOB05
4	MIOB01		MIOB03
3	0V		0V
2	MIOB02		MIOB13
1	MIOB07		MIOB11

Table 10.17 INTERNAL INTERFACE, CONNECTOR J2



Backpanel:

5122 194 33840 for 8 slaves
5122 194 33870 for 4 slaves
5122 194 33880 for 2 slaves

Figure 10.9 BACKPANEL WIRING WMC1/WMB1

10.6 P843-608 WMD MEMORY (HIGH SPEED VERSION)

10.6.1 IDENTIFICATIONS

- Type No. : P843-608 (WMD)
- Testprograms : BRAM (4KW-32KW)
  BBRAM (32KW-512KW)

- Power Consumption:

	Max. Average Current		
	Operating	Stand-By	Stand-By Battery
+5VL +5VM	1.5A 1.14A 1)	1.5A 0.62A	-- 0.62

1) Based on Memory Request Rate of 660 nsec.

- Performance Data

The capacity of one WMD-H/S semiconductor memory (SCM) is 256K bytes (128K words). One word consists of 16 bits plus 5 bits for internal error correction of one faulty bit.
The X-tal frequency of High Speed Version is 27 Mc. Access time = 340 nS.

CYCLE	ACN ACCESS TIME	TSMN ACCESS TIME	MEM	BUS CYCLE
	TYP	TYP	CYCLE	TYP
READ No Error Detected	190nS	340nS	362nS	395nS
READ Error Corrected	190nS	412nS	362nS	430nS
WRITE Word	190nS	190nS	362nS	340nS
WRITE Character	190nS	190nS	724nS	700nS

Table 10.18 ACCESS AND CYCLE TIMES P843-608 (WMD)

WARNING
TAKE CARE OF MOS - HANDLING PROCEDURE!

10.6.2 INSTALLATION DETAILS

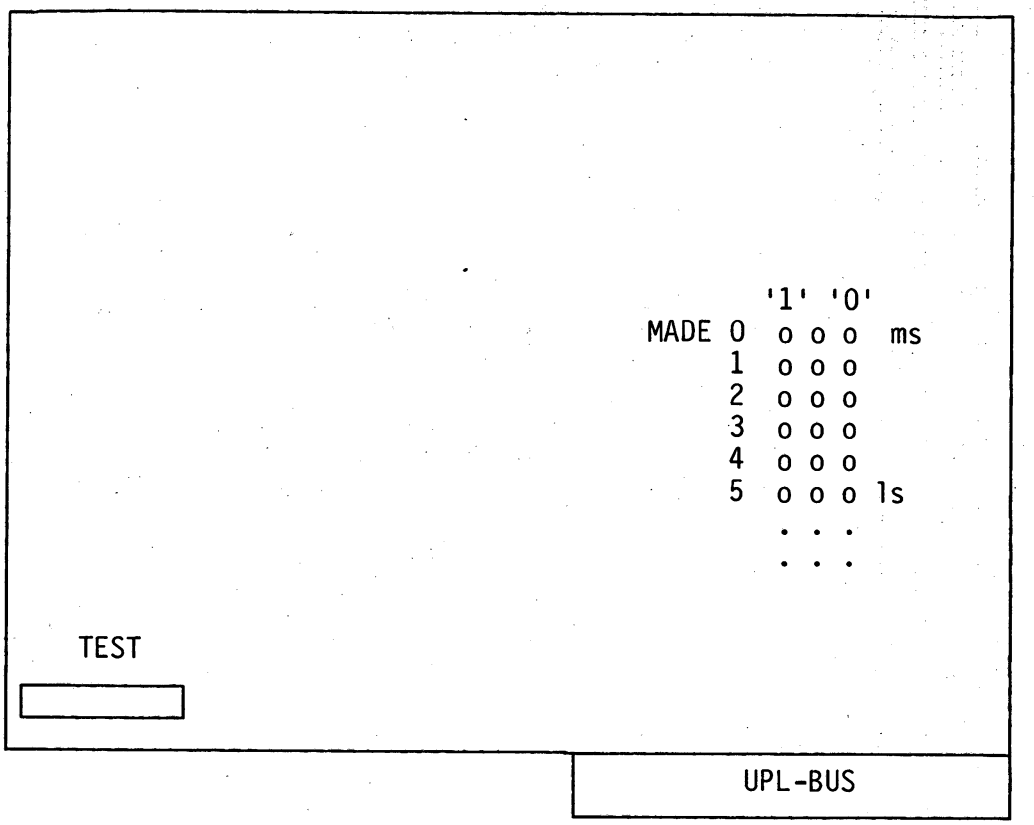
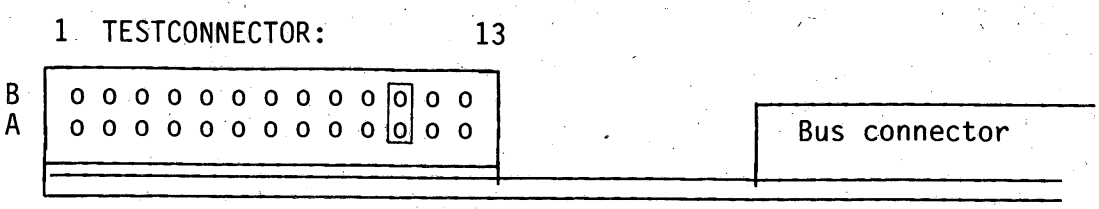


Figure 10.10 U-LINK SETTING P843-608 (WMD)

Module No.	Memory Range	MADE 0 1 2 3 4 5	Address Range
0	0 - 128K16	0 0 0 0 0 0	/000000 - /03FFFE
1	128 - 256	0 0 0 0 0 1	/040000 - /07FFFE
2	256 - 384	0 0 0 0 1 0	/080000 - /0BFFFE
3	384 - 512	0 0 0 0 1 1	/0C0000 - /0FFFFE
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
63	8M16	1 1 1 1 1 1	/FC0000 - /FFFFFE

10.6.3 BLOCKING ERROR RECOVERY

For repair in the workshop error recovery can be blocked.
Also in case of repeated memory faults at the customer, running the testprogram without error recovery may be useful.



Interconnection of TBLECN and 0V (pin B11 to A11) blocks error detection and correction. This link can be made with a U-link and can be applied when running the testprogram. DO NOT FORGET TO REMOVE THIS LINK AFTER SERVICE!

Note: For normal service this is not allowed, as error recovery is to obtain a better MTBF and thus receiving less cards for repair.
A card may be sent up for repair if two errors are on a PCB or the card is suspected to give problems to the customer (= sometimes two errors or timing problems).

10.7 SHORT DESCRIPTION OF TESTPROGRAMS

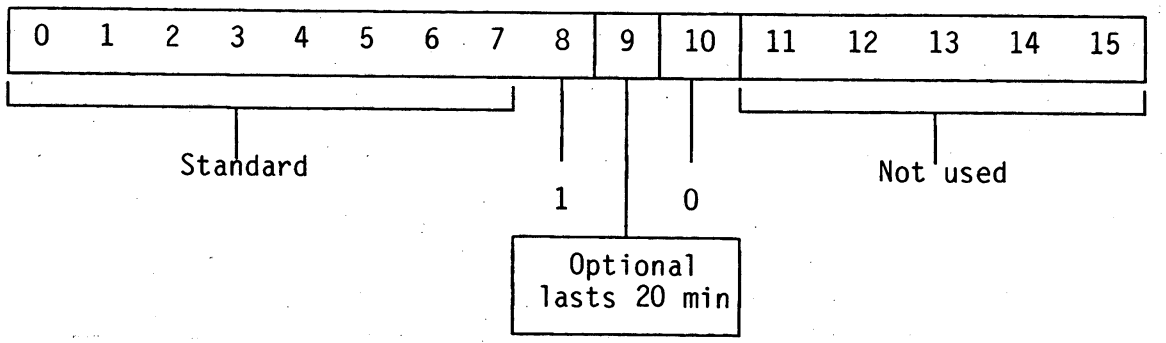
B RAM : Random Access Memory Testprogram

- Memory test 4 - 32k words
- No typewriter
- Program runs for about 5 minutes (16K memory)

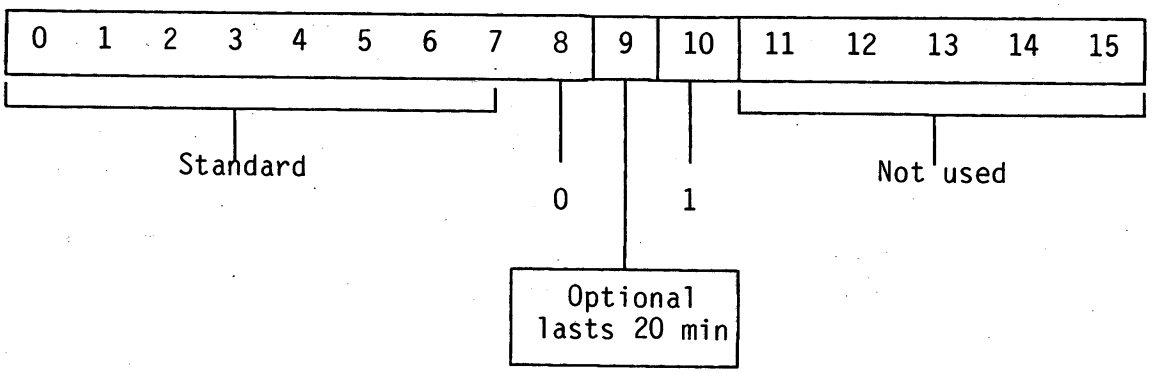
- Program stops at /200 (= restart address and correct end of test)
- Change A9 bit 0=1 (4K chips) - or - bit 1=1 (16K chips)
- Change A12 into last memory address (/7FFE if 16K 16)
- Depress MC, RUN

* Interrupt: stop on /100
* Fault : A1 gives fault indication and checknumber
  Stops on /100 (see testprogram book)
* Testprogram consists of checks:

Register A10: If 4K chips are used.



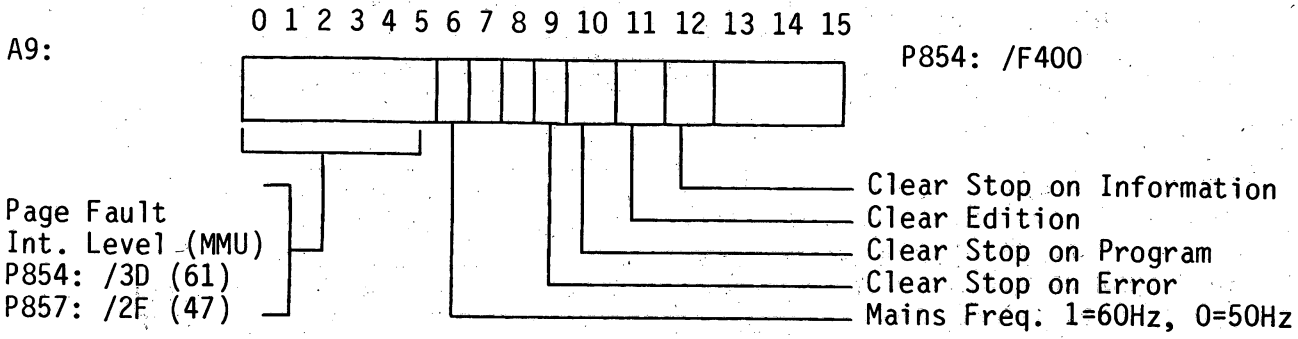
Register A10: If 16K chips are used.



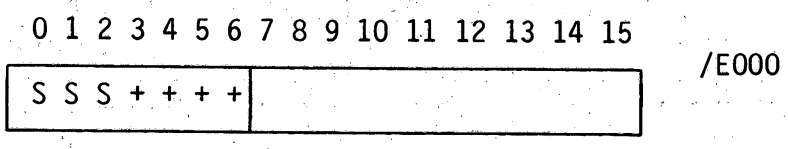
Testprogram BBRAM greater than 32K for RAM 32K to 512K on P854 with MMU.

1) IPL
   Program stops at /700 (=restart address and normal end)
2) Switch on RTC (PF/AR is possible)
3) Program modifications:

A9:



A10:

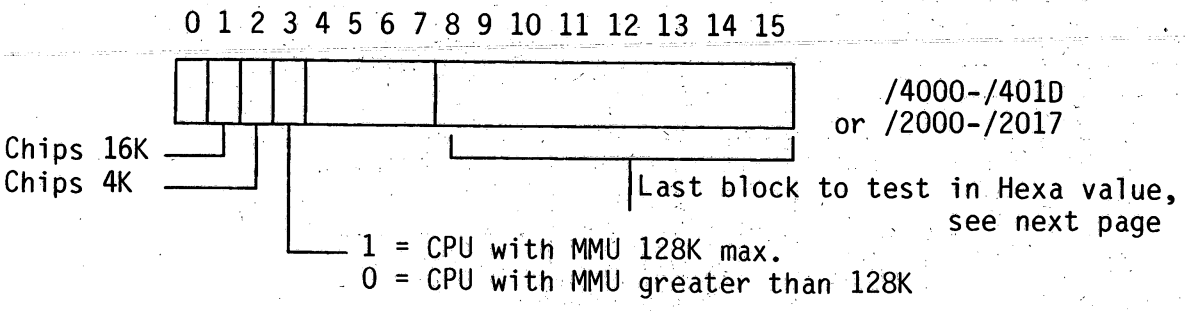


S = Standard Setting
\+ = Optional

A11: First block to be tested in Hexa value: /0 to /1D in bits 8 to 15.

16KW chips	4KW chips
/0 = 32 to 48 /10 = 288 to 304 /1 = 48 to 64 etc. (see table on next pages).	/0 = 32 to 36 /10 = 96 to 100

A12: Last block to be tested in Hexa value, see next pages.



Error stop at /5F0
Restart after power/off: /6E6
Interrupts return to /700
Information stops at /5E0

For more information, see next 2 pages and official description of the testprogram.

ZONE 0 TO 32K RESERVED FOR TESTPROGRAM

0	/0	1	/1	2	/2	3	/3
32 - 48		48 - 64		64 - 80		80 - 96	
4	/4	5	/5	6	/6	7	/7
96 - 112		112 - 128		128 - 144		144 - 160	
8	/8	9	/9	10	/A	11	/B
160 - 176		176 - 192		192 - 208		208 - 224	
12	/C	13	/D	14	/E	15	/F
224 - 240		240 - 256		256 - 272		272 - 288	
16	/10	17	/11	18	/12	19	/13
288 - 304		304 - 320		320 - 336		336 - 352	
20	/14	21	/15	22	/16	23	/17
352 - 368		368 - 384		384 - 400		400 - 416	
24	/18	25	/19	26	/1A	27	/1B
416 - 432		432 - 448		448 - 464		464 - 480	
28	/1C	29	/1D				
480 - 496		496 - 512					

BLOCK NUMBER

Decimal Value — Hexa Decimal Value

X	Y
N	N+16KW

LOCATION IN MEMORY

Table 10.19 MEMORY DESCRIPTION WITH 16KW CHIPS

ONE 0 TO 32K RESERVED FOR TESTPROGRAM

0	/0	1	/1	2	/2	3	/3
32 - 36		36 - 40		40 - 44		44 - 48	
4	/4	5	/5	6	/6	7	/7
48 - 52		52 - 56		56 - 60		60 - 64	
8	/8	9	/9	10	/A	11	/B
64 - 68		68 - 72		72 - 76		76 - 80	
12	/C	13	/D	14	/E	15	/F
80 - 84		84 - 88		88 - 92		92 - 96	
16	/10	17	/11	18	/12	19	/13
96 - 100		100 - 104		104 - 108		108 - 112	
20	/14	21	/15	22	/16	23	/17
112 - 116		116 - 120		120 - 124		124 - 128	

BLOCK NUMBER

Decimal Value / Hexa Decimal Value

X	Y
N	N+4KW

Table 10.20 MEMORY DESCRIPTION WITH 4KW CHIPS

Program MEM

Memory Address	Data	Program Instructions		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	Start	HLT	
0086	818E	Write	LDR	A9,A11
0088	85A7	Load	STR	A13,A9
008A	91A0		ADKL	A9,2
008C	0002			
008E	E992		CWR	A9,A12
0090	5C0A		RB(4)	Load
0092	5700		RF	* +2
0094	818E		LDR	A9,A11
0096	80A6	RDC	LDR *	A8,A9
0098	E896		CWR	A8,A13
009A	5002		RF(0)	Suit3
009C	207F		HLT	Fault
009E	91A0	Suit3	ADKL	A9,2
00A0	0002			
00A2	E992		CWR	A9,A12
00A4	5C10		RB(4)	RDC
00A6	5F22		RB	Write

Start the program:

- Load the starting address in register A11
- Load the ending address in register A12
- Load the test-pattern in register A13
- Load the start-address of the program (/0086) into register A0
- Push the RUN button

After Start:

If no fault the program runs in loop

Fault: program stops at /009E

- A9 contains address of erronous memory location
- A8 contains read pattern
- A13 contains expected pattern

DUMP FACILITY

This program enables an area of memory to be printed out on either the ASR or PTS3100, or to be Displayed. It can be loaded either with the IPL routine or by hand using the control panel switches. Once loaded the following routine should be used:

- Load the starting address to be printed into register A7. *)
- Load the ending address of the area into register A8.
- Load the starting address of the program into register A0.
- Push the RUN button.

The program will stop when the last memory address has been either printed or displayed.

*) Bit 15 must be zero.

Program DUMP

Memory Address	Data	Program Instructions		
0080	FFFF		DATA	-/FFFF
0082	0000		DATA	0
0084	207F	START	HLT	
0086	20BF		INH	
0088	47D0		CIO	A7,1,/10
008A	813C	WORD	LDR *	A1,A7
008C	0204		LDK	A2,4
008E	060F	CONT	LDK	A6,/F
0090	A604		ANR	A6,A1
0092	E558		LC	A5, TABLE, A6
0094	00BE			
0096	E549		SC	A5,BUFF + 1.A2
0098	00CF			
009A	39E4		SRC	A1,4

Memory Address	Data	Program Instructions		
009C	1A01		SUK	A2,1
009E	5C12		RB(NZ)	CONT
00A0	E348	OUT1	LC	A3,BUFF,A2
00A2	00CE			
00A4	4310		OTR	A3,0,/10
00A6	5C04		RB(NA)	* -2
00A8	1201		ADK	A2,1
00AA	EA20		CWK	A2,6
00AC	0006			
00AE	5C10		RB(NE)	OUT1
0080	1702		ADK	A7,2
00B2	EF02		CWR	A7,A8
00B4	5D2C		RB(NG)	WORD
00B6	4790		CIO	A7,0,/10
00B8	4FD0		SST	A7,/10
00BA	5C04		RB(NA)	* -2
00BC	5F3A		RB	START
00BE	3031	TABLE	DATA	'0123456789'
00C0	3233			
00C2	3435			
00C4	3637			
00C6	3839			
00C8	4142		DATA	'ABCDEF'
00CA	4344			
00CC	4546			
00CE	0D0A	BUFF	DATA	/0D0A

```
00000                                IDENT    MEM3
00001                               *MEMORY TEST FOR MEMORY FROM 32KW TILL END OF MEM
00002                               *
00003                               *(A1)=MOST SIGNIFICANT MEMORY ADDRESS
00004                               *(A2)=LEAST SIGNIFICANT MEMORY ADDRESS
00005                               *(A3)=BEGIN ADDRESS TO TEST (MOST SIGNIFICANT PART)
00006                               *(A5)=PAL.....PAM OF MMU TABLE
00007                               *(A6)=TEST PATTERN (ROTATED)
00008                               *(A7)=TEST PHASE : 1, 2 OR 3
00009                               *(A8)=NUMBER OF COMPLETE TEST CYCLES
00010                               *(A9)=MEMORY END ADDRESS (MOST SIGN.)
00011                               *(A10)=MEMORY END ADDRESS LEAST SIGNIFICANT
00012                               *(A11)=
00013                               *(A12)=WANTED TEST PATTERN
00014                               *(A13)=TEST PATTERN (ROTATED), READ FROM MEMORY
00015                               *(A14)=WRITTEN DATA OF TEST-PHASE 1
00016                               *(A15)=READ DATA OF TEST-PHASE 1
00017                               *
00018                               *AFTER LOADING THE PROGRAM THE NEXT REGISTERS CAN BE CHANGED:
00019                               *    -A3 :MOST SIGNIFICANT PART OF BEGIN ADDRESS
00020                               *     A3 PRESET WITH /0001 = 32KW BASE
00021                               *    -A12:TEST PATTERN FOR TEST PHASE 2 & 3
00022                               *REGISTER A8 WILL COUNT THE NUMBER OF COMPLETE TEST CYCLES AND
00023                               * THE PROGRAM STAYS RUNNING UNTIL AN ERROR IS FOUND
00024                               *  REGISTERS A1 & A2 CONTAIN THE ERROR ADDRESS.
00025                               *            A7 CONTAINS THE TEST PHASE: 1= ALL /5555, /AAAA
00026                               *                                       2= WRITE TEST PATTERN
00027                               *                                       3= READ TEST PATTERN
00028                               *
00029  0000                                  RES      /40
00030  0080  FFFF                            DATA     /FFFF,0
       0082  0000
00031  0084  208F                   START    INH
00032  0086  80A0                            LDKL     A8,0
       0088  0000
00033  008A  0301                            LDK      A3,1
00034  008C  0701                            LDK      A7,1
00035  008E  84A0                            LDKL     A12,/3569          DEFAULT TEST PATTERN
       0090  3569
00036  0092  207F                   RESTAR   HLT
00037  0094  810C                   NEXTPH   LDR      A1,A3              0000000000000001
00038  0096  8504                   NEX32K   LDR      A5,A1              0000000000000001
00039  0098  3DE2                            SRC      A5,2               0100000000000000
00040  009A  0400                            LDK      A4,0
00041  009C  8551                   NEXWRD   ST       A5,TABLE,A4
       009E  0126  R
00042  00A0  1402                            ADK      A4,2
00043  00A2  9520                            ADKL     A5,/400            INCREMENT PAL WITH 1
       00A4  0400
00044  00A6  EC20                            CWK      A4,32              16 WORDS PREPARED
       00A8  0020
00045  00AA  5C10                            RB(NE)   NEXWRD
00046  00AC  8840                            TL       TABLE
       00AE  0126  R
00047  00B0  EF20                            CWK      A7,1               TEST PHASE 1 OR HIGHER?
       00B2  0001
00048  00B4  5130                            RF(G)    TEST2
00049  00B6  0200                   TEST1    LDK      A2,0               PROGRAM ADDRESS 0
00050  00B8  86A0                   TES32K   LDKL     A14,/5555          CHECK FIRST 32K
       00BA  5555
00051  00BC  D6A9                            ESR      A14,A2             WITH /5555 AND
00052  00BE  D7A8                            ELR      A15,A2
00053  00C0  EE9E                            CWR      A14,A15
00054  00C2  5412                            RF(NE)   MEMEND
00055  00C4  969A                            ADR      A14,A14
00056  00C6  D6A9                            ESR      A14,A2             WITH /AAAA
00057  00C8  D7A8                            ELR      A15,A2
00058  00CA  EE9E                            CWR      A14,A15
00059  00CC  5408                            RF(NE)   MEMEND
00060  00CE  1202                            ADK      A2,2
00061  00D0  5C1A                            RB(NZ)   TES32K
00062  00D2  1101                            ADK      A1,1               NEX 32K RELOAD THE TABLE
00063  00D4  5F40                            RB       NEX32K
00064  00D6  EFA0                   MEMEND   CWK      A15,0
       00D8  0000
00065  00DA  5448                            RF(NZ)   ERROR1
00066  00DC  8288                            LDR      A10,A2
00067  00DE  8184                            LDR      A9,A1              (A9,A10)=MEMORY END ADDRESS
00068  00E0  0702                            LDK      A7,2               FLAG FOR TESTPHASE 2
00069  00E2  8612                            LDR      A6,A12             LOAD ROTATE REG WITH TEST PATTERN
00070  00E4  5F52                            RB       NEXTPH
00071  00E6  0200                   TEST2    LDK      A2,0
00072  00E8  EF20                            CWK      A7,2               PHASE 2 OR 3 ?
       00EA  0002
00073  00EC  5112                            RF(G)    TEST3
00074  00EE  D629                   TES32    ESR      A6,A2
00075  00F0  3EE3                            SRC      A6,3
00076  00F2  1202                            ADK      A2,2
00077  00F4  5C08                            RB(NZ)   TES32
00078  00F6  1101                            ADK      A1,1
00079  00F8  E906                            CWR      A1,A9              COMPARE END ADDR (N X 32K)
00080  00FA  5D66                            RB(NG)   NEX32K
00081  00FC  0703                            LDK      A7,3               FLAG TEST PHASE 3
00082  00FE  5F6C                            RB       NEXTPH
```

```
00083  0100  0200      TEST3    LDK      A2,0
00084  0102  D5A8      TST32    ELR      A13,A2
00085  0104  ED98               CWR      A13,A6
00086  0106  540C               RF(NE)   ERR0R3
00087  0108  3EE3               SRC      A6,3
00088  010A  1202               ADK      A2,2
00089  010C  5C0C               RB(NZ)   TST32
00090  010E  1101               ADK      A1,1
00091  0110  E906               CWR      A1,A9
00092  0112  5D7E               RB(NG)   NEX32K
00093  0114  EA0A      ERR0R3   CWR      A2,A10
00094  0116  520C               RF(L)    ERR0R1
00095  0118  E906               CWR      A1,A9
00096  011A  5208               RF(L)    ERR0R1
00097  011C  0701               LDK      A7,1
00098  011E  90A0               ADKL     A8,1
       0120  0001
00099  0122  5F90               RB       NEXTPH
00100  0124  5F94      ERR0R1   RB       RESTAR
00101  0126           TABLE    RES      16
00102                           END      START
```

SYMB0L TABLE

ERR0R1	0124	R	ERR0R3	0114	R	MEMEND	00D6	R	NEX32K	0096	R
NEXTPH	0094	R	NEXWRD	009C	R	RESTAR	0092	R	START	0084	R
TABLE	0126	R	TES32	00EE	R	TES32K	00B8	R	TEST1	0086	R
TEST2	00E6	R	TEST3	0100	R	TST32	0102	R			

ASS.ERR. 00000

```
:EOF
PROG ELAPSED TIME:  00H-00M-42S-060MS-
```

11 MEMORY MANAGEMENT UNIT

SECTION	11.1	MEMORY MANAGEMENT UNIT IDENTIFICATIONS	PAGE 11-2
	11.2	MEMORY MANAGEMENT UNIT FUNCTIONS	11-3
	11.3	SHORT DESCRIPTION OF TESTPROGRAMS	11-6
	11.4	SHORT ROUTINE	11-7

LIST OF ILLUSTRATIONS

FIGURE	11.1	MEMORY MANAGEMENT	11-4
	11.2	PAGE FAULT SEQUENCE	11-5

11.1 MEMORY MANAGEMENT UNIT (MMU) - IDENTIFICATIONS

Type Number : Standard with P854 (MIOP).

Testprogram : REPAF, REMMUI

Power Consumption : Refer to CPU (MIOP), see chapter 8.

11.2 MEMORY MANAGEMENT UNIT - FUNCTIONS

The Memory Management Unit (MMU) is a hardware facility which provides extended memory addressing and memory protection facilities for the P854 system.

EXTENDED MEMORY ADDRESSING (TRANSLATION)

The principal function of the MMU is to extend the memory addressing up to 8M physical words (24 address bits). (See Figure 11.1)
The basic rules for the operation of this facility are as follows:

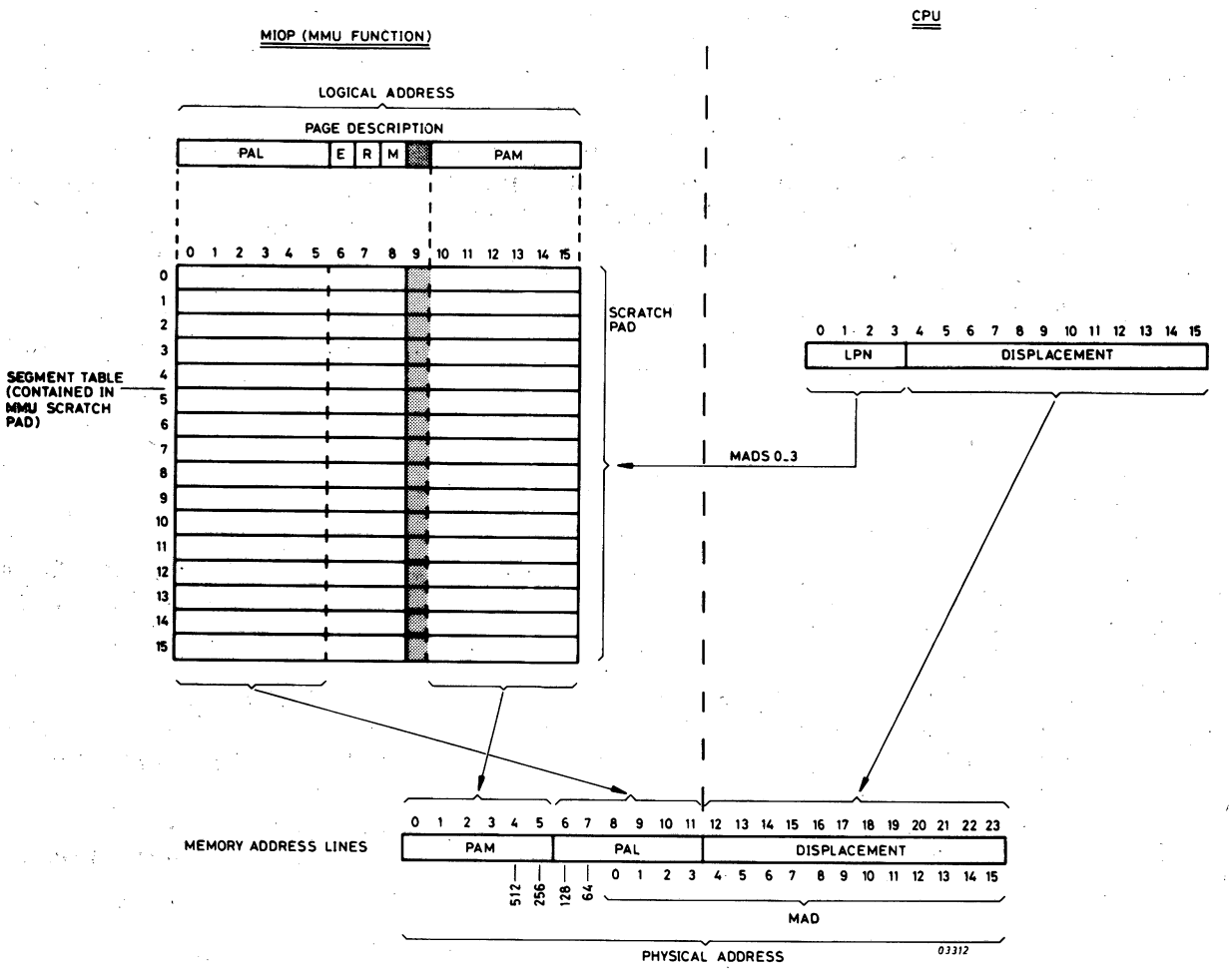
- A 16 word segment table is pre-loaded with page addresses by one Table Load Instruction.
- All CPU/Memory transfers via the MMU use the four most significant address lines (MAD0-3) to select the table segment (page 0-15). The content of each page gives the 12 most significant MAD address bits plus 3 control bits.
- The Table Store instruction is used by software to read the 16 word segment table for test purposes or for dynamic relocation.

MEMORY PROTECTION

For memory protection purposes 2 information bits are loaded into the segment table at the same time that the TL instruction loads the page addresses; these information bits are:

- Bit 6 (E) Page Error if 1, page restricted to system mode only.
- Bit 7 (R) Read Only Indicator = 1 to protect the page against Write operations If an address translation in User Mode attempts to Write on this page then the translation is blocked.

In both of these cases the MMU indicates to the CPU that a Page Fault (PAF) has occured.



ABBREVIATIONS

PAL	—	PAGE ADDRESS LEAST SIGNIFICANT
PAM	—	PAGE ADDRESS MOST SIGNIFICANT
E	—	PAGE ERROR; = 1 EXCEPT FOR MEMORY RESIDENT PAGES OF USER PROGRAM
R	—	READ ONLY INDICATOR; = 1 TO PROTECT THE PAGE AGAINST WRITE OPERATIONS
M	—	MODIFIED INDICATOR; = 1 WHEN A WRITE OPERATION IS PERFORMED FOR THAT PAGE
LPN	—	LOGICAL PAGE NUMBER
DISPLACEMENT	—	GIVES THE ADDRESS RELATIVE TO THE BEGINNING OF THE LOGICAL PAGE NUMBER
MAD	—	MEMORY ADDRESS LINES

Figure 11.1 MEMORY MANAGEMENT

MODIFIED PAGE

This feature indicates to the operating system if a page needs to be "swapped out" or not. If it does not need to be "swapped out" then the new page can be overwritten so saving time. This possibility is indicated by bit 8 (M) which is set to "1" by the MMU whenever a Write operation (Store Instruction) is performed on a specific page.

PAGE FAULT

When an attempt is made to write into a protected page or access is made in user mode to a page that is restricted to system mode only, the MMU signal "Page Fault" initiates an interrupt TRAP Routine at the CPU. The sequence of events is indicated in the following Flow Chart:

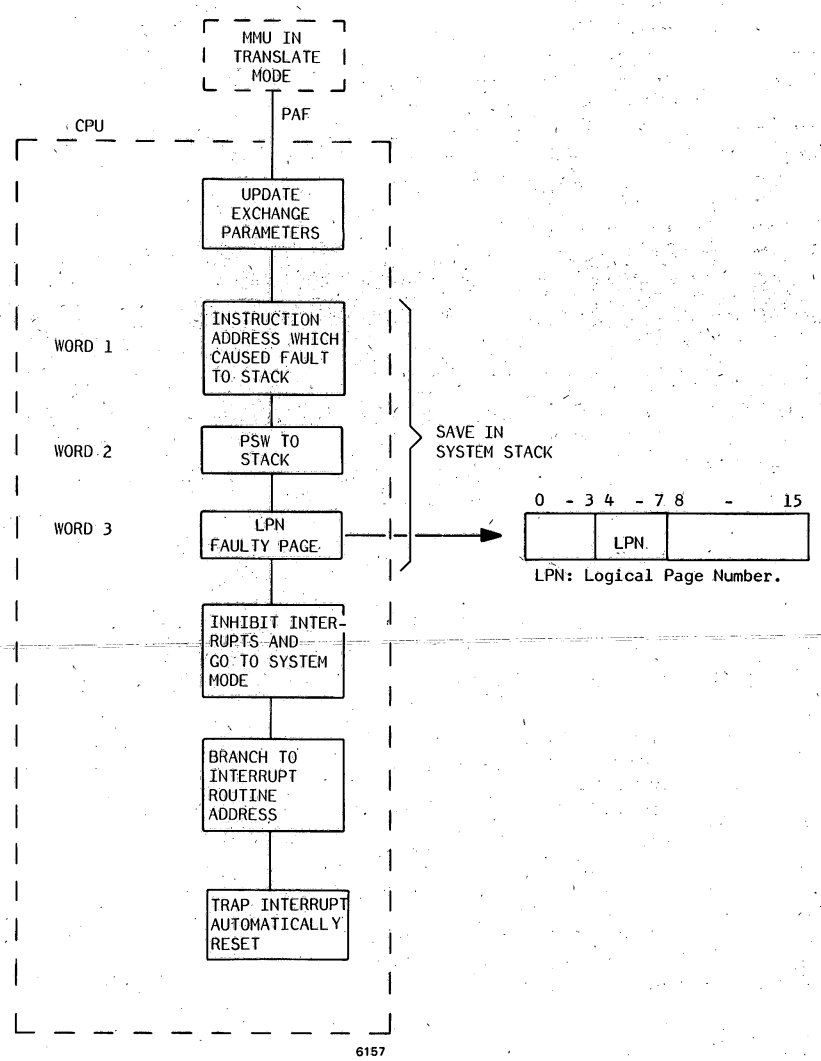


Figure 11.2 PAGE FAULT SEQUENCE

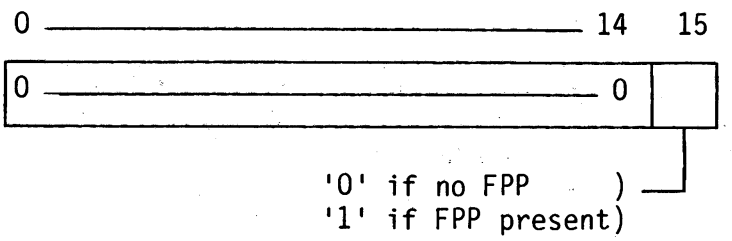
11.3 SHORT DESCRIPTION OF TESTPROGRAMS

PROGRAM REPAF — 32 KW memory min.
test for page fault, RTC and PF/AR

. IPL

. Stop at /400

Modify register: A10



. MCL, RUN

- Switch on the RTC (LOCK for PF/AR)

. - The program loops continuously . /2B4 contains test loop counter = check on run-. (one loop lasts about 0.1 sec.).
  - Error: program stops. A6 contains error info.
  - Stop at /31A: reception of unexpected interrupt.
  - /2B6 contains counter for no. of auto restarts.
  - Restart address is /3EA (after power fail).

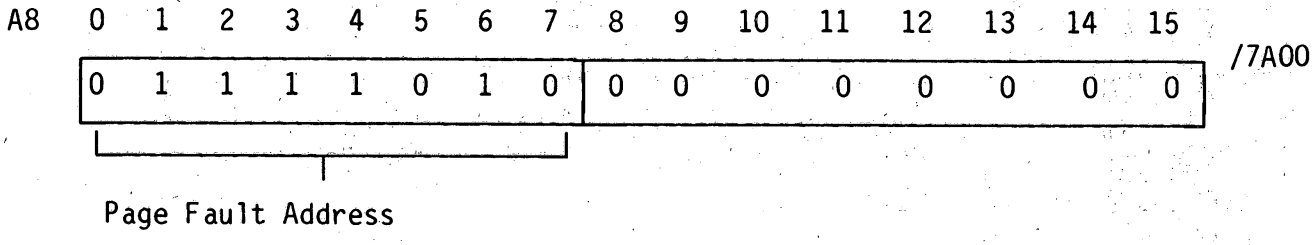
For more information see official description of testprograms.

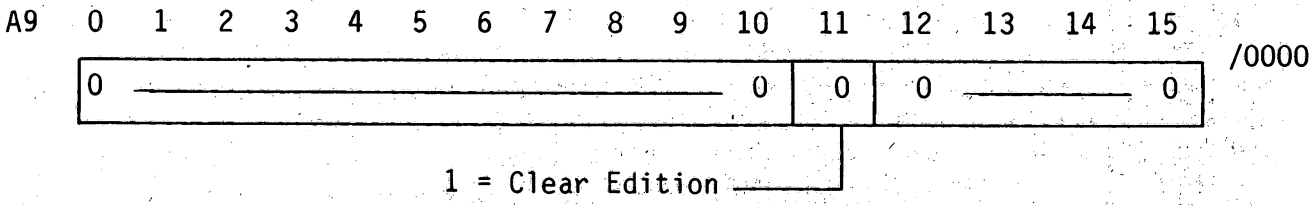
PROGRAM REMMU1 Memory size 32 KW min.
Test of MMU in memory size 0 - 32 KW

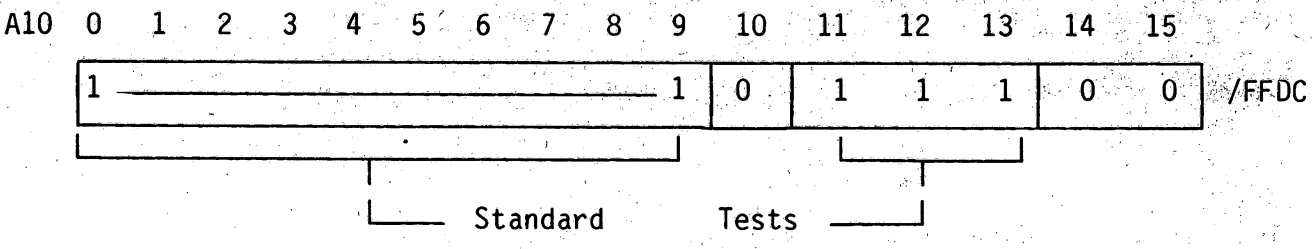
. IPL

. Stop at /700 = restart address = after reception of unexpected interrupt.

- Change registers:







Switch on RTC (PF/AR also possible).

. MCL, RUN

. /700 Normal end.

- /5E0 Info stop (A1 may contain info code).

- /5F0 Error stop A1 contains error code (see also official description of testprogram).

- Restart after power off: /6EE.

Note: Some checks are in inhibit mode. In such a case the power fail interrupt may be handled too late and auto restart fails.

11.4 SHORT ROUTINE

```
00000                          IDENT    MMU2C
00001                  *
00002                  *
00003                  *PROGRAM TO TEST MMU FUNCTIONS
00004                  *
00005                  *THE USER PART OF THIS PROGRAM WILL BE TRAPPED ON A NOT ALLOWED
00006                  *STORE OPERATION IN PAGE 2.
00007                  *EACH TIME THE CP-INT BUTTON IS PRESSED, THE PROGRAM WILL BE
00008                  *MODIFIED, GIVING TRAPS ON ACCESS PAGE 1 OR WRITE ACCESS PAGE 2
00009                  *WHEN THE PROGRAM IS STOPPED BY A HLT INSTRUCTION IT IS POSSIBLE
00010                  *TO CHECK THE SYSTEM STACK (A15) AND THE SEGMENT TABLE (/300).
00011                  *
00012          0006    CPLEV    EQU      6                  FOR P854: /E IF P858/P859
00013                           AORG     /100
00014                  *
00015                  *
00016  0100    8841    PROGINT  TS       /300               SEGMENT TABLE TO MEMORY
       0102    0300
00017  0104    20FB             RIT      /1D
00018  0106    207F             HLT                         CHECKPOINT:TABLE + STACK
00019  0108    8840             TL       /200               LOAD SEGMENT TABLE INTO MIOP
       010A    0200
00020  010C    87A0             LDKL     A15,/150           LOAD STACK POINTER
       010E    0150
00021  0110    8120             LDKL     A1,/FFE            PROGRAM COUNTER OF USER
       0112    0FFE
00022  0114    813F             STR      A1,A15             TO THE STACK
00023  0116    8120             LDKL     A1,/4041           PSW OF USER
       0118    4041
00024  011A    813F             STR      A1,A15             TO THE STACK
00025  011C    8120             LDKL     A1,/160            START ADDRESS TRAP ROUT.
       011E    0160
00026  0120    8141             ST       A1,/7A             PAGE FAULT TRAP ENTRY
       0122    007A
00027  0124    8120             LDKL     A1,/100            START ADDRESS PROG.INT ROUT.
       0126    0100
00028  0128    8141             ST       A1,2               LEVEL 1
       012A    0002
00029  012C    8120             LDKL     A1,/400            START ADDRESS CPINT ROUTINE
       012E    0400
00030  0130    8141             ST       A1,CPLEV           LEVEL:P854=3,(P858/9=?)
       0132    0006
00031  0134    F03E             RTN      A15                START USER PROGRAM (LEVEL=/1D)
00032                           AORG     /160
00033                  *
00034                  *
00035  0160    8841    TRAP     TS       /300               SEGMENT TABLE TO MEMORY
       0162    0300
00036  0164    207F             HLT                         CHECKPOINT:TABLE + STACK
00037  0166    8120             LDKL     A1,/200C           RESTART USER
       0168    200C
00038  016A    8141             ST       A1,/150            PROGRAM AT ADDRESS /200C (=/300C)
       016C    0150
00039  016E    813E             LDR*     A1,A15             A15 ADJUSTED +2 AFTER PAGE FAULT TRAP
00040  0170    F03E             RTN      A15
00041                           AORG     /200
00042                  *
00043                  *
00044  0200    0000    SEGTAB   DATA     /0000              SEGMENT TABLE PAGE 0
00045  0202    0400             DATA     /0400              PAGE 1
00046  0204    0D00             DATA     /0D00              PAGE 2
00047                           AORG     /400
00048                  *
00049                  *
00050  0400    8120    CPINT    LDKL     A1,/200            ROUTINE TO CHANGE TABLE :PAGE 1
       0402    0200
00051  0404    B141             XRS      A1,/202            BIT 6 (E) SET OR RESET
       0406    0202
00052  0408    20DF             RIT      /0F                RESET CONTROL PANEL INT.
00053  040A    F03E             RTN      A15                GO BACK TO USER PROGRAM
00054                           AORG     /FFE
00055                  *
00056                  *
00057  0FFE    013F    USER     LDK      A1,/3F             PAGE 0 IS ACCESSED
00058  1000    1102    PAGE1    ADK      A1,2               PAGE 1 IS ACCESSED
00059  1002    8F20             ABL      /2000              BRANCH TO PAGE 2 (/3000)
       1004    2000
00060                           AORG     /3000
00061                  *
00062                  *
00063  3000    8141    PAGE2    ST       A1,/500            STORE INTO PAGE 0
       3002    0500
00064  3004    8140             LD       A1,/2200           LOAD FROM PAGE 2
       3006    2200
00065  3008    8141             ST       A1,/2200           STORE INTO PAGE 2 (TRAPPED)
       300A    2200
00066  300C    2804             LKM                         CALL SYSTEM MODE VIA PROG. INT
00067  300E    0000             DATA     0
00068                           END
```

12 ASYNCHRONOUS SERIAL CONTROL UNIT P845-145 (ASCU4Z)

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12.1 ASCU4Z IDENTIFICATIONS

Type Number : P845-145
Test program : BASCU4
Channel : PC (all lines) or IOP (line 2 and 3 only)
Interrupt connection : 1CO5 (all lines)
Break connection : 1AO5 (line 2)
; 1AO4 (line 3)

Devices : 4 lines Half Duplex or
2 line Full Duplex or
2 line Half Duplex + 1 line Full Duplex.

Power consumption : +5VL 700mA
+12VL 40mA
-12VL 40mA

12NC code on the sticker on the board:

5111 199 6827X (5322 216 25316)

X = modification level.

12.2 FACILITIES

- Control Unit for four local lines, V24 or current loop connection, A-synchronous.
- Connections 4 x Half Duplex
2 x Full Duplex -or-
1 x Full Duplex and 2 x Half Duplex
- Transfer rate selectable 11Ø-15Ø-3ØØ-6ØO-12ØØ-24ØØ-48ØØ-96ØØ bps.
- Word length selectable, 7 or 8 bits
- Parity (VRC) software controlled
- Stopbits: 1 for reception, 2 for transmission
- Echo mode selectable (ASCU Half Duplex, 4 wire connection)
- Break detection for all lines (Half Duplex, input during output detected)
- Break key detection on line 'Ø' to be used as Control Panel Interrupt; not used on P853/4
- Framing error detection on line 1, 2 and 3
- CT133 selectable (Ready for Receive) to connect PER 31ØØ CTW
- Four (consecutive) device addresses, one for each line
One (shared) interrupt on pin 1CØ5
Two break levels: line '2' on pin 1AØ5
line '3' on pin 1AØ4
- Break key Detection (line OO, only for P851 systems) Connect pin 1CO4 of ASCU4Z Card (signal IR1N) to pin 2AO4 of the CPU (P851).

- Connect pin 2C11 of the P851 CPU (signal CPZON) to pin 1CO3 of the ASCU4Z card.

12.3 INSTALLATION DETAILS

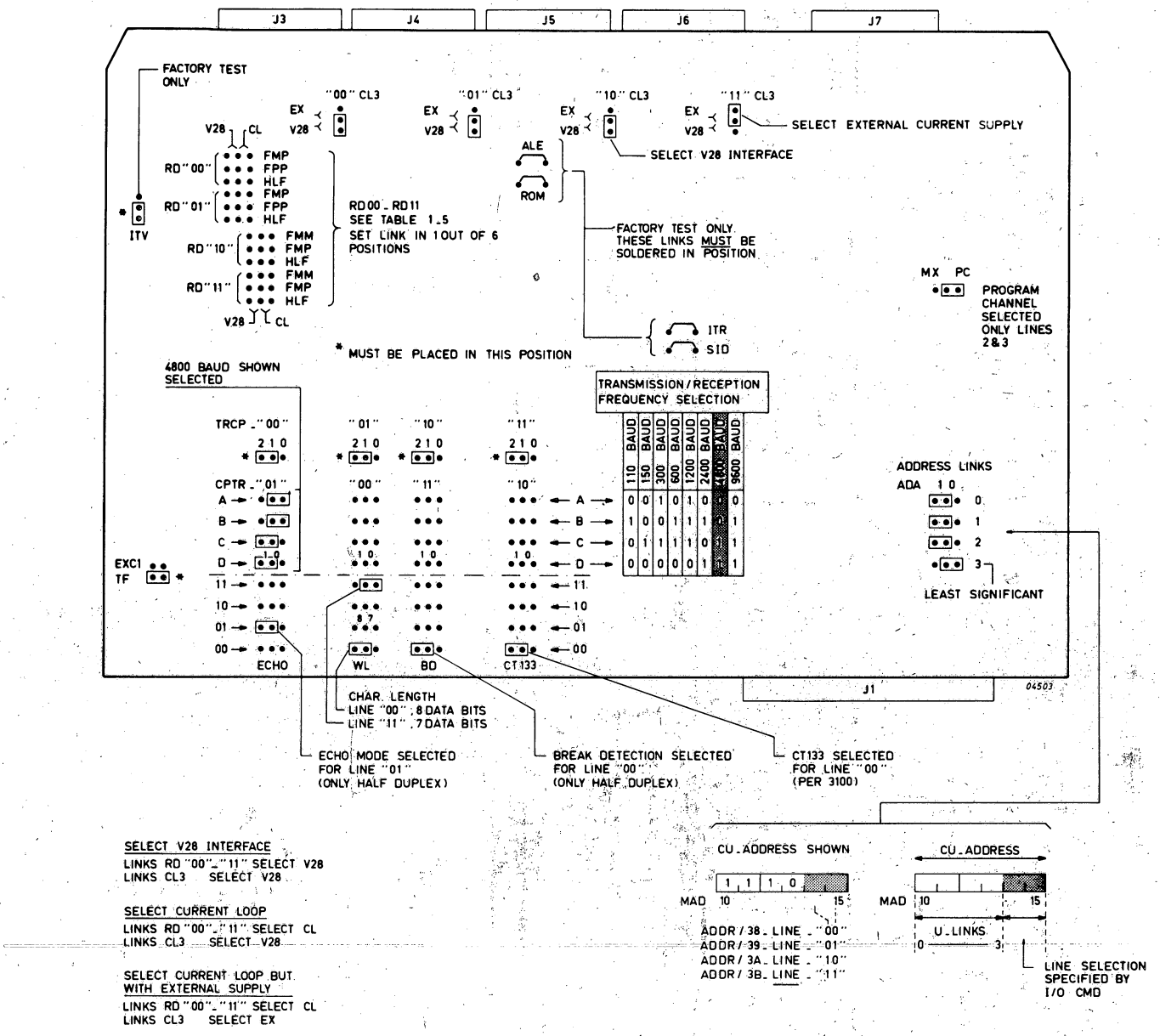


Figure 12.1 U-LINK SETTING

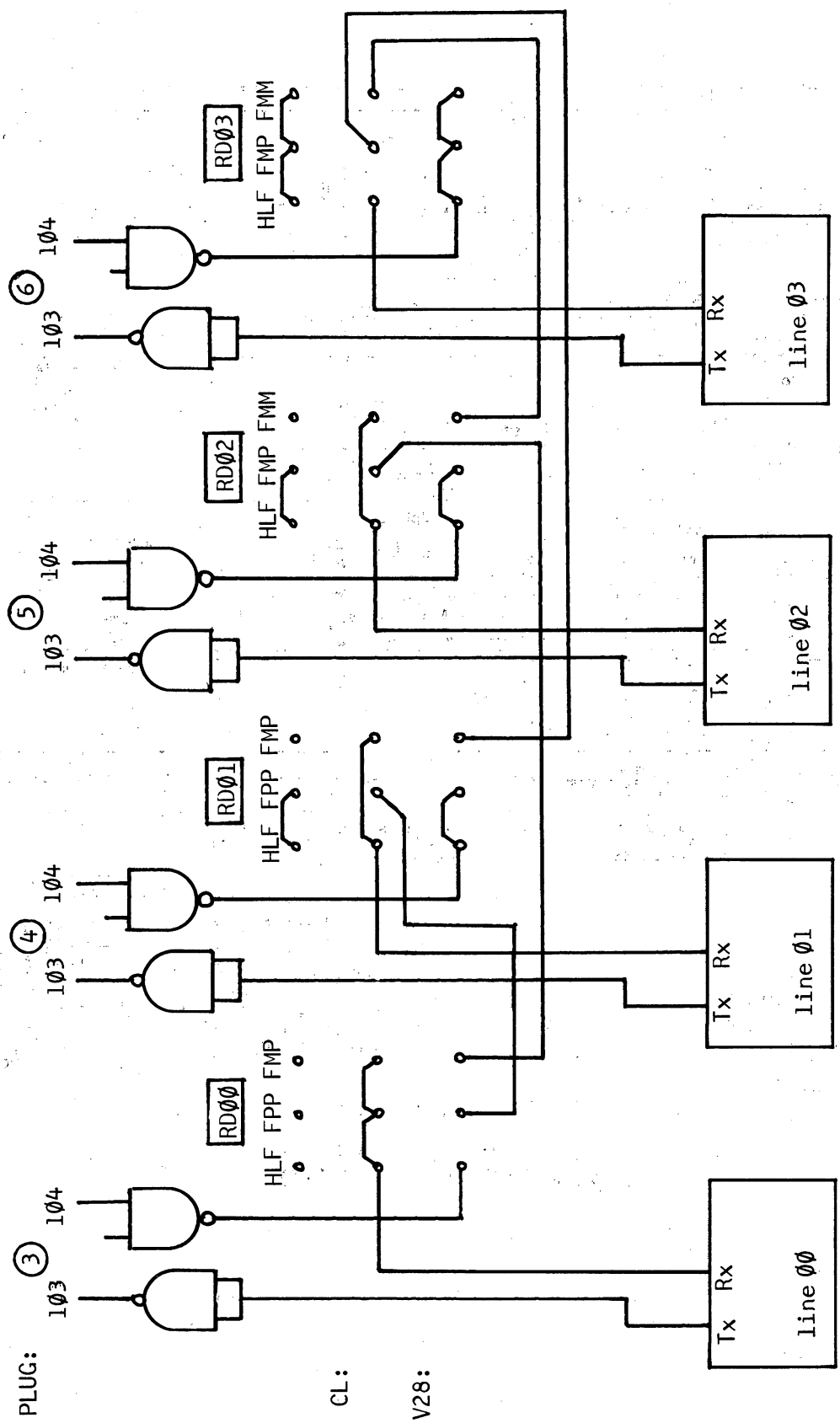


Figure 12.2 U-LINK SETTING (HLF, FPP, FMP, FMM)

LINE OUT OR IN		PERIPH CONN.	U-LINKS				
LINE ADDR	CHANNEL TYPE		MX/PC	RD00	RD01	RD10	RD11
00	PC	3J ┐	PC	HLF	HLF	HLF	HLF
01	PC	4J ├					
10	PC	5J					
11	PC	6J ┘					
00	PC	3J ┐	MX	HLF	HLF	HLF	HLF
01	PC	4J ├					
10	MX	5J					
11	MX	6J ┘					

Table 12.1 FOUR LINES HALF DUPLEX

LINE OUT		LINE IN		PERIPH CONN.	U-LINKS				
LINE ADDR.	CHANNEL TYPE	LINE ADDR.	CHANNEL TYPE		MX/PC	RD00	RD01	RD10	RD11
01	PC	00	PC	4J ┐	PC	FPP	FPP	FMM	FMM
11	PC	10	PC	6J ┘					
10	PC	00	PC	5J ┐	PC	FMP	FMP	FMP	FMP
11	PC	01	PC	6J ┘					
01	PC	00	PC	4J ┐	MX	FPP	FPP	FMM	FMM
11	MX	10	MX	6J ┘					
10	MX	00	PC	5J ┐	MX	FMP	FMP	FMP	FMP
11	MX	01	PC	6J ┘					

Table 12.2 TWO LINES FULL DUPLEX

HALF DUPLEX			HALF DUPLEX			FULL DUPLEX				U-LINKS				
						LINE OUT		LINE IN		PER CONN				
LINE ADDR.	CHANNEL TYPE	PER. CONN.	LINE ADDR.	CHANNEL TYPE	PER CONN.	LINE ADDR.	CHANNEL TYPE	LINE ADDR.	CHANNEL TYPE		MX/PC	RD00	RD01	RD10	RD11
10	PC	5J	11	PC	6J	01	PC	00	PC	4J	PC	FPP	FPP	HLF	HLF
00	PC	3J	01	PC	4J	11	PC	10	PC	6J	PC	HLF	HLF	FMM	FMM
01	PC	4J	11	PC	6J	10	PC	00	PC	5J	PC	FMP	HLF	FMP	HLF
00	PC	3J	10	PC	5J	11	PC	01	PC	6J	PC	HLF	FMP	HLF	FMP
00	PC	3J	01	PC	4J	11	MX	10	MX	6J	MX	HLF	HLF	FMM	FMM
10	MX	5J	11	MX	6J	01	PC	00	PC	4J	MX	FPP	FPP	HLF	HLF
01	PC	4J	11	MX	6J	10	MX	00	PC	5J	MX	FMP	HLF	FMP	HLF
00	PC	3J	10	MX	5J	11	MX	01	PC	6J	MX	HLF	FMP	HLF	FMP

Table 12.3 TWO LINES HALF DUPLEX/ONE LINE FULL DUPLEX

NAME U-LINK	NUMBER OF U-LINKS	FUNCTIONS OF U-LINKS	SETTING OF U-LINKS
ADA	4	Selection Control Unit Address	
RD	3 per line	Selection Configuration	
MX/PC	1 per line		Link pos. MX (=IOP connection) may only be selected if ASCU4Z has the basic address of /00 or /04
RD	3 per line	Selection V24/V28, Current Loop	
CL3	1 per line	- Selection V24/V28	Links RD pos. V28 Links CL3 pos. V28
		- Selection Current Loop	Links RD pos. CL Links CL3 pos. V28
		- Selection Current Loop (External Power Supply)	Links RD pos. CL Links CL3 pos. EX
CPTR	4 per line	Selection Data transmission / reception speed	
WL	1 per line	Selection character length	
BD	1 per line	Break detection option	Only for half duplex
ECHO	1 per line	Echo option	Only for half duplex
ITV	1	Factory Test Facilities	Must be in position as shown in figure 12-1
EXC1/TF	1		
TRCP	1 per line		
ITR	1	Factory Test Facilities	Links are hard wired must not be disconnected
ALE	1		
ROM	1		
SID	i		
CT133	1 per line	Device Ready (PER 3100)	

Table 12.4 CHECK LIST U-LINKS

12.4 INTERFACE CONNECTIONS

a) V24 Interconnections
b) Current Loop Interconnections
c) Cables (Asynchronous mode)
d) Connector for an external current supply: J7

a) V24 INTERCONNECTIONS:

Interconnections between ASCU4Z and the peripheral is with a V24/V28 cable

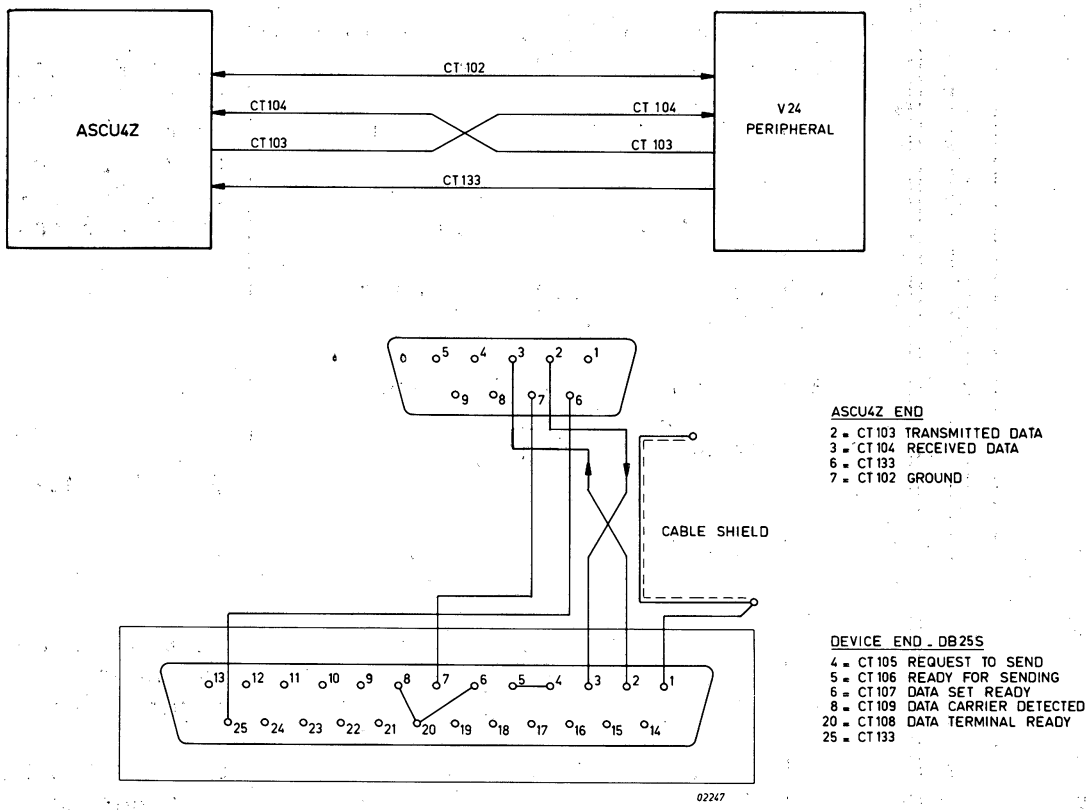


Figure 12.3 V24 INTERCONNECTIONS

b) CURRENT LOOP INTERFACE INTERCONNECTIONS

Interconnections between ASCU4Z and the Current Loop Peripheral is with a Current Loop Cable.

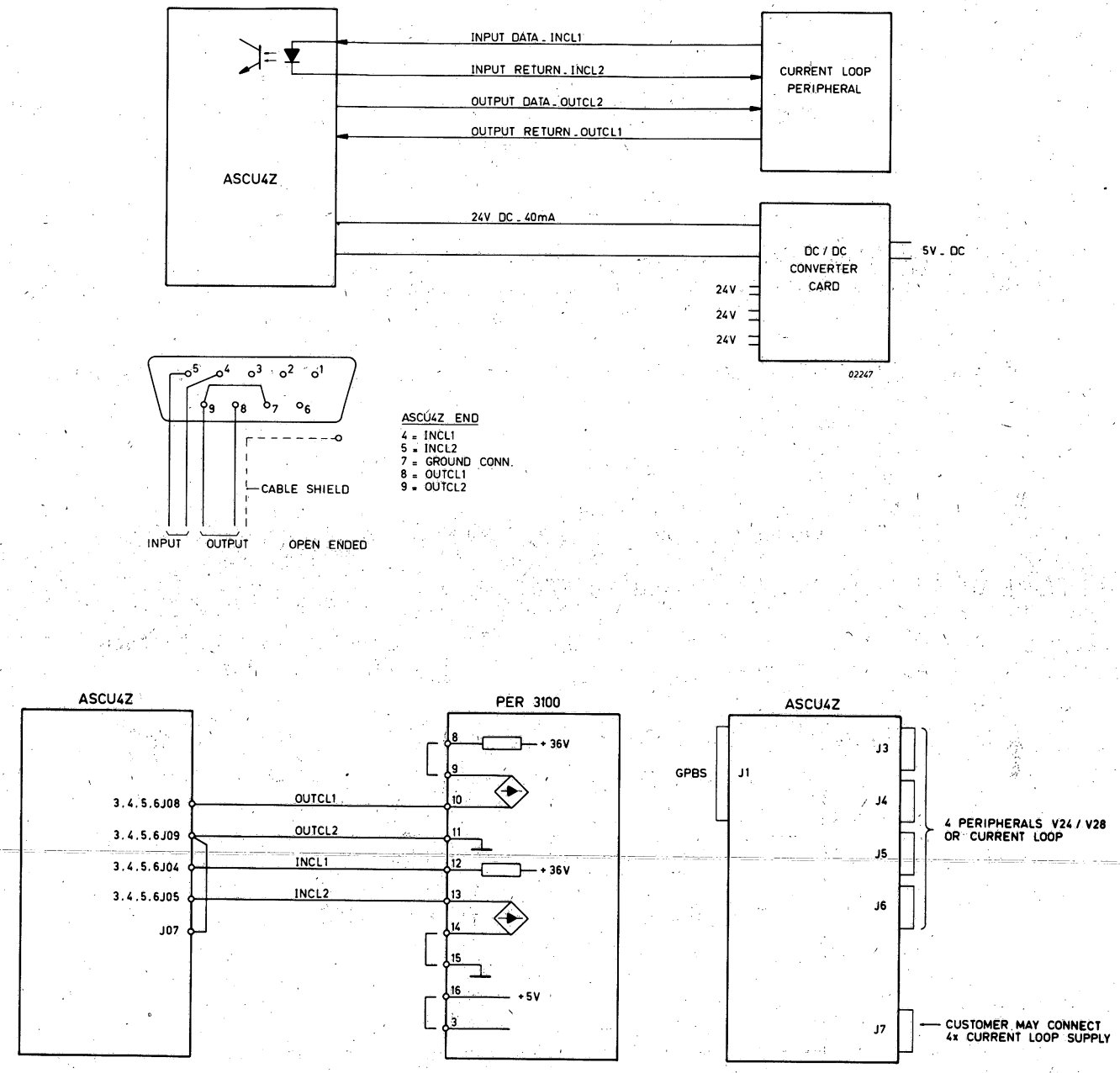


Figure 12.4 CURRENT LOOP INTERCONNECTIONS

c) CABLES (ASYNCHRONOUS MODE)

In the catalogue a maximum length of 100 m is mentioned for 9600 bps. For different transfer rates the following list may be an aid.

INTERFACE	V 28	CURRENT LOOP	
Cables	A	A	B
600 Bds	250 M	1 300 M	2 500 M
1 200 Bds	200 M	1 000 M	2 000 M
2 400 Bds	180 M	900 M	1 800 M
4 800 Bds	160 M	750 M	1 500 M
9 600 Bds	120 M	600 M	800 M

Table 12.5 CABLE LENGTHS

Cables: The following characteristics correspond to the standard cables used:
A = 243 Ohm/KM
110 pF/M between a pair
150 pF/M between a pair and ground
B = CMC04 46 Ohm/KM
20 pF/M between two conductors
130 pF/M between a conductor and ground

d) CONNECTION TO AN EXTERNAL CURRENT SUPPLY

For the purpose to insert a current supply into a current loop interface, it is possible to use an external power supply (24V, DC, 40m A per line).

Connector for an external current supply:

Pin Number	Inputs	Direction
7 J01	+V	Line 0
7 J02	Ground	
7 J03	+V	Line 1
7 J04	Ground	
7 J05	+V	Line 2
7 J06	Ground	
7 J07	+V	Line 3
7 J08	Ground	

Note: When an external power supply is used, the "U" links 1CL3, 2CL3, 3CL3, 4CL3 must have the position EX.

Table 12.6 CONNECTOR J7

CARD CONNECTORS				PERIPHERAL CONNECT	SIGNAL NAME	FUNCTION
3J07	4J07	5J07	6J07	07	CT 102	Command Retun (ground conn.)
3J02	4J02	5J02	6J02	02	CT 103	Transmitted Data
3J03	4J03	5J03	6J03	03	CT 104	Received Data
3J06	4J06	5J06	6J06	25	CT 133	Peripheral Ready to send or receive the next character

Table 12.7 V24 DEVICE INTERFACE J3, 4, 5, 6

CARD CONNECTORS				PERIPHERAL CONNECT	SIGNAL NAME	FUNCTION
3J04	4J04	5J04	6J04	12	INCL1	Incoming data
3J05	4J05	5J05	6J05	13	INCL2	Incoming data
3J08	4J08	5J08	6J08	10	OUTCL1	Outgoing Data
3J09	4J09	5J09	6J09	11	OUTCL2	Outgoing Data

Table 12.8 CURRENTLOOP INTERFACE J3, 4, 5, 6

APPLICATION NOTES

ASCU4Z may be used in V24 or Current Loop configurations. Two configuration examples are given in the following figures, these are:

* Current Loop, ASCU4Z/ASCU4Z Connection
* Current Loop, ASCU4Z/AMA8C Connection

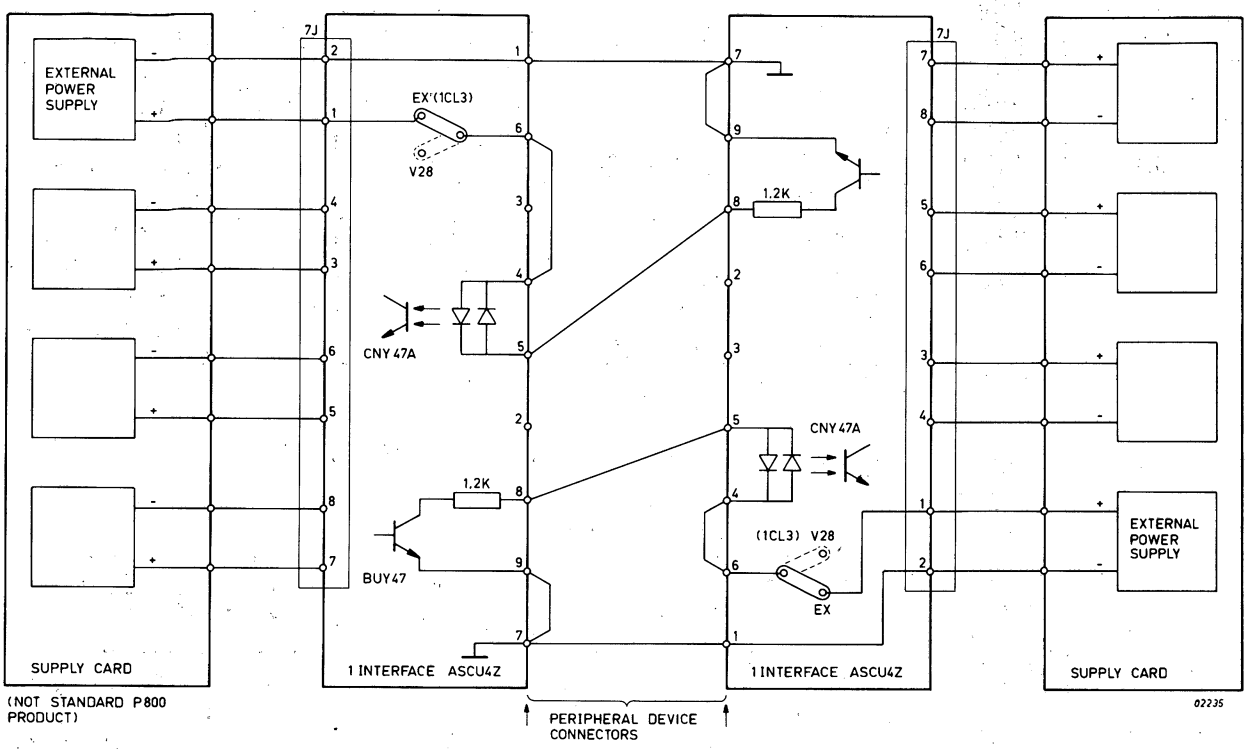


Figure 12.5 ASCU4Z/ASCU4Z, CURRENT LOOP

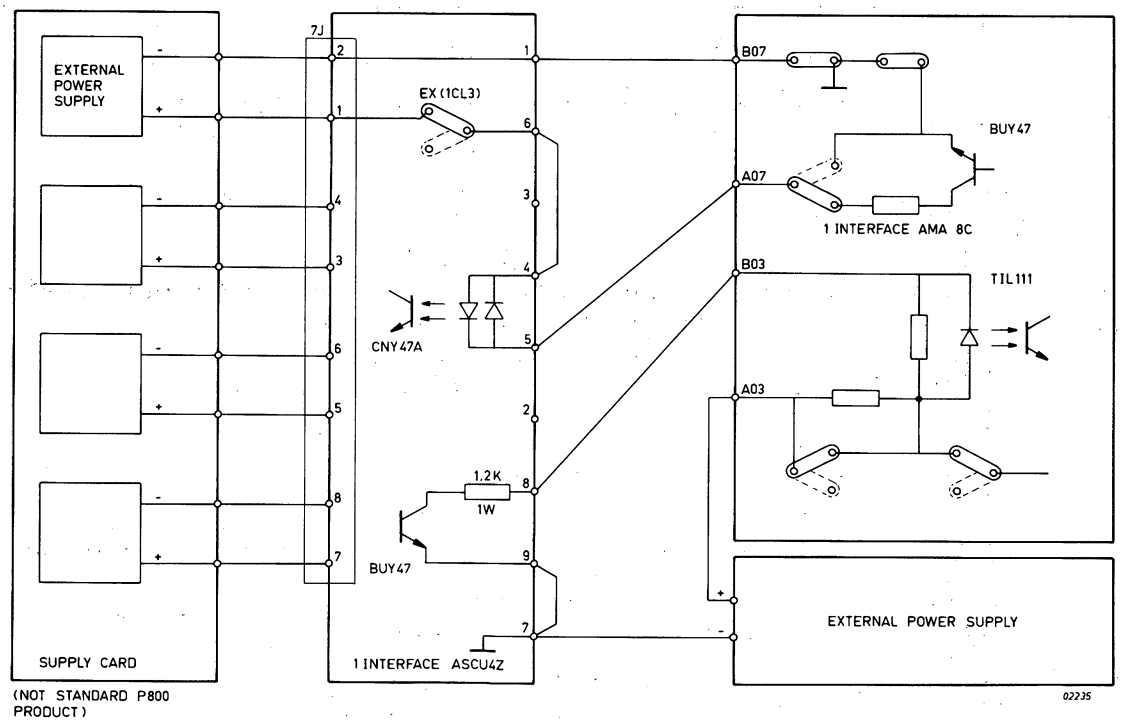
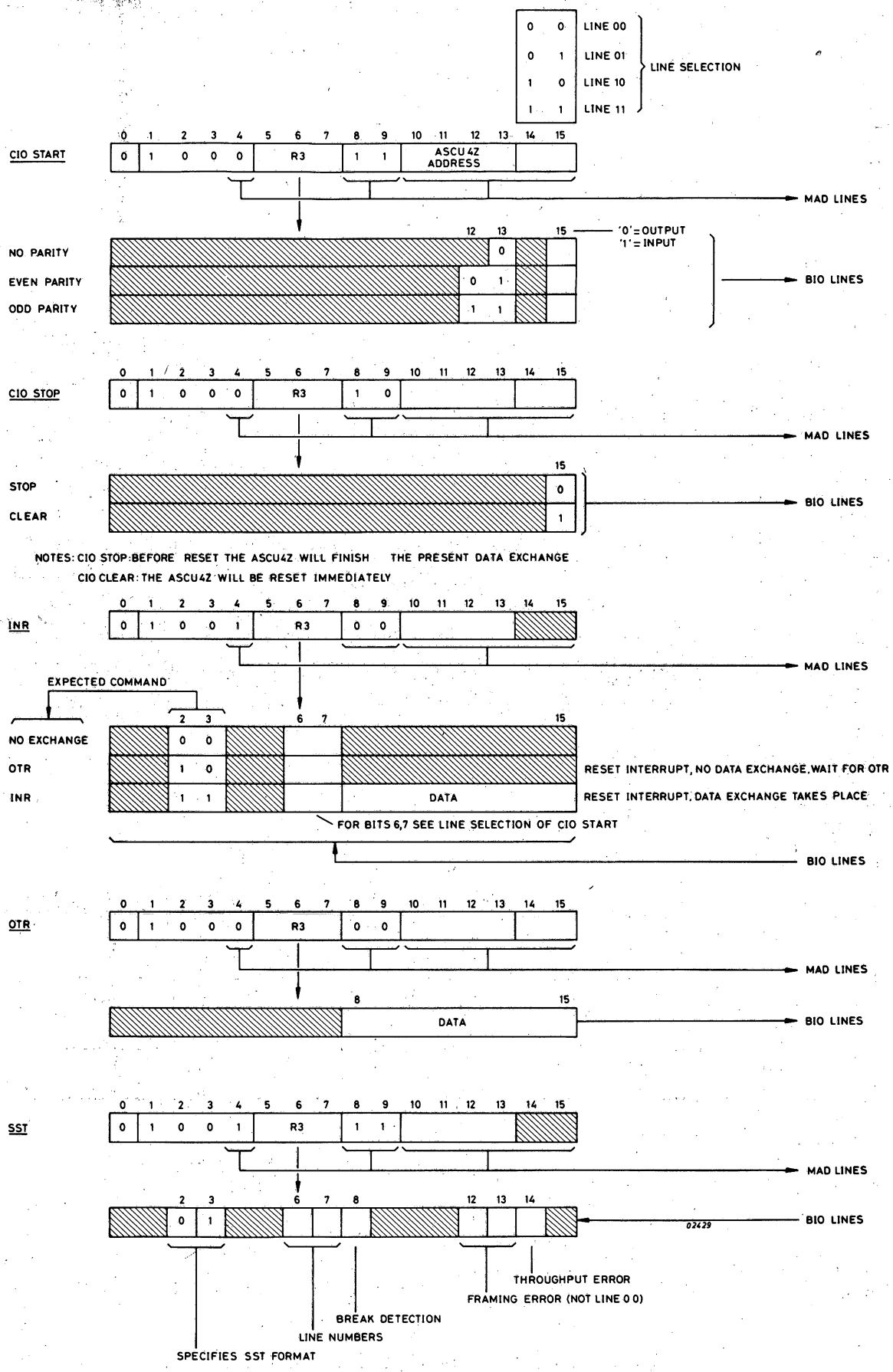


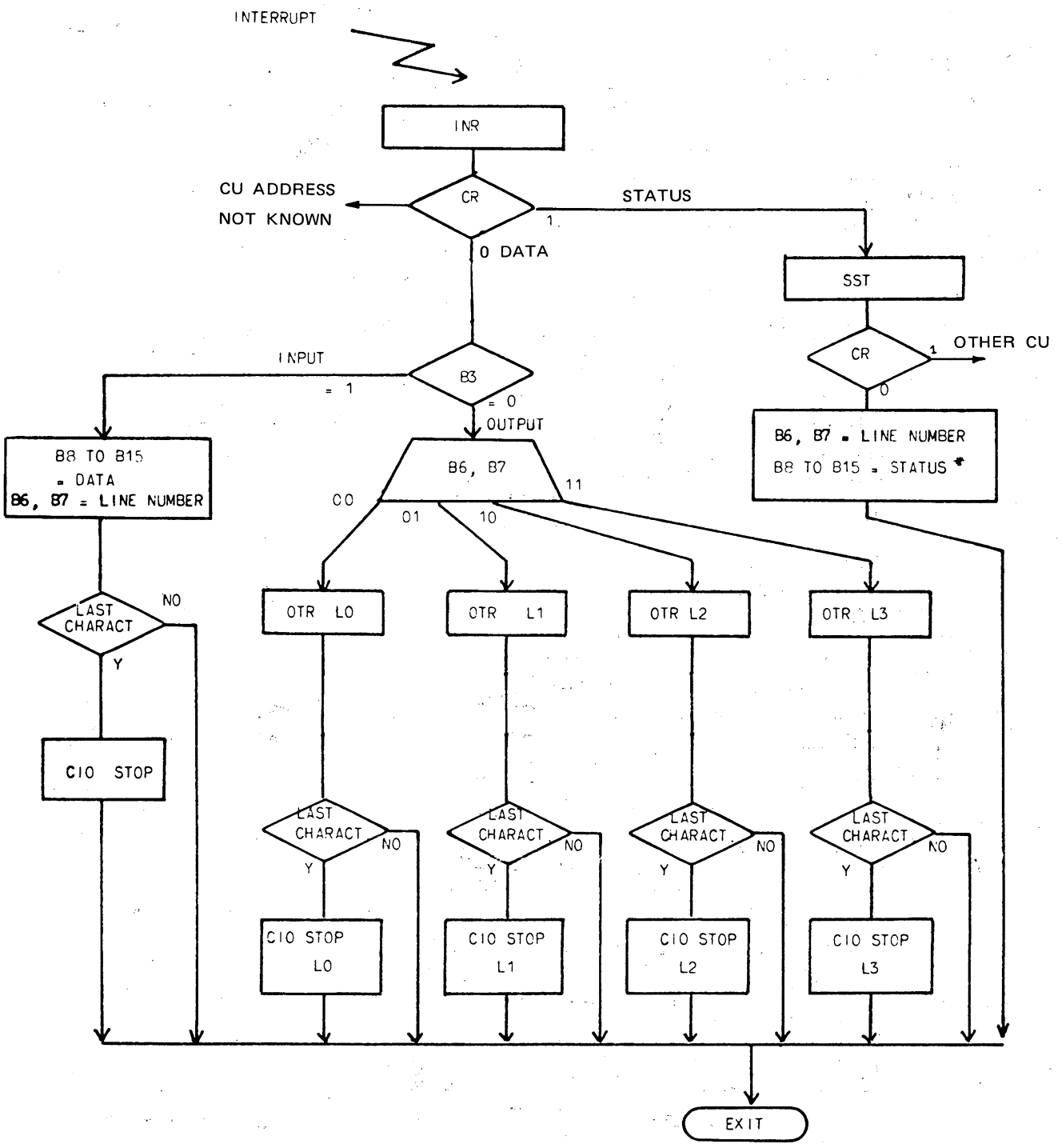
Figure 12.6 ASCU4Z/AMA8C, CURRENT LOOP

12.5 HARDWARE SOFTWARE INTERFACE DETAILS



Interrupt routine on Programmed Channel

CIO STOP instruction will be executed with line number indicated on the INR instruction.



* Status, Troughput Error, Parity Error, Break Detection, Framing Error

Figure 12.7 PROGRAMMING FLOWCHART

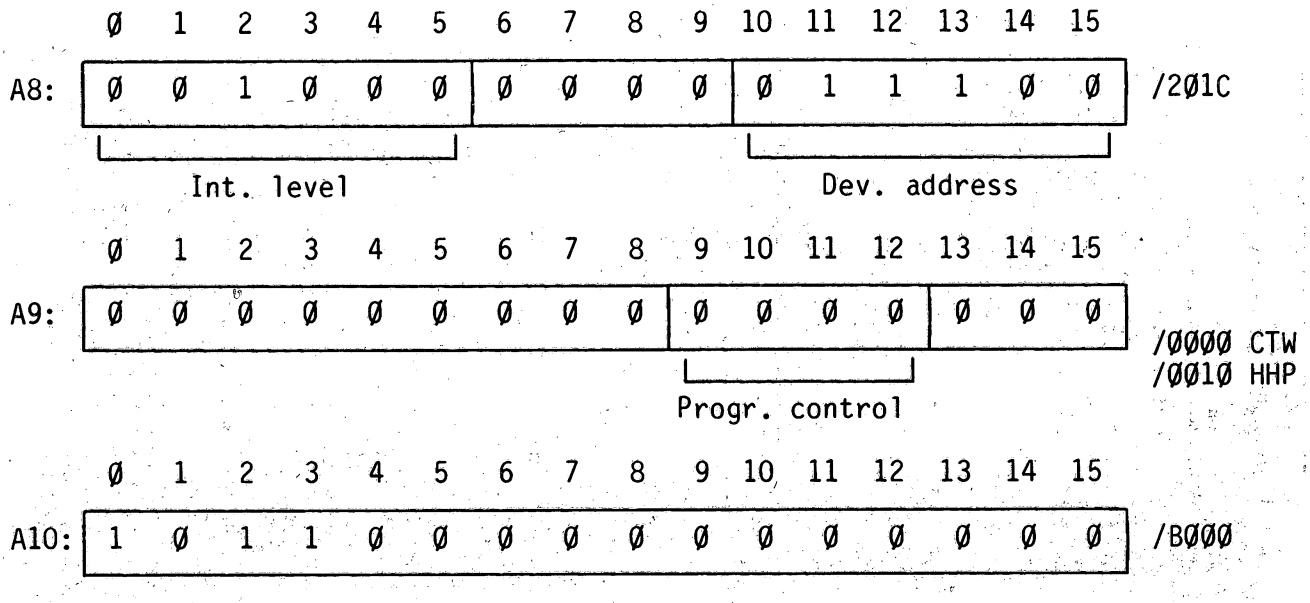
12.6 SHORT DESCRIPTION OF TESTPROGRAM

TESTPROGRAM BASCU4Z:

- Settings: HLF on RD 1,2,3,4 prog.channel no CT133
  non-echo no BD 8 bits data

Procedure:

- IPL
  Program displays /7ØØ
  Modify registers

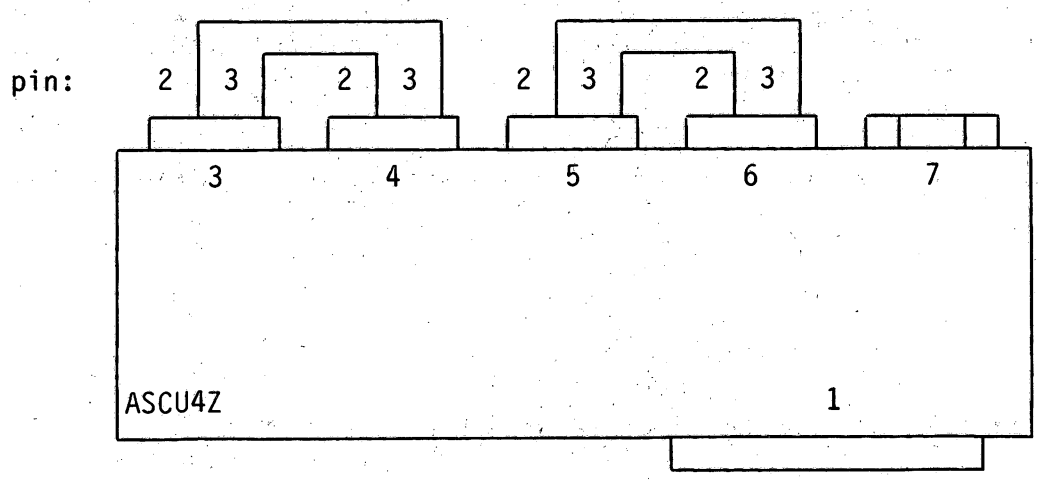


1 = Tests selected

Start program

Display /5EØ = information stop
Display /5FØ = error stop
The error code is displayed. After error: reload the program, before retry.

Interconnect



Information Messages

IFØXYZ

X = check no.
Y = phase no.
Z = type of info

Hnfo Type	Meaning
Ø	Change strap position
1	-
2	-
3	Parity error
4	Framing error
5	-
6	Throughput error
7	-
8	Put ground on pin
9	Break key detected
A	Wait for 64 data input
B	Break detect
C	-
D	-
E	-
F	-

Program checks - Standard

Check ØØØ - Address recognition 4 lines
ØØ - Check data exchange PC
2ØØ - Check data exchange 4 lines simult. PC
3ØØ - Check on parity error
4ØØ - Check echo and break detection
5ØØ - Check data exchange - MX

Program checks - Special

Check 6ØØ - Check full duplex
7ØØ - Check interrupt break key line Ø and framing error lines 1,2,3
8ØØ - Check throughput error

ERØXY2

X = check nr.
Y = phase nr.
Z = error type

Error Type	Meaning
Ø	I/O instruction rejected
1	Break key not detected (line Ø)
2	Address not recognised
3	Parity error
4	Framing error
5	Incorrect length
6	Throughput error
7	Contents of SST incorrect
8	Data error
9	Hardware failure
A	Throughput error not detected
B	Break detection
C	Framing not detected

Procedure 5111 991 1ØØ91 = Procedure BASCU4 5111 991 11161
with addendum PTS8ØØØ 5111 991 11381

Listing 5111 991 11Ø81
Program 5111 199 65671

```
                        IDENT    ASCU
                      * THIS PROGRAM TRANSMITS AND RECEIVES CHAR 'U' CONTINUOUSLY
                      * LINE 1 FULL DUPLEX(LINE 00=REC, LINE 01=TRX)
                      * INT LEVEL 8 , DA /1C
                      * INTERCONNECT ON TRX-CU (LINE 01) PIN 4J02 TO REC-CU 00 PIN 4J03
                      *TEST CORRECT RUNNING: CHECK IF A3=/55
                      * (STOP PROGRAM BY CHANGING ADDR /D0 DATA (WAS:/EA0C) IN /207F (=HLT)
                      *          ---- OR -----
                      * CHECK OSCILLOSCOPE PICTURE CT103 ON PIN 4J02
                      *
                      *      +12V    I---I   I---I   I---I   I---I   I---I STOPBITS
                      *      -12V  --I   I---I   I---I   I---I   I---I   I---I---I-
                      *              ST   1   0   1   0   1   0   1   P
                      *                I----------CHAR 'U'---------I PE
                      *
                      *  ERROR: DATA FAULT-STOP IN /DE (/E0 ON HHP)
                      *         STATUS FAULT-STOP IN /DC (/DE ON HHP)
                      *
                      *  TEST OF LINE 10/11: CHANGE DA'S IN PROGRAM, USE CONNECTOR J6
                      *
                      *
0000                            RES     /40
     001C             DA        EQU     /1C
0080 FFFF             DATA      DATA    /FFFF
0082 0000                       DATA    0
                      *
                      *  MAIN PROGRAM
0084 207F             START     HLT
0086 87A0                       LDKL    A15,/120              LOAD STACKPOINTER
0088 0120
008A 8120                       LDKL    A1,INTAD
008C 00A4  R
008E 8141                       ST      A1,/10                STORE INT ROUTINE ADDRESS
0090 0010
0092 0404                       LDK     A4,4                  EVEN PARITY,OUT
0094 0505                       LDK     A5,5                  EVEN PARITY,IN
0096 0255                       LDK     A2,/55                CHAR 'U'
0098 2840                       ENB
009A 45DC                       CIO     A5,1,DA               START INPUT LINE 00
009C 5C04                       RB(4)   *-2
009E 44DD                       CIO     A4,1,DA+1             START OUTPUT LINE 01
00A0 5C04                       RB(4)   *-2
00A2 5F02                       RB      *
                      *
                      *  INTERRUPT ROUTINE
00A4 4B1C             INTAD     INR     A3,0,DA
00A6 8C20                       ABL(4)  STATUS
00A8 00D8  R
00AA 840C                       LDR     A4,A3
00AC 850C                       LDR     A5,A3
00AE A420                       ANKL    A4,/1000              CHECK: INPUT OR OUTPUT
00B0 1000
00B2 8C20                       ABL(4)  INPUT
00B4 00CC  R
                      *
00B6 A520             OUTPUT    ANKL    A5,/300               LOOK FOR LINENO.
00B8 0300
00BA 3068                       SRL     A5,8                  SHIFT RIGHT LINENO.
00BC 8420                       LDKL    A4,DA+/4200           /42DA=OTR A2,0,DA
00BE 421C
00C0 9414                       ADR     A4,A5                 ADD OTR AND LINENO.
00C2 8441                       ST      A4,OTR                STORE OTR
00C4 00C6  R
00C6 5700             OTR       RF      *+2                   REPLACED BY OTR
00C8 5C04                       RB(4)   *-2
00CA F03E                       RTN     A15
                      *
00CC A320             INPUT     ANKL    A3,/FF
00CE 00FF
00D0 EA0C                       CWR     A2,A3                 COMPARE OUTPUT AND INPUT DATA
00D2 8C20                       ABL(4)  ERR                   INPUT DIFFERENT FROM OUTPUT
00D4 00DE  R
00D6 F03E                       RTN     A15
                      *
                      *
00D8 4CDC             STATUS    SST     A4,DA
00DA 5C04                       RB(4)   *-2
00DC 207F                       HLT
00DE 207F             ERR       HLT
                                END     START
```

```
00000                          IDENT    ASCU2
00001                     *SHORT ROUTINE FOR INPUT AND OUTPUT ON ASCU4Z CARD
00002                     *
00003                     * PARAMETERS TO ENTER AFTER PROGRAM LOADING ONLY:
00004                     *
00005                     *                          INT LEVEL,PARITY,DEV.ADDR./LINE :PARITY: NO EVEN ODD
00006                     *          REG BITS:    0  TO   5, 6&7  ,   10   TO  15  BIT 6,7=00  01   11
00007                     *
00008                     *  REG  A1 (INPUT LINE) : E.G. /2004 = INT. LEV. 8, NO PARITY, DA /04
00009                     *  REG  A2 (OUTPUT LINE): E.G. /2005 = INT. LEV. 8, NO PARITY, DA /05
00010                     *
00011                     *
00012  0000                            RES      /40
00013  0080  FFFF                      DATA     /FFFF
00014  0082  0000                      DATA     0
00015  0084  87A0           START      LDKL     A15,500              STACKPOINTER
       0086  01F4
00016  0088  8120                      LDKL     A1,/2004             INT LEV 8, DA 04
       008A  2004
00017  008C  8220                      LDKL     A2,/2005             INT LEV 8, DA 1C, LINE 01
       008E  2005
00018  0090  207F                      HLT
00019                     ****PREPARE INPUT ROUTINE****
00020  0092  043F                      LDK      A4,/3F               MASK DEV. ADDR.
00021  0094  A404                      ANR      A4,A1                A4= DEV. ADDR.
00022  0096  AC41                      ORS      A4,CIOIS             MODIFY THE IO INSTRUCTIONS
       0098  0100  R
00023  009A  AC41                      ORS      A4,CIOIH
       009C  015C  R
00024  009E  AC41                      ORS      A4,INRI
       00A0  012C  R
00025  00A2  AC41                      ORS      A4,SSTI
       00A4  0160  R
00026  00A6  9410                      ADR      A4,A4                SHIFT LEFT ONE BIT POS.
00027  00A8  AC41                      ORS      A4,WER1IN
       00AA  00F6  R
00028  00AC  AC41                      ORS      A4,WER2IN
       00AE  00FC  R
00029                     ****PREPARE OUTPUT ROUTINE****
00030  00B0  043F                      LDK      A4,/3F               MASK DEV. ADDR.
00031  00B2  A408                      ANR      A4,A2                A4= DEV ADDR. OUTPUT
00032  00B4  AC41                      ORS      A4,CIOOS             MODIFY THE IO INSTR.
       00B6  0120  R
00033  00B8  AC41                      ORS      A4,CIOOH
       00BA  0150  R
00034  00BC  AC41                      ORS      A4,INRO
       00BE  0132  R
00035  00C0  AC41                      ORS      A4,OTR
       00C2  0144  R
00036  00C4  AC41                      ORS      A4,SSTO
       00C6  0166  R
00037  00C8  9410                      ADR      A4,A4                SHIFT LEFT ONE BIT POS.
00038  00CA  AC41                      ORS      A4,WER1OU
       00CC  0116  R
00039  00CE  AC41                      ORS      A4,WER2OU
       00D0  011C  R
00040                     ****PREPARE INT. ROUTINE ADDRESSES****
00041  00D2  8404                      LDR      A4,A1
00042  00D4  3C6A                      SRL      A4,10
00043  00D6  9410                      ADR      A4,A4                A4 = INT ENTRY ADDR.
00044  00D8  8320                      LDKL     A3,INRI
       00DA  012C  R
00045  00DC  8331                      STR      A3,A4                INTERRUPT ROUTINE ADDR
00046  00DE  8408                      LDR      A4,A2
00047  00E0  3C6A                      SRL      A4,10
00048  00E2  9410                      ADR      A4,A4                A4 = INT ENTRY ADDR.
00049  00E4  8320                      LDKL     A3,INRO
       00E6  0132  R
00050  00E8  8331                      STR      A3,A4                INTERRUPT ROUTINE ADDR.
00051  00EA  2840                      ENB
00052                     ****START INPUT LINE****
00053  00EC  8504           AGAIN      LDR      A5,A1
00054  00EE  3D66                      SRL      A5,6
00055  00F0  250C                      ANK      A5,/C                PARITY PARAMETERS
00056  00F2  1501                      ADK      A5,1                 INPUT COMMAND
00057  00F4  0401                      LDK      A4,1                 INPUT,CHAR.MODE,BL=1
00058  00F6  7400           WER1IN     WER      A4,0
00059  00F8  8420                      LDKL     A4,BUF+1             DATA ADDRESS
       00FA  017F  R
00060  00FC  7401           WER2IN     WER      A4,1
00061  00FE  0400                      LDK      A4,0                 FLAG:SSTI ACCEPTED
00062  0100  45C0           CIOIS      CIO      A5,1,0
00063  0102  5C04                      RB(NA)   *-2
00064  0104  8410                      LDR      A4,A4                TEST FLAG
00065  0106  5804                      RB(Z)    *-2
00066  0108  0500                      LDK      A5,0
00067                     ****START OUTPUT LINE****
00068  010A  8508                      LDR      A5,A2
00069  010C  3D66                      SRL      A5,6
00070  010E  250C                      ANK      A5,/C                PARITY PARAMETERS, OUTPUT COMMAND
00071  0110  8420                      LDKL     A4,/4010             OUTPUT, CHAR. MODE, BL=16
       0112  4010
00072  0114  0700                      LDK      A7,0                 COUNTER PROG CHANN. OUTPUT
00073  0116  7400           WER1OU     WER      A4,0
```

```
00074  0118  8420          LDKL    A4,BUFOUT          DATA ADDRESS
       011A  0172  R
00075  011C  7401  WER20U  WER     A4,1
00076  011E  0400          LDK     A4,0               FLAG SSTI ACCEPTED
00077  0120  45C0  CI00S   CIO     A5,1,0
00078  0122  5C04          RB(NA)  *-2
00079  0124  8410          LDR     A4,A4              TEST FLAG
00080  0126  5804          RB(Z)   *-2
00081  0128  0500          LDK     A5,0
00082  012A  5F40          RB      AGAIN
00083                      ****INTERRUPT ROUTINE****
00084  012C  4800  INRI    INR     A3,0,0
00085  012E  5430          RF(NA)  SSTI
00086  0130  5704          RF      *+6
00087  0132  4800  INR0    INR     A3,0,0
00088  0134  5430          RF(NA)  SST0
00089  0136  860C          LDR     A6,A3
00090  0138  A620          ANKL    A6,/1000           INPUT OR OUTPUT?
       013A  1000
00091  013C  5416          RF(NZ)  INPUT
00092  013E  E35C  OUT     LC      A3,BUFOUT,A7
       0140  0172  R
00093  0142  23FF          ANK     A3,/FF
00094  0144  4300  OTR     OTR     A3,0,0
00095  0146  1701          ADK     A7,1
00096  0148  EF20          CWK     A7,16              ALL OUTPUT CHARS DONE ?
       014A  0010
00097  014C  5404          RF(NE)  *+6
00098  014E  0500          LDK     A5,0
00099  0150  4580  CI00H   CIO     A5,0,0
00100  0152  F03E          RTN     A15
00101  0154  23FF  INPUT   ANK     A3,/FF
00102  0156  E341          SC      A3,BUF+1
       0158  017F  R
00103  015A  0500          LDK     A5,0
00104  015C  4580  CI0IH   CIO     A5,0,0
00105  015E  F03E          RTN     A15
00106                      ****STATUS ROUTINE****
00107  0160  4CC0  SSTI    SST     A4,0
00108  0162  5C04          RB(NA)  *-2
00109  0164  F03E          RTN     A15
00110  0166  4CC0  SST0    SST     A4,0
00111  0168  5402          RF(NA)  DELAY
00112  016A  F03E          RTN     A15
00113  016C  1401  DELAY   ADK     A4,1               WAITLOOP AFTER NOT ACC SST
00114  016E  5C04          RB(NZ)  *-2
00115  0170  5F46          RB      INRI
00116                      ***DATA BUFFER***
00117  0172  4153  BUFOUT  DATA    'ASCU4Z TEST '
       0174  4355
       0176  345A
       0178  2054
       017A  4553
       017C  5420
00118  017E  2058  BUF     DATA    ' X'
00119  0180  0A0D          DATA    /0A0D
00120                      END     START
```

13 SERIAL CONTROL UNIT P845-140 (SCUZ)

SECTION	13.1	SCUZ IDENTIFICATIONS	PAGE 13-2
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13.1 S.C.U.Z. IDENTIFICATIONS

Typenumber : P845-140
Testprogram : BZSCU for serial V24 or current loop interfaced ASR 33, PER 3100, or VDU.
I/O-channel : program channel; Interrupt connection: 1C05
speed: 110-9600 Baud.
Devices : PER 3100, P842-001 (V24 or current loop)
ASR 33, P841-101 (V24 or current loop)
VDU , P817-002 (V24 or current loop)

Power consumption : +5V 800mA
+12V, 25mA
-12V, 45mA

12NC code on the sticker on the board:
SCUZ : 511 199 6855X (5322 216 25125)
X = modification level.

13.2 INSTALLATION DETAILS

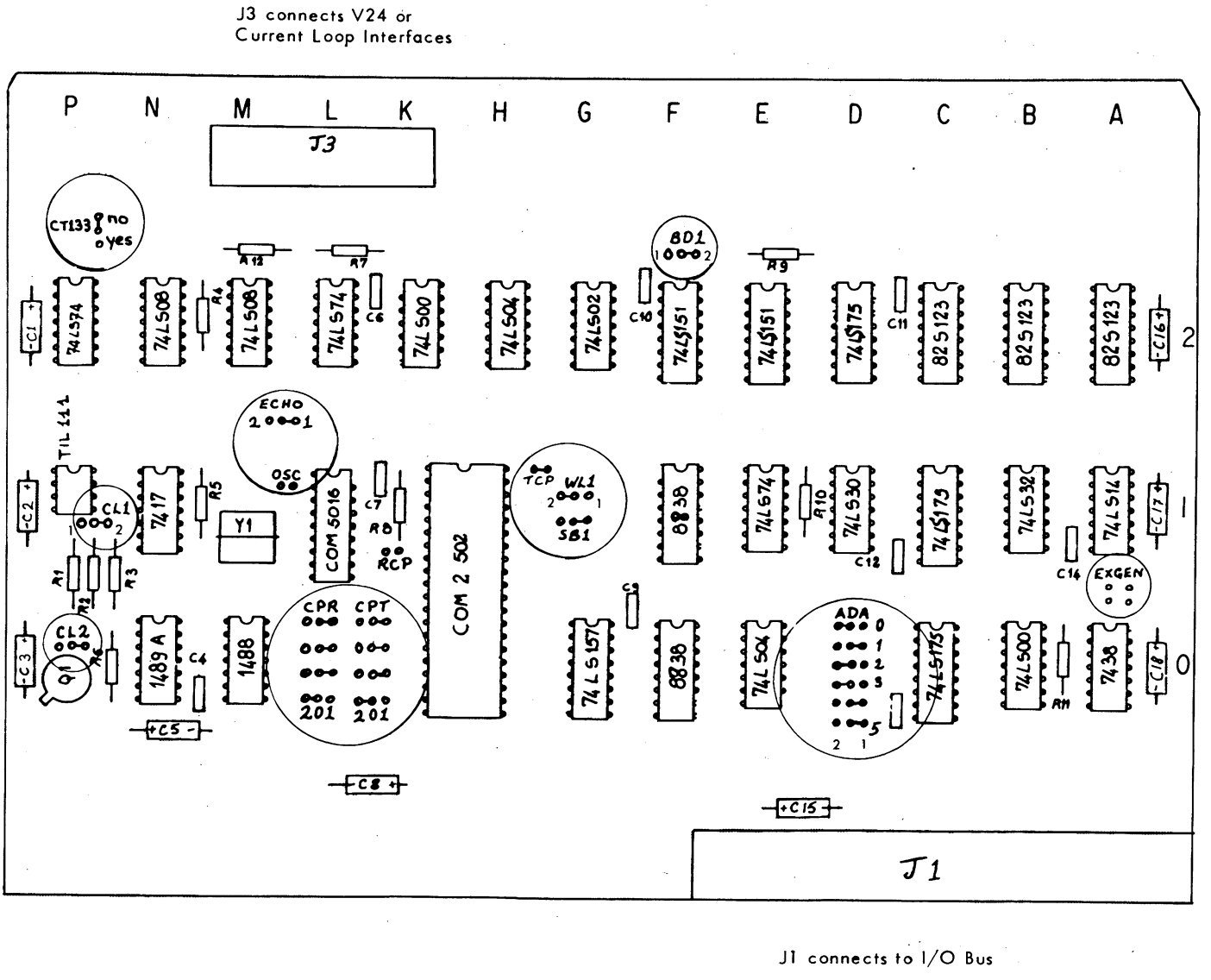


Figure 13.1 U-LINK SETTING SCUZ

Link Name	Meaning	Selection
SB1	Select no of stop bits per character	2 stop bits (0 1) / 1 stop bit (0 2)
WL1	Select no of data bits per character	8 data bits (0 1) / 7 data bits (0 2)
BD1	Recognise a character input while in output mode?	Yes (0 1) / No (0 2)
ECHO	Echo Mode?	Yes (0 1) / No (0 2)
CL1	Select V24 or Current Loop Interface	Current Loop (0 1) / V24 (0 2)
CL2	Current Loop? Then select 2 or 4 wire interface.	2 Wire (0 1) / 4 Wire (0 2)
TCP	Testing with an external generator?	Yes / No
RCP	Testing with an external generator?	Yes / No
CT133	Using signal CT133 from device to request transfer in output mode?	Yes (10 9) PER 3100 / No (10 11)
EXGEN	Testing with an external generator?	Yes / No *
OSC	Crystal oscillator connected?	Yes / No *
ADA	6 links must be fitted to select the address code	0 1 2 3 4 5 (2 0 1) ← most significant. This example shows the links connected for address 000000
CPT and CPR	4 links must be fitted to CPT and 4 to CPR in the same positions to select the indicated frequency	Link Positions to Select Indicated Frequency (Hz)

CPR (2 0 1)	CPT (2 0 1)	50	75	110	134.5	150	300	600	1,200	1,800	2,000	2,400	3,600	4,800	7,200	9,600	19,200
2 0 1	2 0 1	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1
2 0 1	2 0 1	2	2	2	2	1	1	1	1	2	2	2	2	1	1	1	1
2 0 1	2 0 1	2	2	1	1	2	2	1	1	2	2	1	1	2	2	1	1
2 0 1	2 0 1	2	1	2	1	2	1	2	1	2	1	2	1	2	1	2	1

Note: 1 means link is between 0 and 1
2 means link is between 0 and 2

* not on later boards

Table 13.1 U-LINK SETTING SCUZ

13.3 INTERFACE CONNECTIONS

Signals	SCUZ Connector J3	D8255 Device Connector Per3100 (P817)	Remarks
Signal Ground	07		Strap
Return (MCLO)	11	11 (14)	Yellow
Received Data (CL1)	12	12 (16)	White
Return (MCL1)	13	13 (13)	Blue
Transmitted Data (CLO)	10	10 (12)	Red
Protective Earth			Connected to Braid

Table 13.2 CURRENT LOOP INTERFACE - 2 WIRE

Signals	SCUZ Connector J3	D8255 Device Connector	Remarks
Ground			Connected to Braid
		08	Strap
		09	
Transmitted Data (CLO)	10	10	Red
Return (MCLO)	11	11	Yellow
Signal Ground	07		Strap
Received Data (CL1)	12	12	White
Return (MCL1)	13	13	Blue
		14	Strap
		15	
		03	Strap
		16	

Table 13.3 CURRENT LOOP INTERFACE - 4 WIRE

Signals	SCUZ/ Connector J3	D8255 Device Connector	Remarks
CT101		01	Braid connected to Ground
CT102	07	07	Signal Earth or Common Return
CT103	02	03	Data SCUZ to Peripheral (Yel)
CT104	03	02	Data Peripheral to SCUZ (Blue)
CT105		04	Strap
CT106		05	
CT107		06	Strap
CT108/2		20	
CT109		08	Strap
CT133	25	25	Ready for Receiving (White)

Table 13.4 V24 INTERFACE

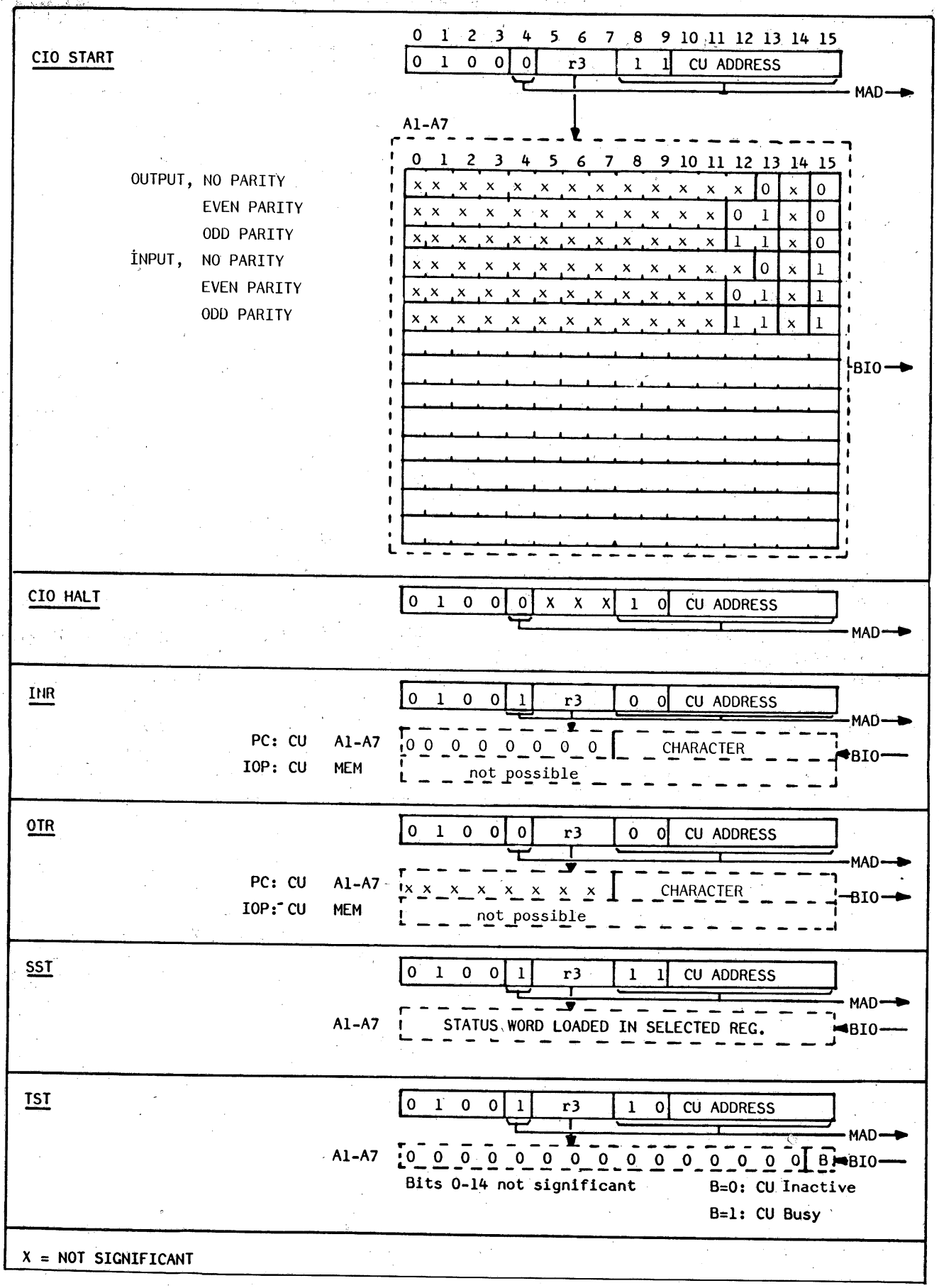


Figure 13.2 INSTRUCTION-/COMMAND WORD FORMATS SCUZ

13.4.1 STATUSWORD:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0		0	0	0	0		0	0

Break Detection

parity error

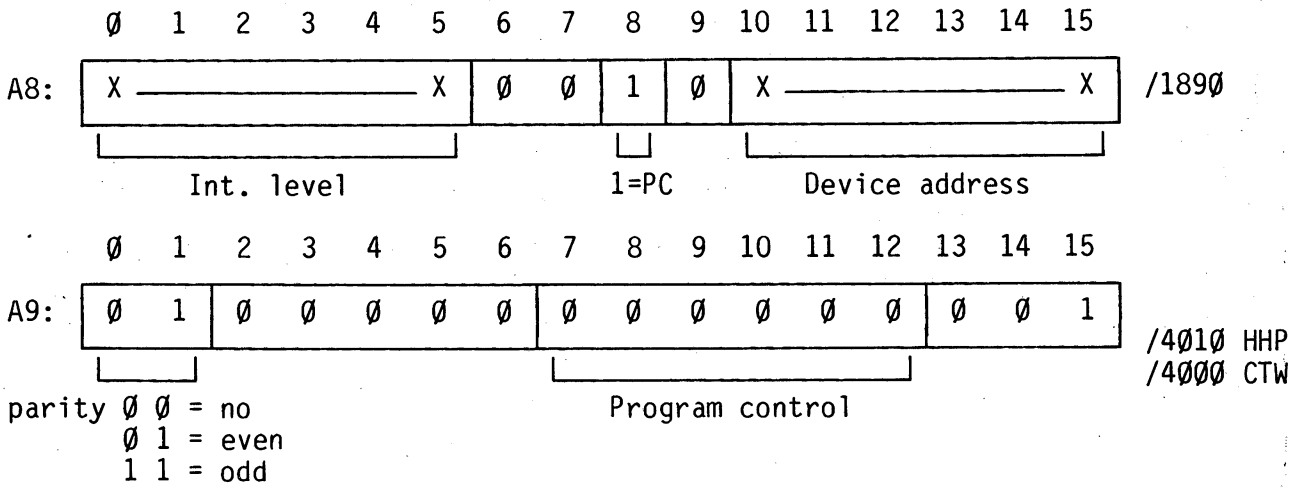
13.5 SHORT DESCRIPTION OF TESTPROGRAMS

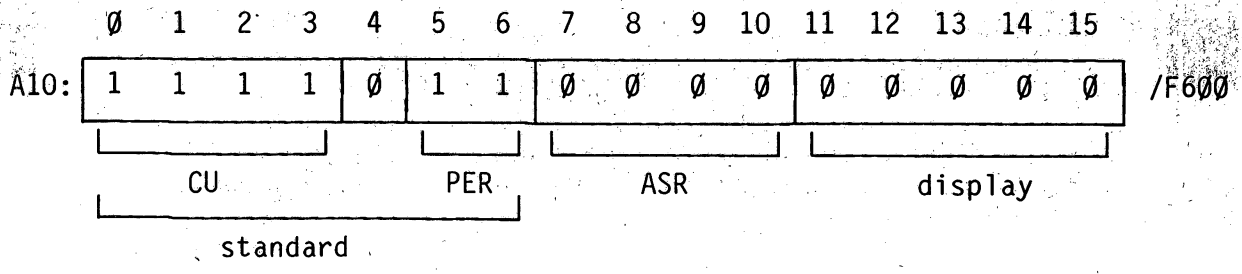
TESTPROGRAM BZSCU

CTW: interrupt level 6
dev. address /1Ø (if P853), dev. address /10 not allowed on P854 (integrated CU = /10).
even parity
Transfer 96ØØ bps max.
RTC, PF/AR allowed.
- May be used to test the integrated control unit of CP57E.
- Intended for test of SCUZ card from level 5 and on.

Procedure:

- IPL
  RTC on
- Program displays /7ØØ (= restart, normal end of tests. Framing error and interrupt also return to /7ØØ.)
- Change registers





Type in: test 1, char. within 1Ø sec.
3, text, line feed, carr. return, '$' on CTW keyboard.
Error stop at /5FØ
Information stop at /5EØ
If VDU used as CTW for P857E CPU: - Do not use CT133
- Preset A1O with /A7DF (keyboard not tested)
This program may also be used to test the integrated V24-Control Unit of the P854 CPU

BZSCU tested:

If ØØØØ check Ø : Output Mode Controller Test
If ØØØ1 check 1 : Input Mode Controller Test
If ØØØ2 check 2 : Inhibit Mode Controller Test
If ØØØ3 check 3 : Echo Mode Test
If ØØØ4 check 4 : Input Mode Parity Test
If ØØØ5 check 5 : PER 31ØØ Printer Function Test (11Ø characters)
If ØØØ6 check 6 : Character Loss Test (11Ø characters)
If ØØØ7 check 7 : ASR "Worst Pattern"
If ØØØ8 check 8 : ASR 75 character per line
If ØØØ9 check 9 : ASR "Dash-pot"
If ØØ1Ø check 10 : ASR "Punch" and "Reader" Test
If ØØ11 check 11 : Display, all display functions
If ØØ12 check 12 : Display, screen vertically test
If ØØ13 check 13 : Display, screen horizontally test
If ØØ14 check 14 : Display, oblique alignment test
If ØØ15 check 15 : Display, character lost test

Procedure 5111 991 1Ø191 = Procedure BZSCU 5111 991 Ø8377
with addendum PTS8ØØØ 5111 991 11381
Listing 5111 991 1Ø2Ø1
Program 5111 199 656Ø1

13.6 SHORT ROUTINES

ASR, PTS 3100 AND DISPLAY

These peripherals and their CU's can be checked with the aid of two small programs called Line, and Echo, if the standard test program either cannot be loaded or if it will not run.

PROGRAM LINE

MEMORY ADDRESS	DATE	PROGRAM INSTRUCTION		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	START	HLT	
0086	20BF		INH	
0088	0200		LDK	A2, 0
008A	4BD0		SST	A3,/10
008C	42D0		CIO	A2,1,/10
008E	5C04		RB(NA)	* -2
0090	8520	OUTCR	LDKL	A5,/0A0D
0092	0A0D			
0094	4510	OUT	OTR	A5,0,/10
0096	5C04		RB(NA)	* -2
0098	3D68		SRL	A5,8
009A	5C08		RB(NZ)	OUT
009C	4610	OUTCH	OTR	A6,0,/10
009E	5C04		RB(NA)	* -2
00A0	1201		ADK	A2,1
00A2	EA1C		CWR	A2,A7
00A4	5C0A		RB(NE)	OUTCH
00A6	0200		LDK	A2,0
00A8	5F1A		RB	OUTCR

* Load the ASCII character in register A6
* Load the number of times you wish the character to be repeated into register 7
* Load the start address of the program into register A0 (/0086).
* Push the RUN button

MEMORY ADDRESS	DATA	PROGRAM INSTRUCTIONS		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	START	HLT	
0086	20BF		INH	
0088	0221	IN	LDK	A2,/21
008A	42D0		CIO	A2,1,/10
008C	5C04		RB(NA)	* -2
008E	4B10		INR	A3,0,/10
0090	5C04		RB(NA)	* -2
0092	4290		CIO	A2,0,/10
0094	4CD0		SST	A4,/10
0096	5C04		RB(NA)	* -2
0098	0200		LDK	A2,0
009A	42D0		CIO	A2,1,/10
009C	5C04		RB(NA)	* -2
009E	4310		OTR	A3,0,/10
00A0	5C04		RB(NA)	* -2
00A2	4290		CIO	A2,0,/10
00A4	4CD0		SST	A4,/10
00A6	5C04		RB)NA)	* -2
00A8	5F24		RB	IN

Program Echo:

Once loaded and started any input character from the keyboard will be printed, displayed or executed on the device.

14 TRANSLATOR UPL BUS TO GP BUS P843-117 (TUGP)

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14.1 TUGP IDENTIFICATION

Type number : P843-117
Testprogram : depending on connected Control Unit
Channel : depending on connected COntrol Unit
Power consumption : 5VL, 1.5A

12NC number on the sticker on the board
TUGP: 5111 199 6769x (5322 216 25527)

14.2 INSTALLATION DETAILS

14.2.1 CONFIGURATION DESCRIPTION

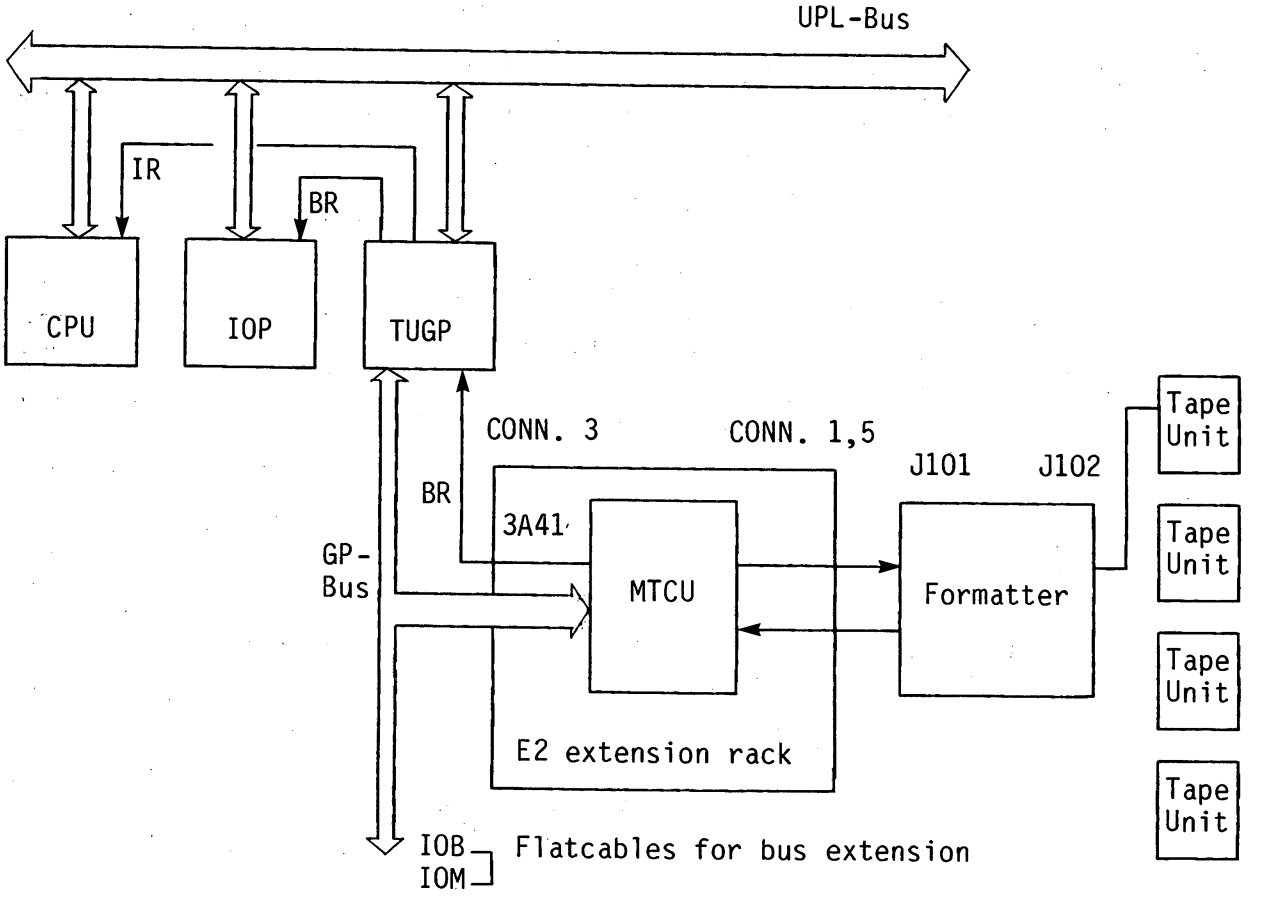


Figure 14.1 MAG. TAPE CU/SYSTEM DIAGRAM

Configuration Description

The minimum configuration is:

- A basic cabinet plus Power supply with:
  . UPL CPU
  . Memory
  . IOP
  . TUGP
- An E2 extension cabinet with a Magnetic Tape Control unit.
- Magnetic Tape Peripheral(s) and Formatter.
- GP Bus cables (IOB and IOM), Break cable for E2 rack, GP Bus terminator.

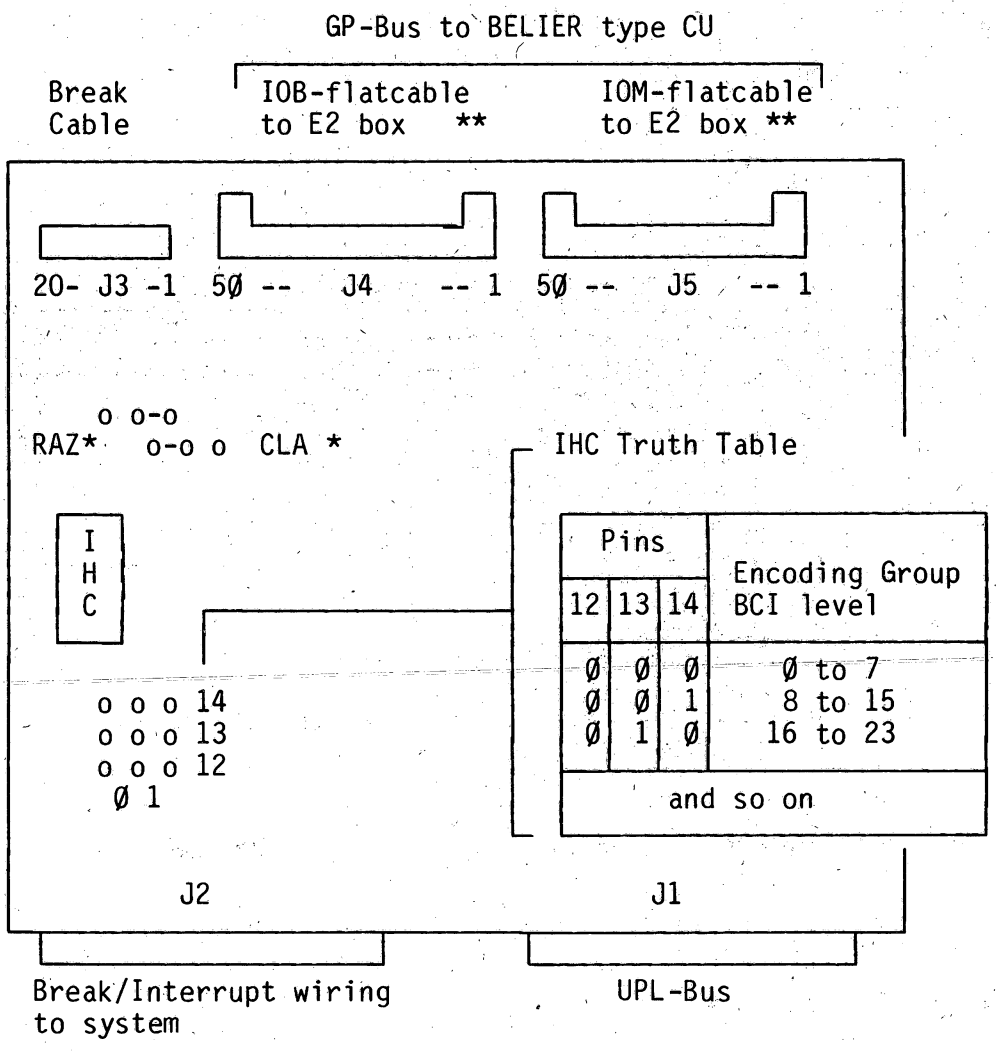
14.2.2 TUGP INTERRUPTS

The interrupt level of MTCU is recencoded:

. either by Interrupt Handler Chip (IHC) on BCI line between 0 and 63 (U-link setting).
. or by a single interrupt wire to the star interrupt system (level 4-31) from an intermediate level between 0 and 7 at the output of TUGP.

Note: as the required interrupt level cannot be selected on the TUGP board, an intermediate level must be used to transport between MTCU and TUGP. (eg. level 7).
Remove IHC chip if not used.

14.2.3 TUGP U-LINK SETTING



* = mandatory position
** = red edge of cable

Figure 14.2 TUGP U-LINK SETTING

14.2.4 TUGP CONNECTIONS

The TUGP card can be mounted on any UPL-compatible backpanel, subject to the following constraint in respect of the length of the RSLN line (if the RSLN is used).

Power Supply RSLN emitter-follower output to Control Unit RSLN input:
- total length shorter than 5m.

When RSLN is not used by the GP Bus, the maximum permitted length of the GP Bus is 15 m.

INTERCONNECTIONS

Connector J1	UPL Bus
Connector J2	Break Lines and single-interrupt lines (if any) to UPL system
Connector J3	Standard P800 Break cable from extension rack
Connector J4	IOB Flat Cable Connections for GP Bus
Connector J5	IOM Flat Cable Connections for GP Bus

14.3 INTERFACE CONNECTIONS

Break Line

Pin No.	Signal	Function
J1B22	BRON	Break Request Not Lines (Not used - see connector J2)
B23	BR1N	
B24	BR2N	
B25	BR3N	
B27	BR4N	
B28	BR5N	
B29	BR6N	
B30	BR7N	

Table 14.1 TUGP CONNECTOR J1 (UPL-INTERFACE)

BREAK/INTERRUPT LINES

Pin No.	Signal	Function
J2C01	IRON	Interrupt Request Not (Single Interrupt Lines)
C02	IR2N	
C03	IR4N	
C04	IR6N	
C29	BRON	Break Request Not (Break Request Lines)
C30	BR2N	
C31	BR4N	
C32	BR6N	
J2A01	IR1N	Interrupt Request Not (Single Interrupt Lines)
A02	IR3N	
A03	IR5N	
A04	IR7N	
A29	BR1N	Break Request Not (Break Request Lines)
A30	BR3N	
A31	BR5N	
A32	BR7N	

Table 14.2 TUGP CONNECTOR J2 (UPL INTERFACE)

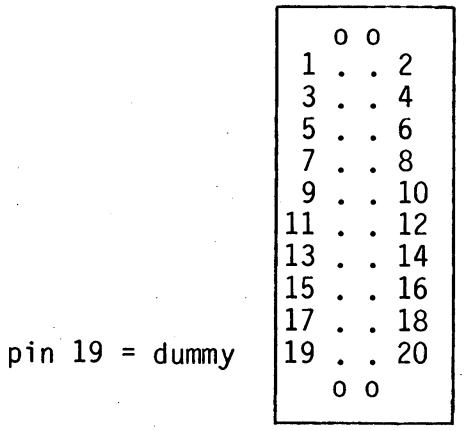
For MTCU, used device address /04, BR04N on pin 2C31 is connected to the IOP. For intermediate interrupt, level 7 on pin 2A04 may be chosen for interconnection to the CPU. U-links on the MTCU must have the same level.

TUGP CABLE CONNECTION TO EQUIPMENT BOX E2.

Pin No.	Signal	Function	Extension Box Pin	Extension Box Colour
J301	BRON	Break Request Not (Break Request Lines and Screens) and Screens	A	Blanc
02	BR1N		C	Green
03	OV		B	Brown
04	OV		D	Yellow
05	BR2N		E	Grey
06	BR3N		G	Blue
07	OV		F	Rose
08	OV		H	Red
09	BR4N		J	Black
10	BR5N		L	Grey Rose
11	OV		K	Violet
12	OV		M	Blue Red
12	BR6N		N	Blanc Green
14	BR7N		R	Blanc Yellow
15	OV		P	Green Brown
16	OV		S	Yellow Brown
17				
18				
19		dummy		
20				

Table 14.3 TUGP CONNECTOR J3 (GP INTERFACE)

J3 (contd)



Component side view Connector pinning

TUGP Cable Connection to Equipment Box E2, IOB

Pin No.	Signal	Function	Pin No.	Signal	Function
J401	0V		J426	BIO05N	Bus Input/Output Lines and Guards
02	RSLN	Reset Line Not	27	0V	
03	0V		28	BIO04N	
04	PWFN	Power Failure Not	29	0V	
05	0V		30	BIO03N	
06	BIO15N	Bus Input/Output Lines and Guards	31	0V	
07	0V		32	BIO02N	
08	BIO14N		33	0V	
09	0V		34	BIO01N	
10	BIO13N		35	0V	
11	0V		36	BIO00N	
12	BIO12N		37	0V	Interrupt Line and Guard
13	0V		38	BIEC5	
14	BIO11N		39	0V	Scan External Int. and Guard
15	0V		40	SCEIN	
16	BIO10N		41	0V	Interrupt Lines and Guards
17	0V		42	BIEC3	
18	BIO09N		43	0V	
19	0V		44	BIEC4	
20	BIO08N		45	0V	
21	0V		46	BIEC1	
22	BIO07N		47	0V	
23	0V		48	BIEC2	
24	BIO06N		49	0V	
25	0V		50	BIEC0	

Max. cable length 14.5m, 12NC 5111 199 7778x

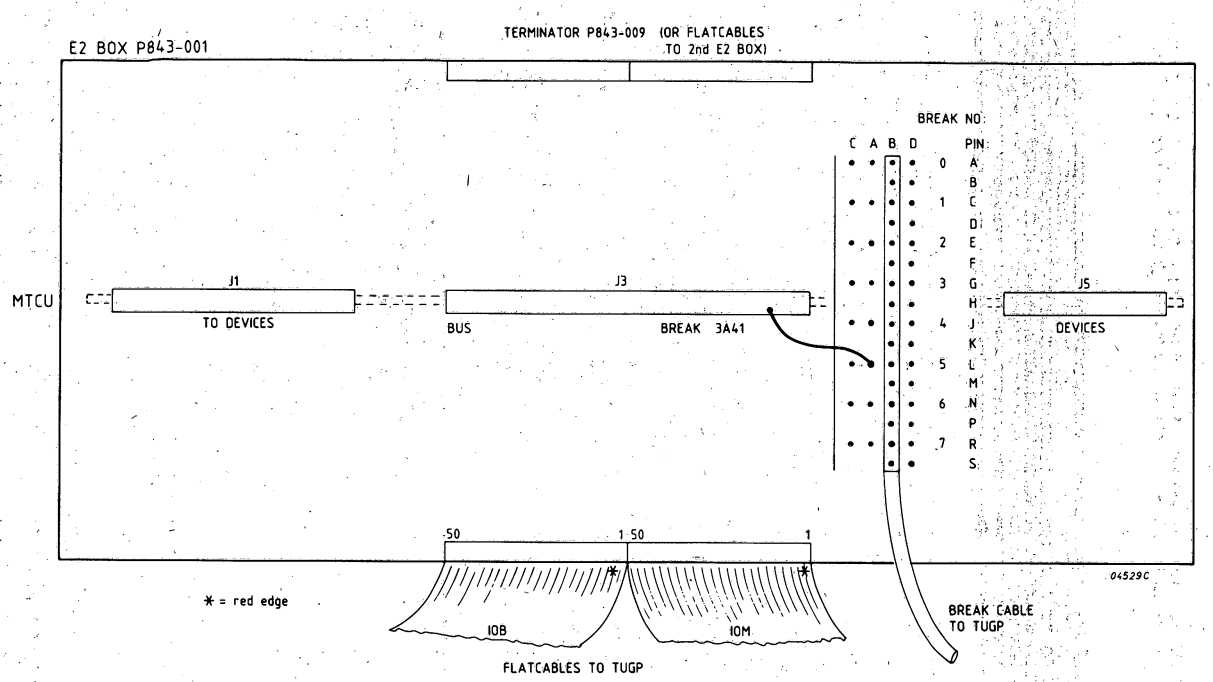
Table 14.4 TUGP CONNECTOR J4-IOB (GP INTERFACE)

TUGP CABLE CONNECTION TO EQUIPMENT BOX E2, IOM

Pin No.	Signal	Function	Pin No.	Signal	Function
J501	0V		J526	0V	
02	MAD04		27	CLEARN	
03	0V		28	0V	
04	MAD03		29	0V	
05	0V		30	TPMN	
06	MAD08		31	0V	
07	0V		32	0V	Control Signals and Guards
08	MAD09		33	TMPN	
09	0V		34	0V	
10	MAD10	Master Address and Guard Lines	35	0V	
11	0V		36	TMEN	
12	MAD11		37	0V	
13	0V		38	0V	
14	MAD12		39	TRMN	
15	0V		40	0V	
16	MAD13		41	0V	
17	0V		42		
18	MAD14		43	0V	
19	0V		44		
20	MAD15		45	0V	
21	0V		46		
22	ACN	Accept Line and Guard	47	0V	
23	0V		48		
24	0V		49	0V	
25	0V		50	+5VL	

Max. cable length 14.5m., 12NC 511 199 7778x

Table 14.5 TUGP CONNECTOR J5-IOM (GP INTERFACE)



Internal connection:

pins row 'C' = 'D'
'A' = 'B'

If a 2nd E2 box is connected, the BREAKcable can be extended by using row 'D'. For the used breaklevels on the 2nd box, interconnections must be made between row 'C' and 'A'.

Figure 14.3 EQUIPMENT BOX E2 CONNECTIONS

15 FLEXIBLE DISC CONTROL UNIT P830-145 (FLDZ)

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	15.3	INTERFACE CONNECTIONS	15-8
	15.4	HARDWARE-SOFTWARE INTERFACE DETAILS	15-9
	15.4.1	Status Word	15-10
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	15.7	PREVENTIVE MAINTENANCE	15-17
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15.1 FLEXIBLE DISC CONTROL UNIT - IDENTIFICATIONS

```
Type Number       : P-830-145 (FLDZ)
Testprogram       : BFLOP1
Channel           : PC or IOP
                    Break-connection: 1A05 Interrupt-connection: 1C05
Devices           : Flexible Disc Drive CDC 9404, with doorlock P830-006
                                        CDC 9404, no doorlock   P830-015
Power Consumption : +5  Volt, 4.7 Amp.
                    +25 Volt, 1.3 Amp. (Drive)
                    +5  Volt, 0.8 Amp. (Drive)
```

12 NC number on the sticker on the board:

```
FLDZ - (assy)     : 5111 199 6225x  (5322 216 25259)
FLD1              : 5111 199 6965x
FLD2 (with "LOCK"): 5111 199 6964x
```

X = modification level.

15.2 INSTALLATION DETAILS

Example:

CU Address = 3
Device Address = /03 DRIVE 0
/13 DRIVE 1
/23 DRIVE 2
/33 DRIVE 3

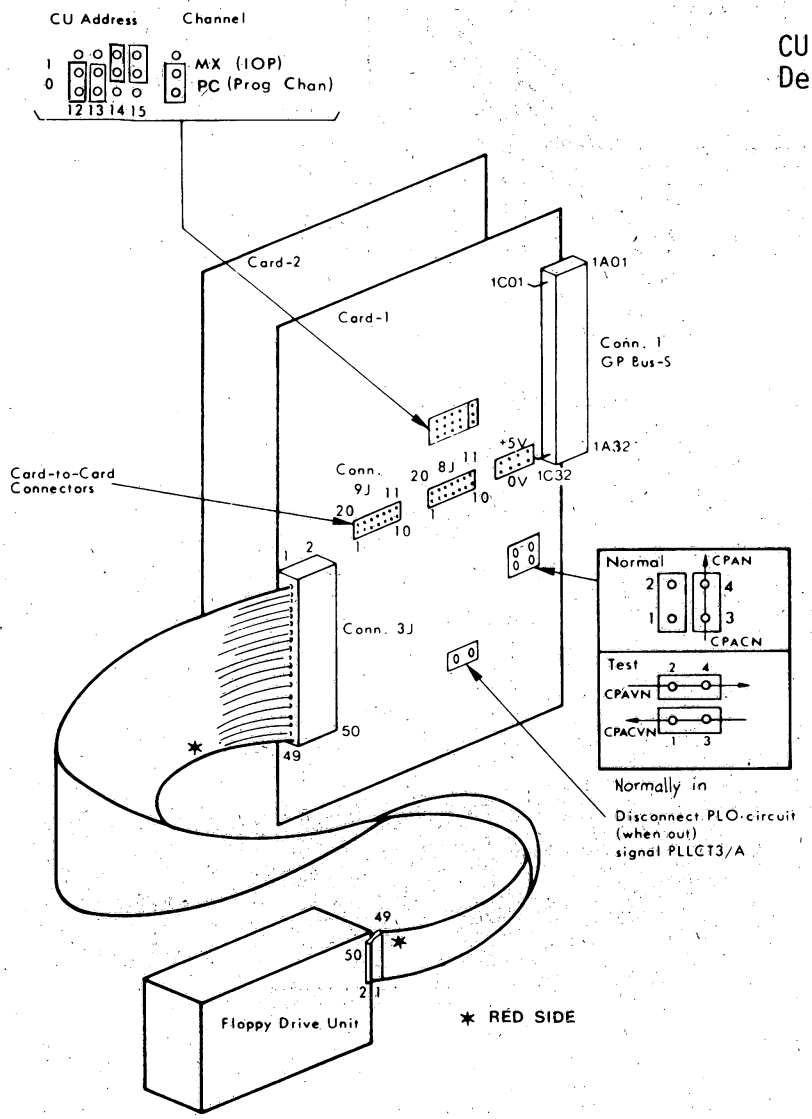
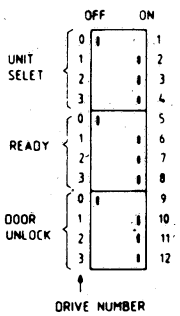


Figure 15.1 CONNECTORS, CABLES, U-LINKS

- Drive Select switch:
  (on drive)



Example drive 0

Note: Text 'OFF/ON' not according function.

Terminator: Only on last drive on the bus.

Figure 15.2 FLOPPY DRIVE SETTINGS

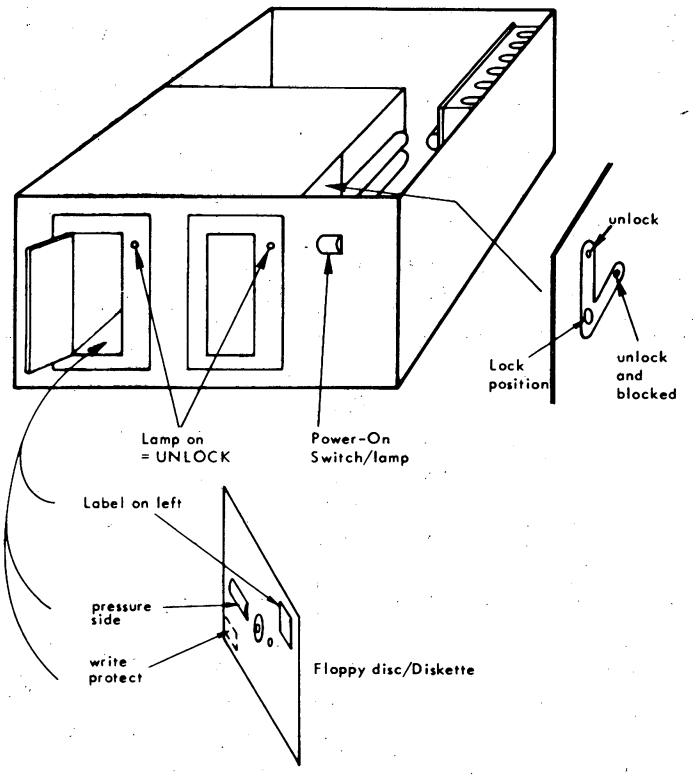


Figure 15.3 FLOPPY DRIVE CHASSIS, FRONT VIEW

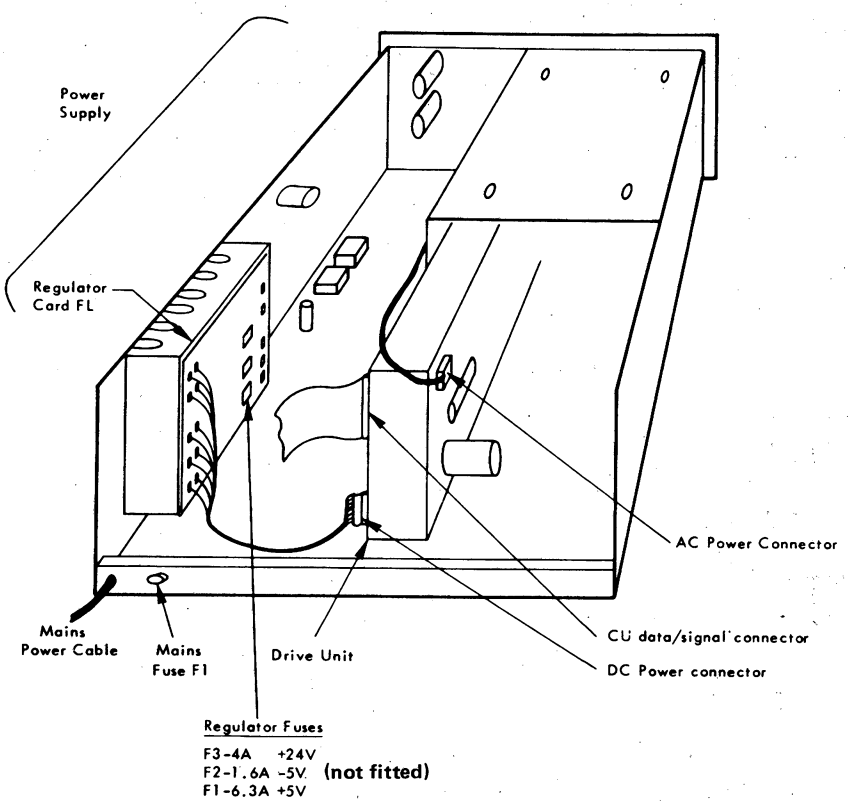


Figure 15.4 FLOPPY DRIVE CHASSIS, REAR VIEW

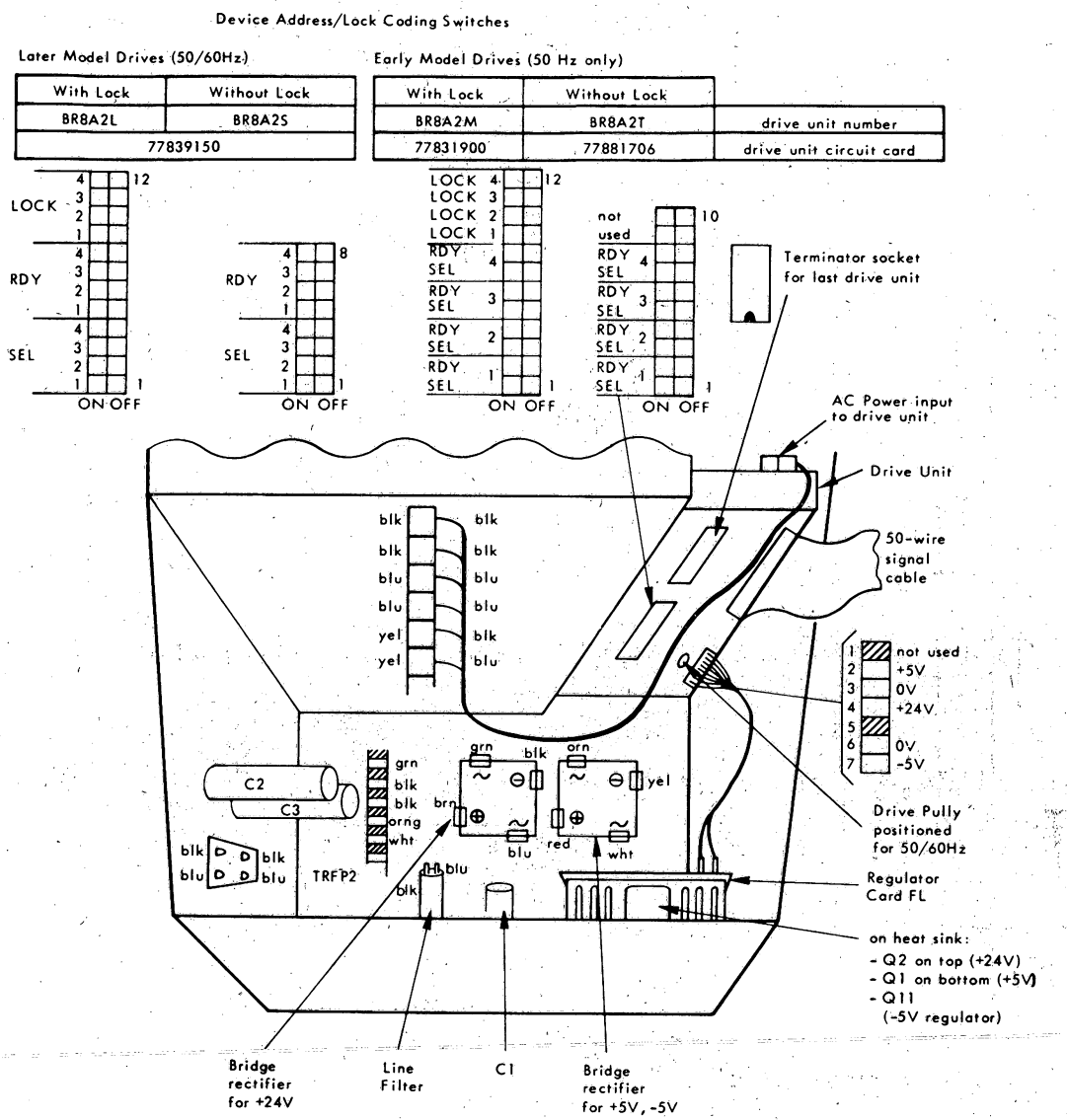


Figure 15.5 FLOPPY DRIVE CHASSIS, RIGHT SIDE INTERIOR

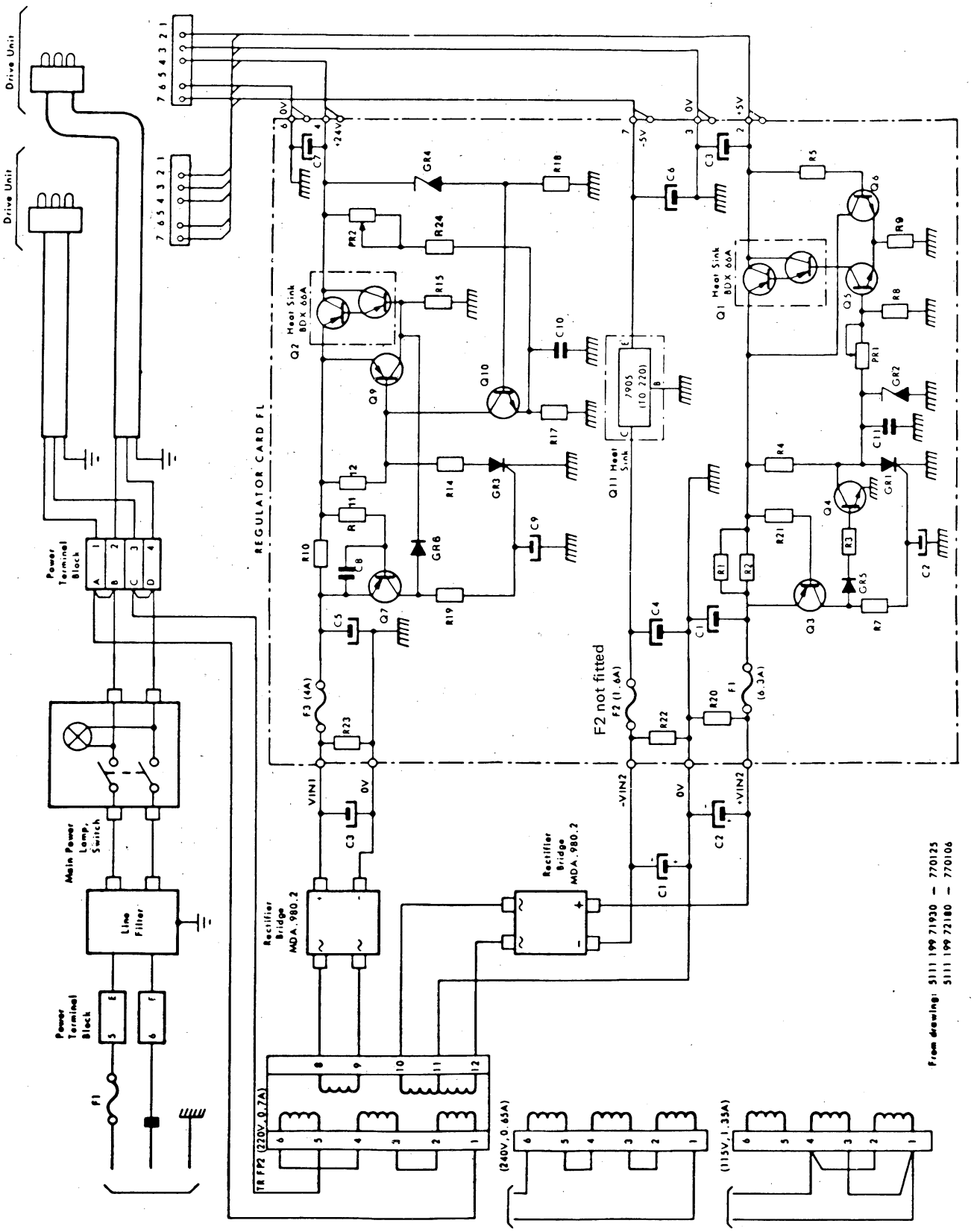


Figure 15.6 POWER SUPPLY SCHEMATIC

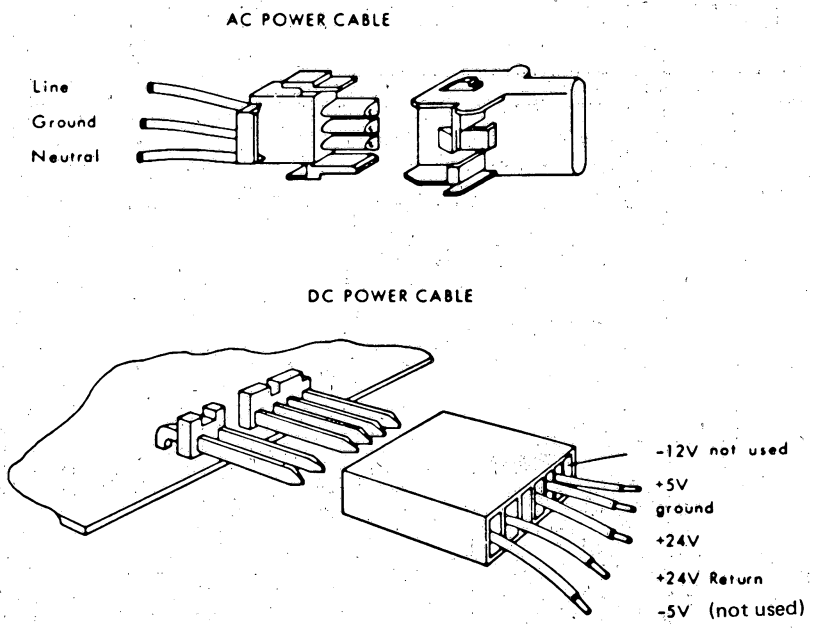


Figure 15.7 FLOPPY DISC DRIVE POWER CONNECTORS

Control Unit				Disc Drive		
Logic Sheet	I/O Conn	I/O Conn	Signal Name		Drive Conn 3M	Drive Conn AMP
				ground	1	A
	7A02	5A37	←RDLN	READ DATA/CLOCK COMPOSITE	2	B
				ground	3	C
	7A03	5A36	HEADLN	HEAD LOAD →	4	D
				ground	5	E
	7A04	5A35	←TR0N	TRACK 00	6	F
				ground	7	H
	7A05	5A34	←INDN	INDEX	8	J
				ground	9	K
	7A06	5A33	LWCN	LOW WRITE CURRENT →	10	L
				ground	11	M
	7A07	5A32	STEPN	STEP →	12	N
				ground	13	P
	7A08	5A31	DIRN	DIRECTION →	14	R
				ground	15	S
	7A09	5A30	WEN	WRITE ENABLE →	16	T
				ground	17	U
	7A10	5A29	WDLN	WRITE DATA →	18	V
				ground	19	W
e	7A11	5A28	SEL0N	UNIT SELECT 1 →	20	X
				ground	21	Y
	7A12	5A27	SEL1N	UNIT SELECT 2 →	22	Z
				ground	23	AA
	7A13	5A26	SEL2N	UNIT SELECT 3 →	24	BB
				ground	25	CC
	6A02	5A25	SEL3N	UNIT SELECT 4 →	26	DD
				ground	27	EE
	6A03	5A12	←RDY0N	UNIT READY INTERRUPT 1	28	FF
				ground	29	HH
	6A04	5A11	←RDY1N	UNIT READY INTERRUPT 2	30	JJ
				ground	31	KK
	6A05	5A10	←RDY2N	UNIT READY INTERRUPT 3	32	LL
				ground	33	MM
	6A06	5A09	←RDY3N	UNIT READY INTERRUPT 4	34	NN
				ground	35	PP
	6A07	5A08	←WRPN	WRITE PROTECT	36	RR
				(ground	37	SS
				READ DATA SEPARATED)	38	TT
				ground	39	UU
	6A09	5A06	UNLOCK0N	DOOR UNLOCK 1 →	40	VV
				ground	41	WW
	6A10	5A05	UNLOCK1N	DOOR UNLOCK 2 →	42	XX
				(ground	43	YY
d				WRITE FAULT)	44	ZZ
				(ground	45	AB
				WRITE FAULT RESET)	46	AC
				ground	47	AD
	6A12	5A02	UNLOCK2N	DOOR UNLOCK 3 →	48	AE
				ground	49	AF
	6A13	5A01	UNLOCK3N	DOOR UNLOCK 4 →	50	AH

for special options

Table 15.1 CU - DEVICE INTERFACE

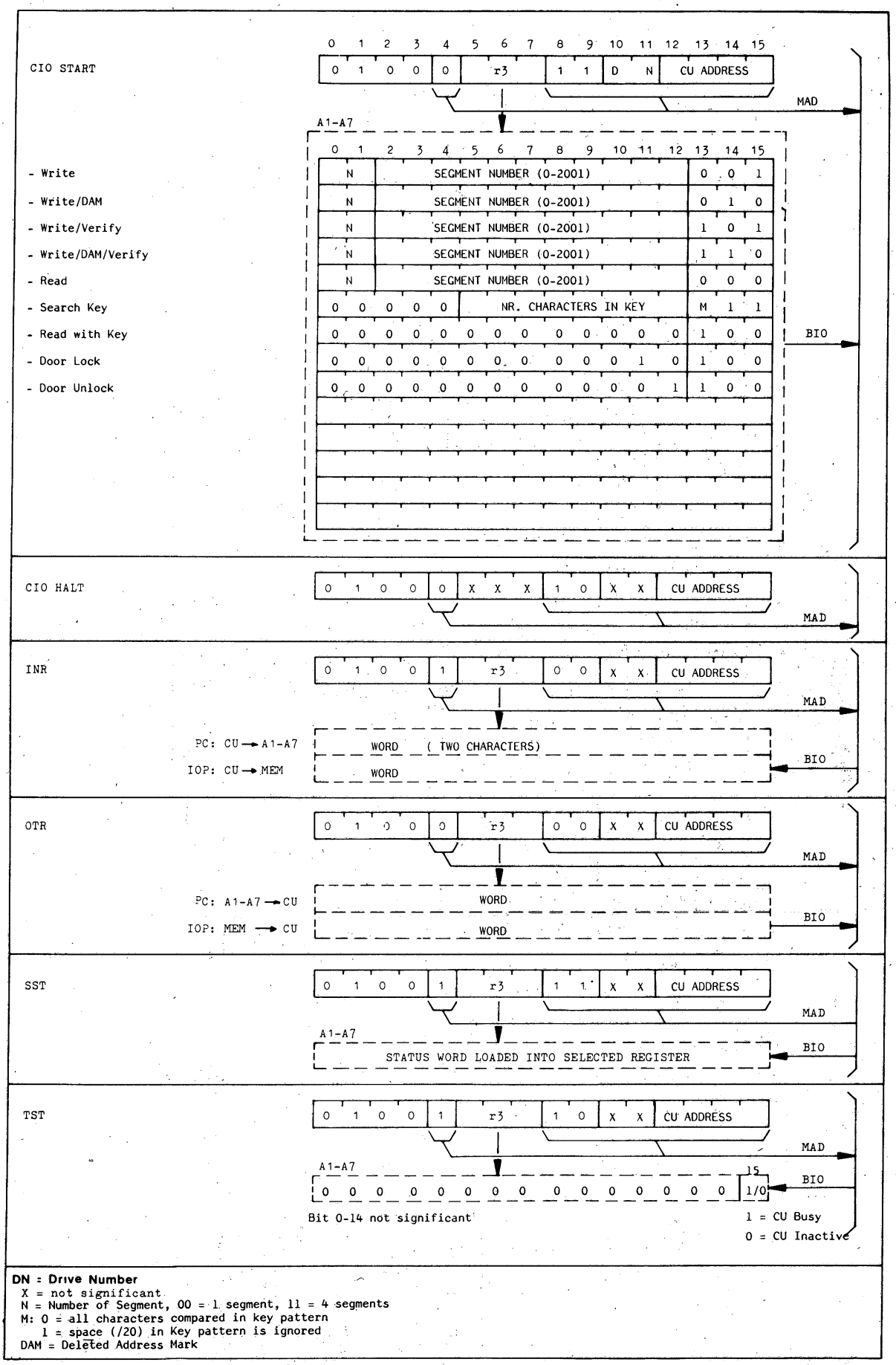


Figure 15.8 INSTRUCTION / COMMAND-WORD FORMATS

15.4.1 STATUS WORD

BIO	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Possible Configurations:
		Drive Ready after Not Ready	Key Not Found		Deleted Data Adr. Mark	Record Not Found	Write Protect		(msb) Drive (lsb)		Retry	Program Error	Incorrect Length	Data Fault		Drive Not Operable	
	0	0	0	0	0	0	0	0			Y	0	0	0	0	0	Write, Write/DAM performed correctly
	0	0	0	0	Y	0	0	0			Y	0	0	0	0	0	Read, Search Key performed correctly
	0	0	0	0	0	0	0	0			0	0	Y	0	0	0	Read Key Segment performed correctly
	0	0	0	0	0	0	0	0			0	0	0	0	0	0	Door command performed correctly
	0	0	0	0	0	x	x	0			Y	x	x	0	0	x	Write, Write/DAM incorrect
	0	0	0	0	0	x	x	0			Y	x	x	x	0	x	Write/Ver, Write/DAM/Verify incorrect
	0	0	0	0	Y	x	0	0			Y	x	x	x	0	x	Read incorrect
	0	0	x	0	Y	x	0	0			Y	x	x	x	0	x	Search Key incorrect
	0	0	0	0	0	0	0	0			0	x	x	0	0	x	Read Key Segment incorrect
	0	1	0	0	0	0	0	0			0	0	0	0	0	0	Device just became operable
	0	0	0	0	0	0	0	0			0	0	0	0	0	1	Door command not performed

Drive Number

Y = bit can be 1 or 0
x = at least one of these bits must be set to 1.

The status bits have the following meanings:

- 15 means command attempted on a Non-Operable Drive or the selected drive goes non-operable. (A non-selected drive going inoperable does not set CU status.) Note: a diskette inserted upside-down will cause the non-operable condition.
- 13 means Data Fault: In the Write/Verify or Write/DAM/Verify mode a CRC error has been detected during the verify reading. In the Read mode there is data-field CRC error non-recoverable with read retries (bit 10 also set). In the Search Key mode there is a non-recoverable data-field CRC error in any segment and the key is not found in any other segment (bits 2, 10 also set).
- 12 means Incorrect Length: Block length specified by channe does not correspond to number of segments to be transferred or required block length. Allowed lengths are:

  Any Write command $\leq (N+1) \times 64$ words
  Read $(N+1) \times 64$ words
  Search Key $\frac{n}{2} + 2$ words, or $\frac{n+1}{2} + 2$ words
  (n = even or odd number of characters)
  Read Key Segment 65 words

- 11 means Program Error:
  — Channel sends INR instead or OTR during any Write or Sea ch Key, or Key command.
  — Segment number command is greater than 2001 or converts to a track number greater than 76.
  — The first segment number is greater than the second segment number for Search Key.
  — Unknown command.

Track	Sector	Segment		Hexadecimal
00	1-26	0- 25	↑	/000-/019
01	1-26	26- 51		/01A-/033
02	1-26	52- 77	Software Limit	/034-/04D
---	---	---		---
73	1-26	1898-1923	↓	/76A-/783
74	1-26	1924-1949		/784-/79D
75	1-26	1950-1975		/79E-/7B7
76	1-26	1976-2001		/7B8-/7D1

- 10 means Retry: ID-field or data-field CRC error caused a read-retry procedure, whether or not the error was recovered.
- 9,8 mean Drive Number:

8	9	Drive
0	0	0
0	1	1
1	0	2
1	1	3

- 6 means Write Protect: Set if any Write command is attempted on a drive with a write-protected diskette loaded.
- 5 means Record Not Found:
  - Unrecoverable ID-Field CRC error during any Write command or Read command.
  - Unrecoverable ID- or data-field error and key is not found, during Search Key.
- 4 means Deleted Data Address Mark: Detected in a segment read during Read command or in the located key segment during a Search Key command.
- 2 means Key Not Found: The key segment not found within the search area of a Search Key command. There may also be a Record Not Found error.
- 1 means Drive Ready After Not Ready: Detected when the CU is in nactive state — the CU sends an interrupt request and goes to Wait Status state.

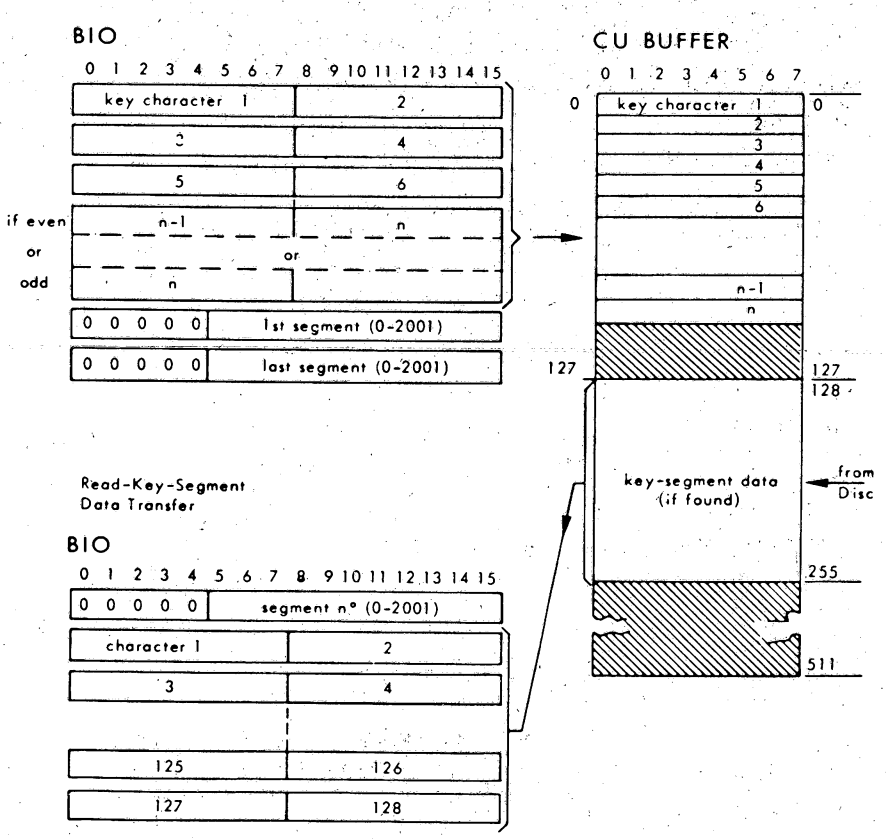


Figure 15.9 SEARCH-KEY, READ-KEY PATTERN / DATA LOADING

15.5 SHORT DESCRIPTION TESTPROGRAMS

Testprogram: BFLOP1

> WARNING: Do Not Switch On/Off Power When Floppy Disc In Drive

Device Address Typewriter: /10

1) IPL PTR /1020
TK /1785 PC
/0785 MX
/D0C3 PC (with correct bootstrap)
/40C3 MX
Program stops at address /700 (restart address, stop after interrupt)

2) A8: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

0	0	1	1	1	0	0	0	0	0	0	0	0	1	1

Int. Level PC/MX (1 0) CU Address

Standard Level:
P853/4:
Addr. /03
Int. Level /E
e.g. /3803

A9 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

Testprogram Control

Drive No.
1 = CU Lock
1 = Drive Lock
Mains Freq., 0=50 Hz., 1=60Hz.

A10 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0

Check Nrs. Standard Optional
/B = Check on IBM format

3) Switch on RTC
Reset bit 4 and 5 of A9 to "0".
4) Depress MC, RUN

Typewriter: If 0000 = Check number
Stop at /5E0
5) Open door of all drives
6) Switch RUN If 0001
00D0 = Drive number
Stop at /5E0
7) Close door of tested drive
8) Switch RUN, etc. program stops after last test at address /700

ERROR : ER xxxx

Stop at address /5E0

Erorr type (see description testprogram)
Phase number
Check number
A2 Reg.: received status
A3 Reg.: expected status
A4 (if MX) Nr. of words not yet exchanged

BFLOP1 tested:

Check	Desctiption
CHK ØØ	Test of the controller
CHK Ø1	Test of the controller
CHK Ø2	Test of the write command
CHK Ø3	Test of the read command
CHK Ø4	Test of the status on a CIO search key
CHK Ø5	Write and read test
CHK Ø6	Write diskette from sector Ø to sector X (value of X = see CHK ØF)
CHK Ø7	Read diskette from sector Ø to sector X (value of X = see CHK ØF)
CHK Ø8	Read random sector
CHK Ø9	Write deleted test
CHK ØA	Search key and read key test
CHK ØB	Read whole diskette so as to check whether it is correct
CHK ØC	Service check for read and write
CHK ØD	Service check for search key and read key
CHK ØF	It permits parameter change in check Ø6

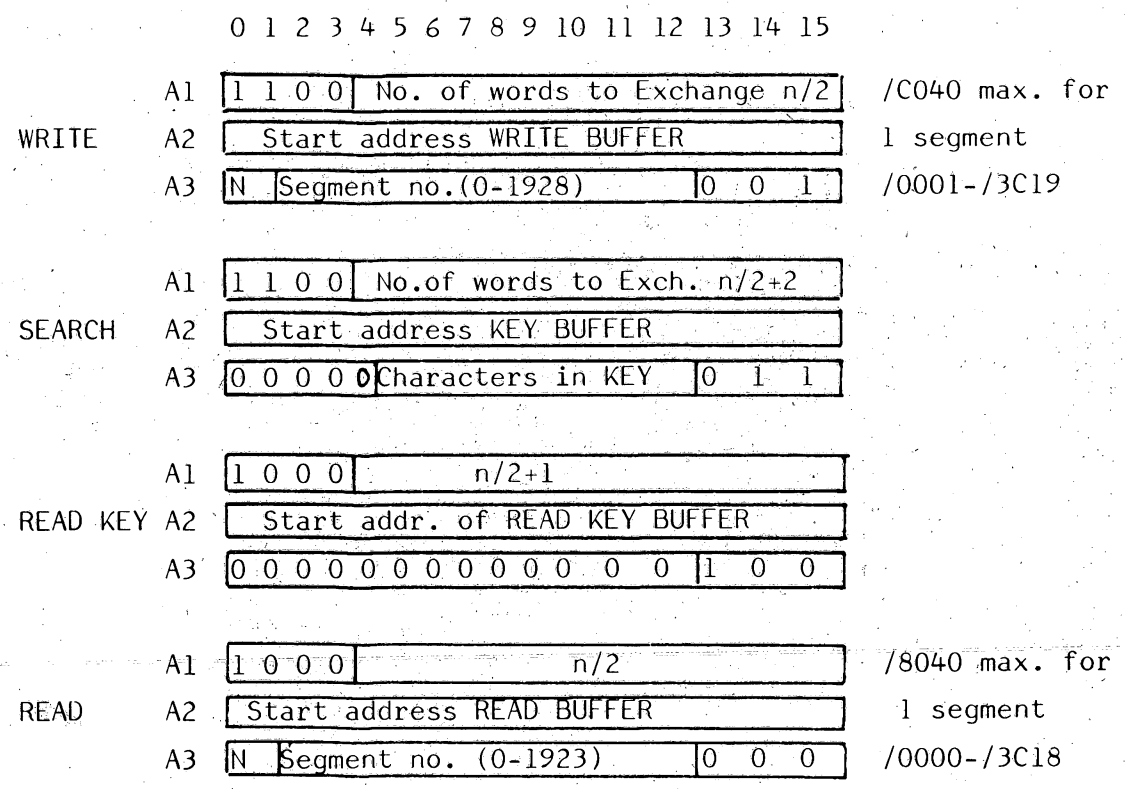
Note: Doorlock tests CHK 10 and 11 are not selected.

Procedure 5111 991 1Ø111 = Procedure BFLOP1 5111 991 Ø8696
with addendum PTS8ØØØ 5111 991 11381
Listing 5111 991 1Ø121
Program 5111 199 65651

15.6 SHORT ROUTINES

```
        DATE  80-03-13        IDENT    FDDWRT    ON PROGRAMMED CHANNEL


00000                         IDENT    FDDWRT                ON PROGRAMMED CHANNEL
00001                  *PROGRAM FOR WRITE OR WRITE KEY COMMANDS
00002                  *        REG. A3  COMMAND
00003                  *        REG. A1  NUMBER OF WORDS TO EXCHANGE
00004                  *        REG. A2  BUFFER ADDRESS IN MEMORY
00005
00006                  *AFTER EXECUTION THE PROGRAM STOPS AT ADDR. /86
00007                  *        REG. A7  STATUS WORD
00008
00009                           AORG     /80
00010  0080  FFFF               DATA     /FFFF
00011  0082  0000               DATA     0
00012  0084  207F       START   HLT                            STATUS IN A7
00013  0086  20BF               INH
00014  0088  8508               LDR      A5,A2                 SAVE A2
00015  008A  8604               LDR      A6,A1                 SAVE A1
00016  008C  43C3               CIO      A3,1,3                START CONTROLLER
00017  008E  5C04               RB(4)    *-2
00018  0090  8434       OUT     LDR*     A4,A5                 LOAD WORD
00019  0092  4403       OTR     OTR      A4,0,3                OUTPUT WORD
00020  0094  5408               RF(4)    SST
00021  0096  1502               ADK      A5,2                  UPDATE BUFFER ADDRESS
00022  0098  1E01               SUK      A6,1                  DECREMENT NO OF EXCHANGES
00023  009A  5C0C               RB(4)    OUT
00024  009C  4483               CIO      A4,0,3                STOP CONTROLLER
00025  009E  4FC3       SST     SST      A7,3                  GET STATUS
00026  00A0  5C10               RB(4)    OTR
00027  00A2  5F20               RB       START
00028                           END      START


        DATE  80-03-13        IDENT    FDDRD     ON PROGRAMMED CHANNEL


00000                         IDENT    FDDRD                 ON PROGRAMMED CHANNEL
00001                  *PROGRAM FOR READ OR READ KEY COMMANDS
00002                  *        REG. A3  COMMAND
00003                  *        REG. A1  NUMBER OF WORDS TO EXCHANGE
00004                  *        REG. A2  BUFFER ADDRESS IN MEMORY
00005
00006                  *AFTER EXECUTION THE PROGRAM STOPS AT ADDR. /86
00007                  *        REG. A7  STATUS WORD
00008
00009                           AORG     /80
00010  0080  FFFF               DATA     /FFFF
00011  0082  0000               DATA     0
00012  0084  207F       START   HLT                            STATUS IN A7
00013  0086  20BF               INH
00014  0088  8508               LDR      A5,A2                 SAVE A2
00015  008A  8604               LDR      A6,A1                 SAVE A1
00016  008C  43C3               CIO      A3,1,3                START CONTROLLER
00017  008E  5C04               RB(4)    *-2
00018  0090  4C03       INR     INR      A4,0,3                READ WORD
00019  0092  540A               RF(4)    SST
00020  0094  8435               STR      A4,A5                 WORD TO BUFFER
00021  0096  1502               ADK      A5,2                  UPDATE BUFFER ADDRESS
00022  0098  1E01               SUK      A6,1                  DECREMENT NO OF EXCHANGES
00023  009A  5C0C               RB(4)    INR
00024  009C  4483               CIO      A4,0,3                STOP CONTROLLER
00025  009E  4FC3       SST     SST      A7,3                  GET STATUS
00026  00A0  5C12               RB(4)    INR
00027  00A2  5F20               RB       START
00028                           END      START
```

```
DATE  80-03-13        IDENT    FDDRWD    ON IOP CHANNEL

00000                         IDENT    FDDRWD                ON IOP CHANNEL
00001                 *PROGRAM FOR WRITE AND READ COMMANDS
00002                 *        REG. A1  FIRST CONTROL WORD
00003                 *        REG. A2  SECOND CONTROL WORD (BUFFER ADDRESS)
00004                 *        REG. A3  COMMAND
00005
00006                 *AFTER EXECUTION PROGRAM STOPS AT ADDRESS /86
00007                 *        REG. A7  STATUS WORD
00008
00009                          AORG     /80
00010  0080  FFFF              DATA     /FFFF
00011  0082  0000              DATA     0
00012  0084  207F      START   HLT                            STATUS IN A7
00013  0086  20BF              INH
00014                 *        PREPARE IOP
00015  0088  7106              WER      A1,6                  FIRST CONTROL WORD
00016  008A  7207              WER      A2,7                  SECOND CONTROL WORD
00017  008C  43C3              CIO      A3,1,3                START CONTROLLER
00018  008E  5C04              RB(4)    *-2
00019  0090  4FC3              SST      A7,3                  GET STATUS
00020  0092  5C04              RB(4)    *-2
00021  0094  5F12              RB       START
00022                          END      START
```



Number of Segments:		Number of Characters:	
N = 00	= 1	n	128
01	= 2		256
10	= 3		384
11	= 4		512

```
          DATE  80-03-13        IDENT    FLTST     ON P800

00000                           IDENT    FLTST                  ON P800
00001                  *         READ-WRITE TEST OF DISCETTE
00002                  *        PROGRAM PRESET:
00003                  *                 FOR DRIVE 0 , DA /03
00004                  *                 START SEGMENT NUMBER 0
00005                  *                 WRITTEN DATA /30 (ASCII FOR '0')
00006
00007                  *        PROGRAM STOP ON /8C:
00008                  *                 WRITTEN DATA CAN BE CHANGED IN A2
00009                  *                 START SEGMENT NUMBER CAN BE CHANGED IN A5
00010                  *                 AFTER EXECUTION DISCETTE IS CORRECT
00011
00012                  *        ERROR STOP ON /E2:
00013                  *                 STATUS IN A6
00014                  *                 SEGMENT NUMBER IN A5
00015
00016
00017                  *                 A5 BIT CONFIGURATION
00018                                                  0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
00019                                                  * **     SEGMENT NUMBER     2*  *  *
00020                           AORG     /80
00021  0080  FFFF               DATA     /FFFF
00022  0082  0000               DATA     0
00023  0084  8220       START   LDKL     A2,/3030               PRESET CHARACTER 0
       0086  3030
00024  0088  0500               LDK      A5,0                   PRESET SEGMENT 0
00025  008A  207F       BEGIN   HLT
00026  008C  20BF               INH
00027  008E  0100               LDK      A1,0                   RESET INDEX FOR BUFFER
00028  0090  8245               ST       A2,BUF,A1              FILL THE WRITE BUFFER
       0092  00EC
00029  0094  1102               ADK      A1,2
00030  0096  E920               CWK      A1,/200
       0098  0200
00031  009A  5D0C               RB(5)    *-/A
00032  009C  0100               LDK      A1,0                   RESET EXECUTE POINTER
00033  009E  8720               LDKL     A7,/FC1D               END SEGMENT
       00A0  FC1D
00034  00A2  9520               ADKL     A5,/C005               SELECT WRITE VERIFY WITH 4 SEGMENT
       00A4  C005
00035                  *        PREPARE THE IOP
00036  00A6  8320       RET     LDKL     A3,/C100
       00A8  C100
00037  00AA  8420               LDKL     A4,/C040               FOR 1 SEGMENT MODE
       00AC  C040
00038  00AE  F045               EX       WER,A1                 EXECUTE WER A3 OR WER A4.
       00B0  00E4
00039  00B2  8420               LDKL     A4,BUF
       00B4  00EC
00040  00B6  7407               WER      A4,7
00041  00B8  45C3               CIO      A5,1,3                 START CONTROLLER
00042  00BA  5C04               RB(4)    *-2
00043  00BC  4EC3               SST      A6,3                   GET STATUS
00044  00BE  5C04               RB(4)    *-2
00045                  *        CHECK STATUS
00046  00C0  A620               ANKL     A6,/641D
       00C2  641D
00047  00C4  5010               RF(0)    CONT                   STATUS OKE
00048  00C6  8104               LDR      A1,A1                  CHECK  4 SEGMENT OR 1 SEGMENT
00049  00C8  5116               RF(1)    STOP
00050                  *        STATUS IS WRONG CHANGE TO WRITE VERIFY SEGMENT BY SEGMENT
00051  00CA  9D20               SUKL     A5,/C000
       00CC  C000
00052  00CE  1102               ADK      A1,2                   UPDATE EXECUTE POINTER FOR 1 SEGMENT MOD
00053  00D0  B720               XRKL     A7,/C000               CHANGE TO TO 1 SEGMENT MODE
       00D2  C000
00054  00D4  5F30               RB       RET                    DO THE LAST ONES AGAIN IN 1 SEGMENTMODE
00055  00D6  F045       CONT    EX       UPDSEG,A1              NEXT SEGMENTS TO DO
       00D8  00E8
00056  00DA  ED1C               CWR      A5,A7                  IS IT THE LAST ONE
00057  00DC  5D38               RB(5)    RET                    NO
00058  00DE  5F58               RB       BEGIN-2                YES
00059  00E0  207F       STOP    HLT                             STATUS ERROR
00060  00E2  5F5C               RB       BEGIN-2                RESTART
00061  00E4  7306       WER     WER      A3,6
00062  00E6  7406               WER      A4,6
00063  00E8  1520       UPDSEG  ADK      A5,/20
00064  00EA  1508               ADK      A5,8
00065  00EC             BUF     RES      /100
00066                           END      START
```

15.7 PREVENTIVE MAINTENANCE

CLEANING THE READ/WRITE HEAD

Every 600 hours the read/write head requires cleaning which is carried out as follows:

- Use a lint free cloth to lightly dry buff head surface. Cleaning is completed if deposits are removed.
- If oxide deposits were not removed in the step above, dampen (do not soak) cloth with head cleaning solution (isopropanol), and wipe head surface. Finish by slightly dry buffing again to ensure that the head is dry and no alcohol residue is left.

CAUTION

Do not smoke while cleaning. Do not touch a head surface with fingers. Do not leave residue or line on the head. surfaces. Residual particles can result in a stored disc and/or loss of a head.

REPLACING THE HEAD LOAD PAD (SEE FIGURE 15.10)

Every 1200 hours, in addition to the cleaning above, the head load pad should be inspected. If the pad is worn, dirty, torn or loose it should be replaced, as described below:

. Remove power from the unit.
. Move the carriage assembly to its rear most position (toward the stepper motor) by turning the back part of the stepper motor shaft (figure 4-32). This will provide clearance for lifting the head load arm.
. Lift the head load arm until the head load pad is visible (see figure 4-32).
. If head load arm is a 77603108 (figure 15.10) proceed four steps ahead, if not go to next step.
. Remove the used pad with a sharp tool, if necessary, and discard. Be sure to remove all of the old pad and adhesive. Alcohol may be used to remove the old adhesive.
. Remove the protective packing from the new head load pad and position pad in approximate center of recess in head load arm. Press pad firmly to insure adhesion with a clean tongue depressor or with a thumb using a lintfree cloth to protect pad from grease or dirt.
. Go to the last step.
. Loosen clamping screw holding rim of head load pad.
. Insert screw driver and rotate head load pad so flat side with clear clamping screw.
. Remove Pad Holder Assembly.
. Insert new Assembly, with flat side toward clamping screw.
. Assuring that head load pad is fully seated, rotate pad 180°.
. Tighten clamping screw to hold pad in place.
. Lower arm gently on to head.

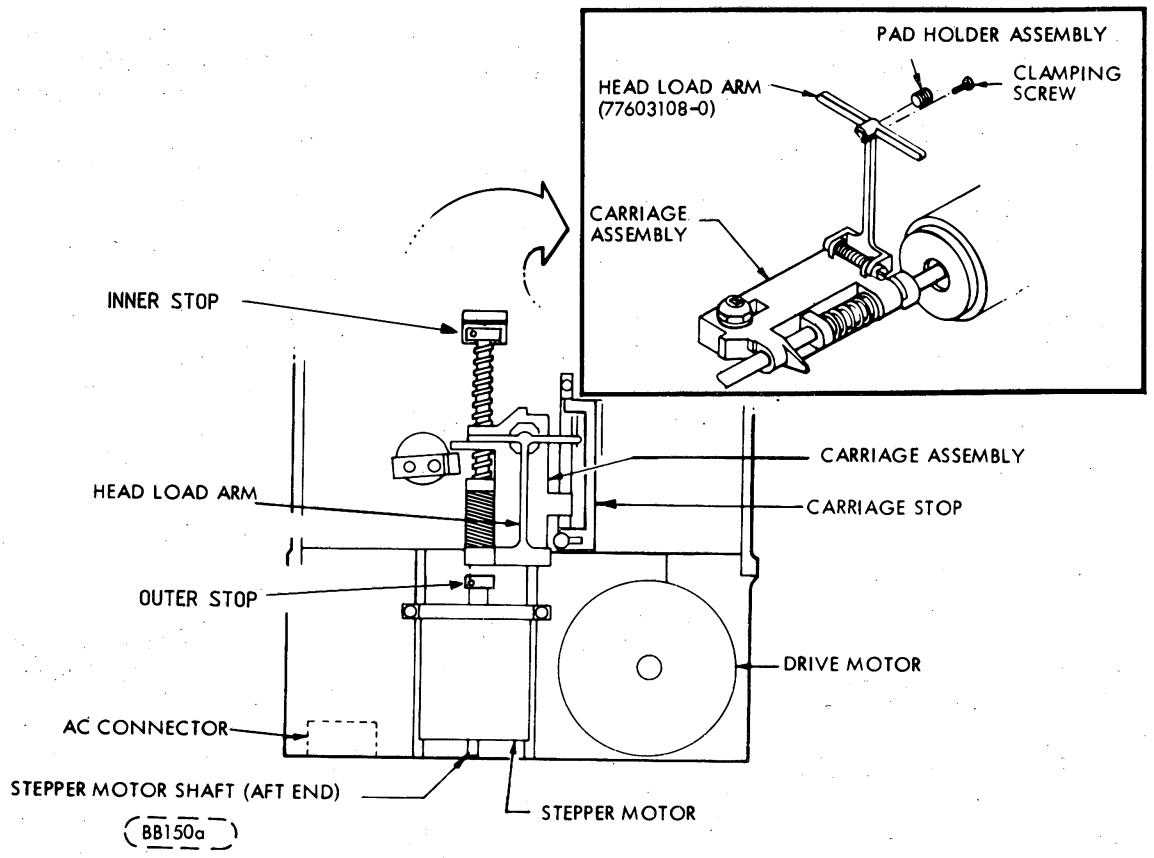


Figure 15.10 HEAD LOAD PAD REPLACEMENT

15.8 OPERATING FREQUENCY CONVERSION PROCEDURE

This procedure should be used to convert the FDD unit from 50Hz. operation to 60Hz. operation or vice vers. This is accomplished by reversing the dual diameter reversible pulley on the spindle motor shaft using the following steps:

. Remove AC power.
. Disconnect I/O cable from J1 on the printed circuit board.
. Disconnect I/O harnesses from J2, J3, J4, J5 and J6 on the board.
. Remove two screws from board adjacent to connector J1 (see figure A).
. Remove board by detaching it from the four push-in clips shown in figure A.
. Remove the belt from the spindle motor pulley (accessible from the under side of unit.
. Loosen set-screw and remove pulley.
. Reverse pulley and replace on motor shaft.
. Position pulley allowing tolerance of 0.079" (2.01 mm) ± 0.010" (0.254 mm) between shoulder of motor mounting screws and pulley. (Figure B).
. Tighten down set-screw.
. Replace belt and printed circuit board.

Note: It is important that the new operating frequency is marked on the units rating nameplate.

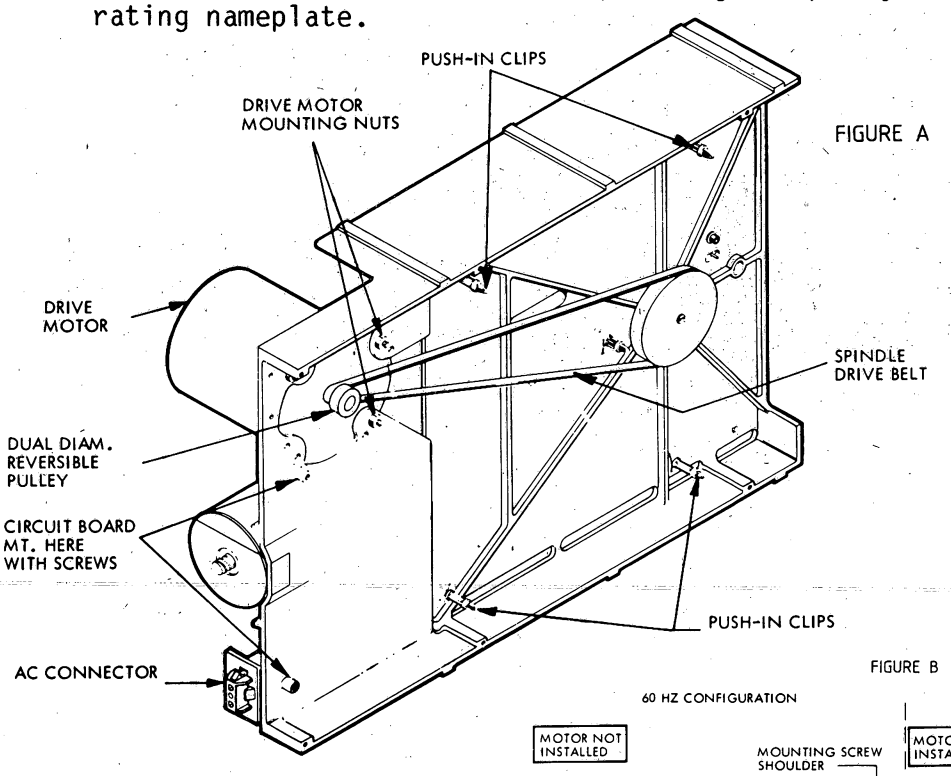


FIGURE A

FIGURE B

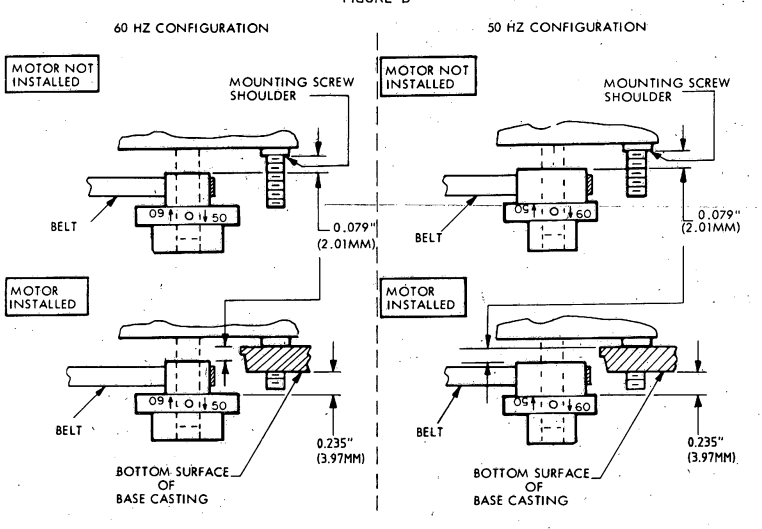


Figure 15.11 FDD FREQUENCY CONVERSION INSTRUCTIONS

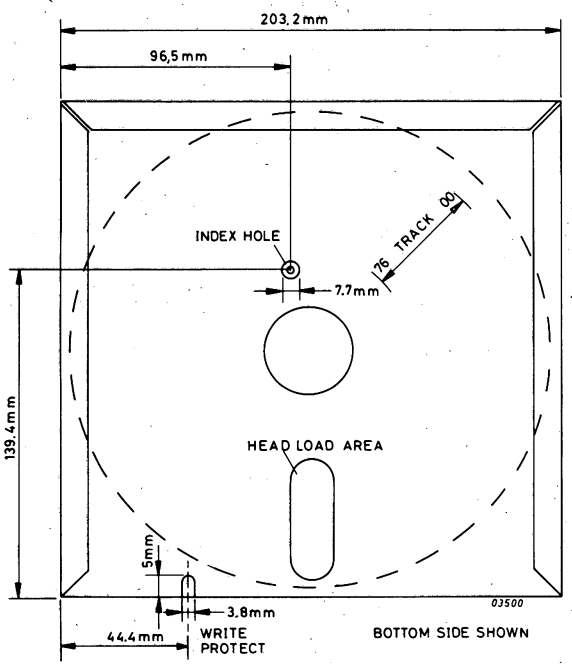


Figure 15.12 DISKETTE DIMENSIONS

16 FLEXIBLE DISC CONTROL UNIT P830-050 (F1MZ)

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	16.3	DRIVE CHARACTERISTICS	16-4
	16.4	INSTALLATION DETAILS	16-5
	16.5	INTERFACE CONNECTIONS	16-9
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16.1 FLEXIBLE DISC CONTROL UNIT (F1MZ) - IDENTIFICATIONS

Type Number : P830-150 (F1MZ)
Testprogram : BF1MZ
Channel : IOP/MIOP only. Break connection: 1A05, Interrupt: 1C05
Devices : Flexible Disc Drive CDC 9404 with or without doorlock option.
CDC 9406 with doorlock option (max. 2).
CDC 9406 without doorlock options (max. 4).
Power Consumption: +5 Volt, 2 Amp.

12NC code on the sticker on the board:
F1MZ: 5111 199 6752x (5322 216 25612)

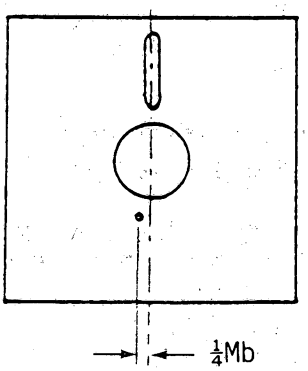
X = modification level.

16.2 FORMATS AND DISKETTES:

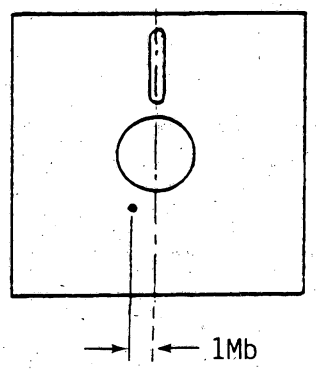
Format 0	Format 1	Format 2
1 sided discette single density 1 head	2 sided discette double density 2 heads	2 sided discette double density 2 heads
77 tracks total (0 - 76) track 0 - Index 1 - 73 or 74 - Data tracks 75,76 - Spare	77 cylinders total (0 - 76) cylinder 0 - Index 1 - 74 - Data cyl 75,76 - Spare	77 cylinders total (0 - 76) cylinder 0 - Index 1 - 74 - Data cyl 75,76 - Spare
26 sectors/track 128 bytes/sector	26 sectors/track * 256 bytes/sector	8 sectors/track * 1024 bytes/sector
total 'data' capacity 246,272 bytes	total 'data' capacity 985,088 bytes	total 'data' capacity 1,212,416 bytes
drive types CDC 9404 or CDC 9406	drive type CDC 9406	drive type CDC 9406
discette type - 20 cm, IBM 1 - sided P/N 2305830 (or equiv.)	discette type - 20 cm, IBM 2 - sided P/N 1766872 (or equiv.)	discette type - 20 cm, IBM 2 - sided P/N 1669045 (or equiv.)
IBM systems using this format - IBM 3740, IBM 5320, IBM 1, all systems using IBM "Standard Data Interchange"	IBM systems using this format - IBM 34-2	IBM systems using this format - IBM 34-2

* Note: Format 1 - Cyl. 0, head 0 is formatted as for format 0
(i.e. 26 sectors/track, 128 bytes/sector)
Format 2 - Cyl. 0, head 0 as for format 0
Cyl. 0, head 1 as for format 1

Table 16.1 FORMATS AND DISKETTES



format 0



format 1 or 2

16.3 DRIVE CHARACTERISTICS

	CDC9404 Single Density 1 side	CDC9406 Double Density 2 sides
Capacity (unformatted) (formatted and excluding spare tracks and track 00) - format 0 - format 1 - format 2	401,016 bytes 246,272 bytes	1,604,064 bytes 246,272 bytes 985,088 1,212,416
Number of discs Number of heads Tracks/surface (including spares)	1 1 77	1 2 77
Transfer rate Recording method	250K bits/sec (4µS/bit) FM (double frequency)	500K bits/sec (2µS/bit) MFM 250K bits/sec (4µS/bit) FM
Disc speed Latency time (1/2 revolution) Seek time - track to track - maximum Settling time Random average seek time (inc. settling time) Head load time	360 rpm 83 ms 10 ms 760 ms 10 ms 260 ms 60 ms	360 rpm 83 ms 3 ms 228 ms 20 ms 96 ms 40 ms

Note: (*) On drive 94Ø6 may also be loaded discettes single density, 1 sided, to be written/read according format Ø.

Table 16.2 DRIVE CHARACTERISTICS

```
**********************************************************************
* Warning: 1. Never switch off power with a discette in.             *
*                                                                    *
*          2. Only insert a discette if the spindle is rotating.     *
**********************************************************************
```

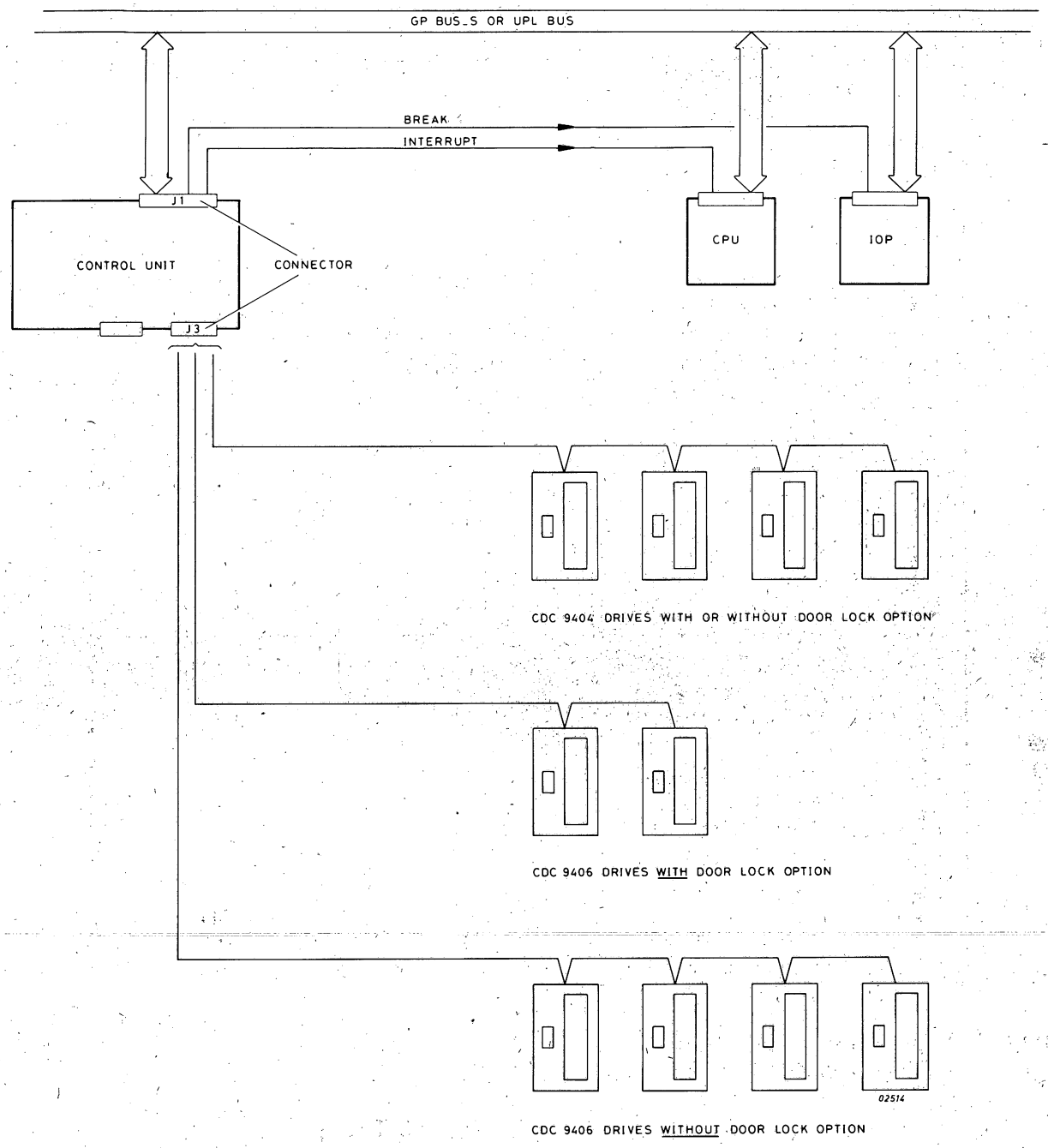
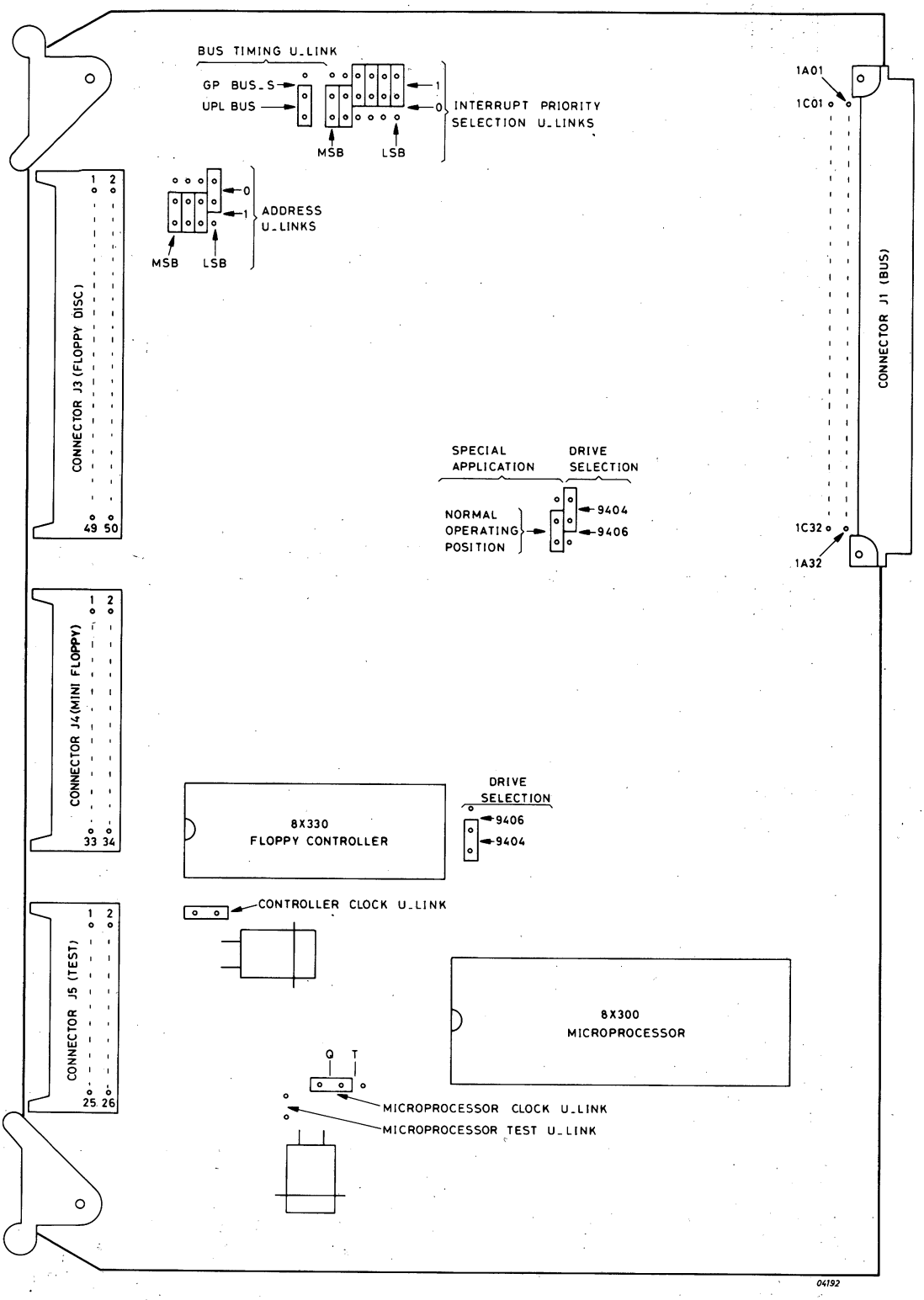


Figure 16.1 POSITION OF CU IN THE SYSTEM



Interrupt U-links for priority level 15 (001111)
Address U-link shown for CU address 14 (1110)
Bus timing link shown for use of CU with UPL Bus
Drive selection links (2) for use with type 9404 drive
Special application link shown in its normal operating position
Microprocessor clock link shown in position for normal operation
Controller clock link normally fitted, microprocessor test link not normally fitted.

Figure 16.2 U-LINK SETTING

INITIAL PROGRAM LOADING

The IPL can be loaded from floppy disc using the standard P800 bootstrap (P843-053 sequential and disc bootstrap). The control panel data switches must be positioned as follows;

0	1	2	3	4 5 6 7	8	9	10 11	12	13 15
0	1	1	0	Sector No. (0-15)0	1	1	Drive No.		CU Address

With this bootstrap the IPL is loaded from cylinder 0, head 0. This track is always formatted with format 0 (single density, 26 sectors/track and 128 bytes/sector).

POWER FAILURE/AUTOMATIC RESTART

The CU and disc drive will be restarted after a power failure without operator action. Information on the disc will not be destroyed but a sector of the disc being written when a power failure occurs must be completely rewritten after the CU is restarted.

DRIVE CONTROL

Up to four drives may be controlled from a single CU but all drives must be of the same type. The drives cannot operate simultaneously, a command for one drive must be finished before a command for another drive is sent by the CPU.

STRAP SETTINGS

U-Links on the card are used to select;

- CU address
- Binary interrupt priority level (when binary interrupts are used)
- Bus timing for exchange timing signal TSMN
- Drive type selection
- Special Applications
  These U-links are set at system installation time. Two other U-links are provided for test purposes.
- Microprocessor test U-links, not normally fitted.
- Microprocessor clock input selection, set at position 'Q' during normal operation of the card. Set at position 'T' for testing the card.
- Disc controller chip clock input U-link, fitted during normal operation of the card. Removed when the card is under test.

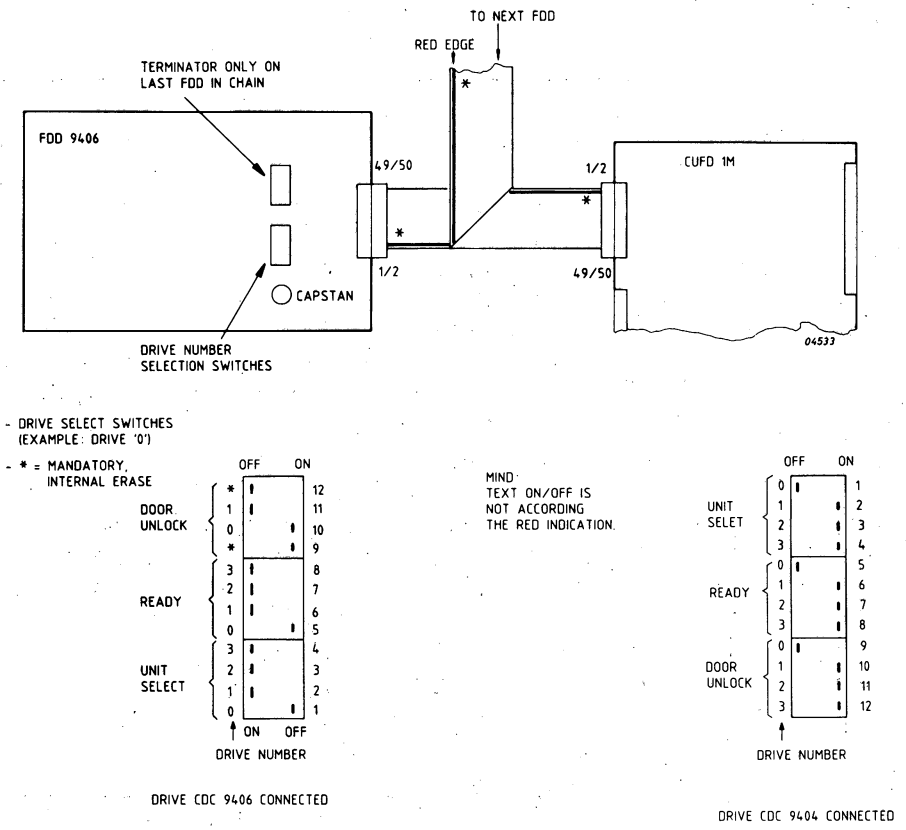


Figure 16.3 INSTALLATION DETAILS

16.5 INTERFACE CONNECTIONS

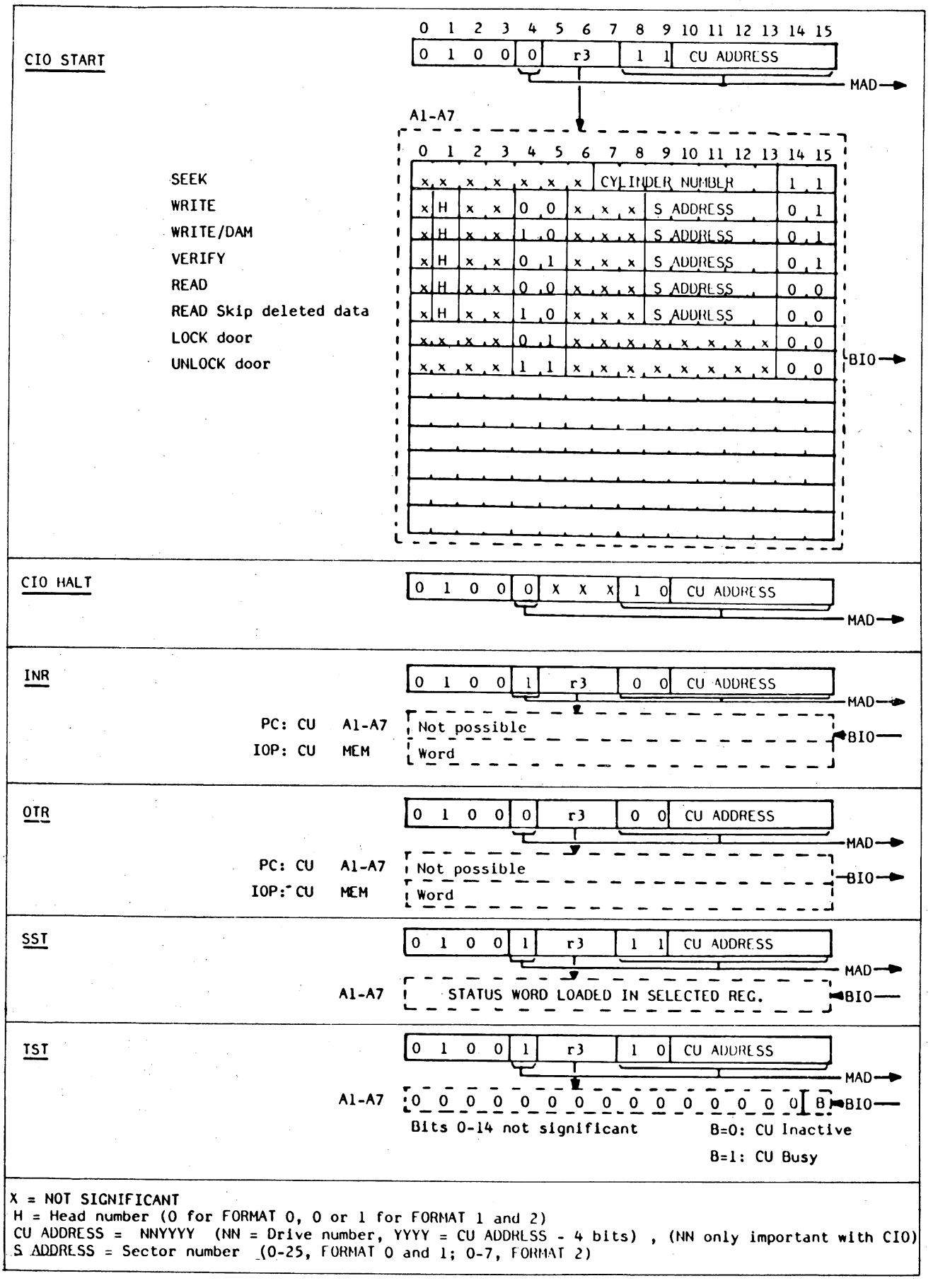
CU-Drive Interface

Pin No.	Signal Mnemonic	Signal Function	
3J01-43, 49 (odd numbers)	0V	Ground	
3J02	RDLN	Read data/clock composite signal	
3J04	HLN	Head load signal	
3J06	TRON	Track Zero detect	
3J08	INDN	Index Pulse	
3J10	LWCN	Low write current select	
3J12	STEPN	Each pulse of STEPN moves the head one track	
3J14	DIRN	in the direction specified by DIRN	
3J16	WEN	Write Enable signal	
3J18	WDN	Write Data signal	
3J20	SELON	Drive unit 1 ready selection signal	
3J22	SEL1N	Drive unit 2 ready selection signal	
3J24	SEL2N	Drive unit 3 ready selection signal	
3J26	SEL3N	Drive unit 4 ready selection signal	
5A28	RDYON	Drive unit 1 ready signal	
3J30	RDY1N	Drive unit 2 ready signal	
3J32	RDY2N	Drive unit 3 ready signal	
3J34	RDY3N	Drive unit 4 ready signal	
3J36	WPRN	Write protected disc	
3J38, 44, 46	--	Not Used	
3J40	DC4ON	Unit 1 door lock (9404)	Head Select (9406)
3J42	DC42N	Unit 2 door lock (9404)	Unit 1 door lock (9406)
3J45	--	Not used (9404)	Special applications
3J47	--	Not used (9404)	(see table below)
3J48	DC48N	Unit 3 door lock (9404)	Unit 2 door lock (9406)
3J50	DC5ON	Unit 4 door lick (9404)	Discette type (9406)

SPECIAL APPLICATIONS

CU signal name	Pin No.	CU function with 9404	9404 drive signal name	CU function with 9404	9406 drive signal name
DC4ON	40	Lock unit 0	Lock unit 1	Head select	Head select
DC42N	42	Lock unit 1	Lock unit 2	Lock unit 0	Lock unit 1
DC45N	45	--	Ground	Lock unit 2	Ground
DC47N	47	--	Ground	Lock unit 3	Ground
DC48N	48	Lock unit 2	Lock unit 3	Lock unit 1	Lock unit 2
DC5ON	50	Lock unit 3	Lock unit 4	Disc type	Disc type

Table 16.3 CONNECTIONS TO FLOPPY DISC DRIVES (CONNECTOR J3)



X = NOT SIGNIFICANT
H = Head number (0 for FORMAT 0, 0 or 1 for FORMAT 1 and 2)
CU ADDRESS = NNYYYY (NN = Drive number, YYYY = CU ADDRESS - 4 bits) , (NN only important with CIO)
S ADDRESS = Sector number (0-25, FORMAT 0 and 1; 0-7, FORMAT 2)

Figure 16.4 INSTRUCTION/COMMAND-WORD FORMATS

16.6.1 STATUS WORD

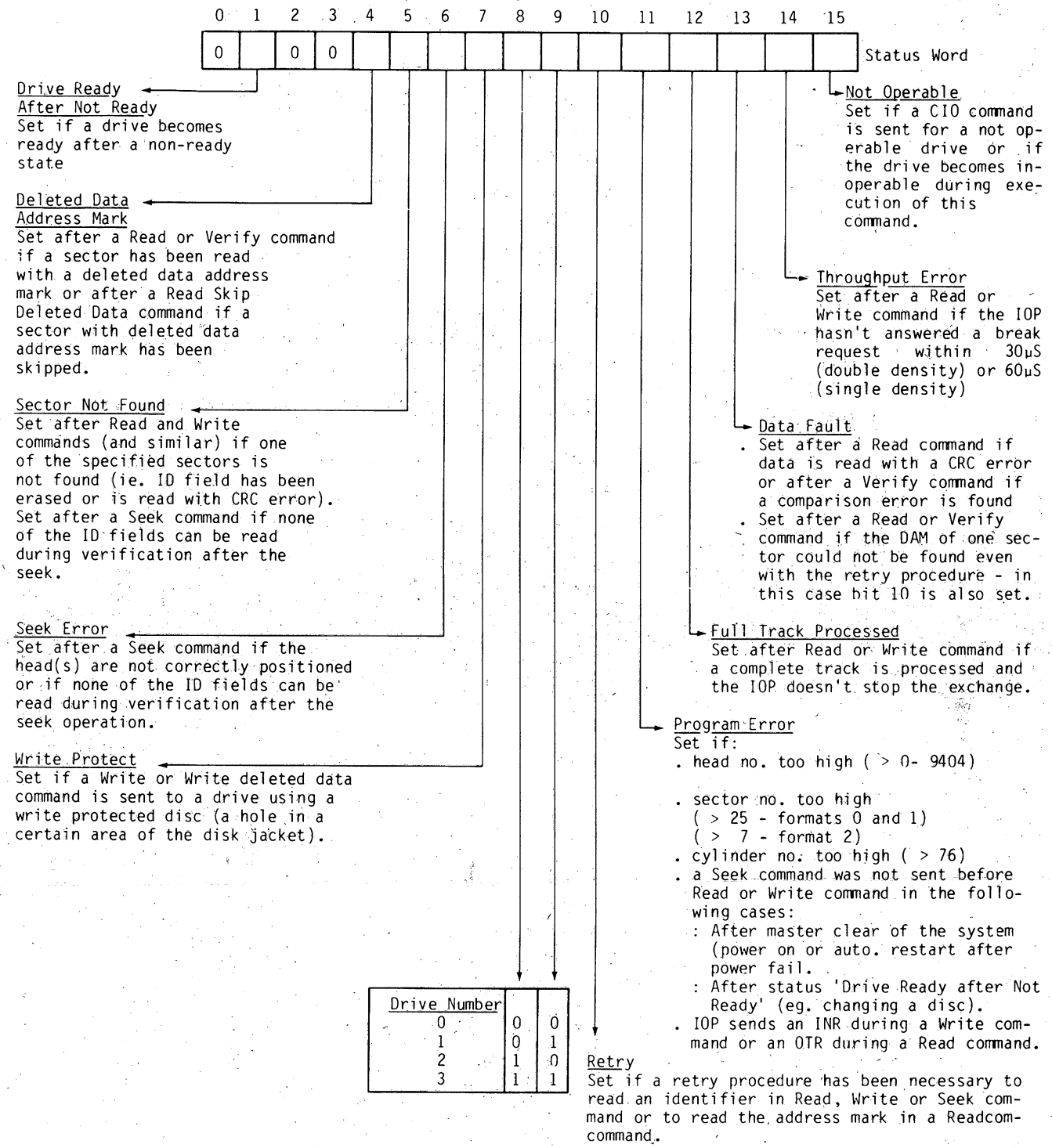


Figure 16.5 EXPLANATION OF STATUS WORD

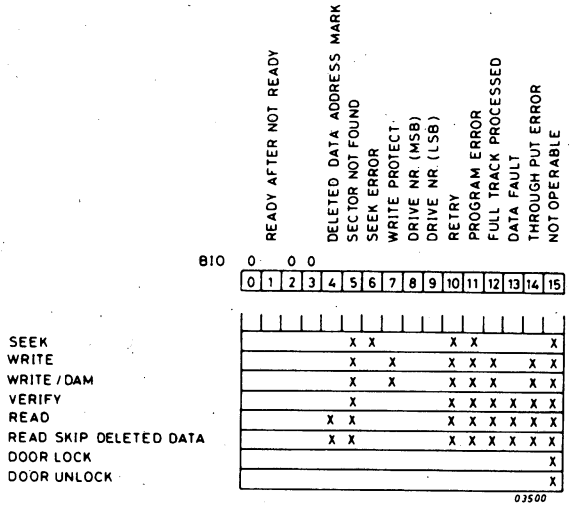


Figure 16.6 STATUS WORD: POSSIBLE CONFIGURATION

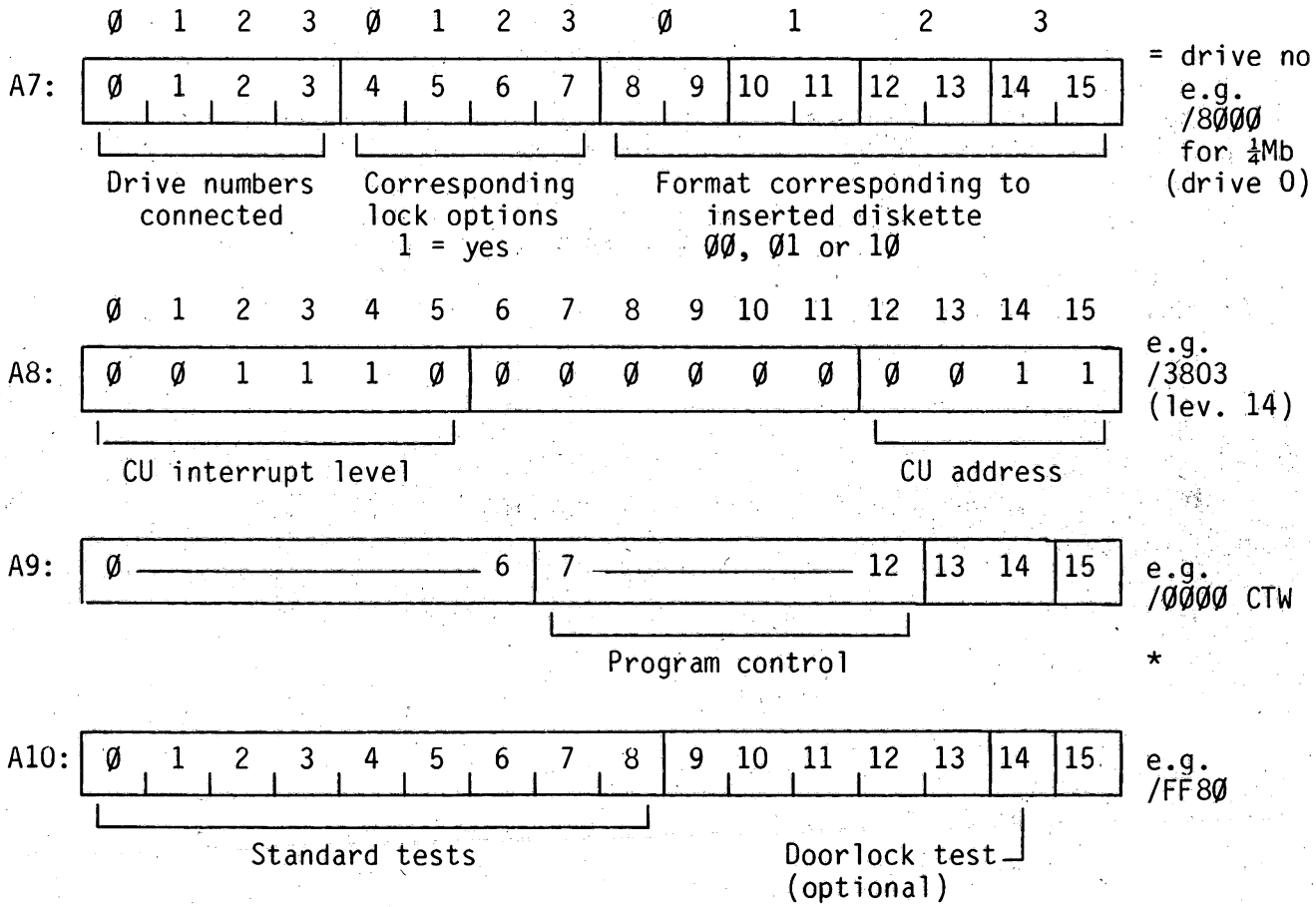
16.7 SHORT DESCRIPTION OF TEST PROGRAMS

TESTPROGRAM BF1MZ (PTS-115)

For testing floppy drives connected to the 1Mb CU
RTC and PF/AR allowed

Procedure:

- IPL
  Program displays /7ØØ = restart point = stop on interrupt
- ==== Load Scratch Diskette! ====
- Fill in registers.



- RTC on
  /7ØØ is normal end (restart) of program
  /5EØ is information stop
  /5FØ is error stop

* Note: The present version of F1MZ prints the program name. Selection of "no output" (reg A9 = /ØØ1Ø) is not possible.

For further information see the official description of the testprograms.

BF1MZ tested:

The Testprogram comprizes can perform the following 9 checks:

Check Ø - IFØØØØ Control Unit Test
Check 1 - IFØØØ1 Control Unit Test (contd)
Check 2 - IFØØØ2 Write on entire diskette
Check 3 - IFØØØ3 Write on sectors sequentially and verify the entire track
Check 4 - IFØØØ4 Write an entire track and verify sectors sequentially
Check 5 - IFØØØ5 Write statement initialized with IOP Read
Check 6 - IFØØØ6 Write a buffer shorter than the sector length
Check 7 - IFØØØ7 Write and read deleted data address marks
Check 8 - IFØØØ8 Random seek commands
Check E - IFØØØE Door lock/unlock test

The Check Ø must only be run once after the MC button is pushed and the loop on test option is not available.
The Check E is considered as an optional check (i.e. it can only be performed with drives having the LOCK option) and must be run separately.

Procedure	5111 991 11361	= Procedure BF1MZ	5111 991 11Ø83
		with addendum PTS8ØØØ	5111 991 11381
Listing	5111 991 11271		
Program	5111 199 62461		

```
00000                          IDENT    ADJF1M
00001                  *PROGRAM TO ADJUST 1M FLOPPY P800 SYSTEMS
00002                  *
00003                  * AFTER IPL THE PROGRAM STOPS
00004                  *
00005                  * LOAD ALIGNMENT FLOPPY IN DRIVE 0
00006                  *
00007                  * PROGRAM SELECTION AFTER EACH TIME THE PROGRAM STOPS:
00008                  *   (REG A1)   1: ALIGNMENT HEAD 0 (CYLINDER 38)
00009                  *              2:           HEAD 1
00010                  *              3: INDEX TO BURST ADJUSTM. HEAD 0 (CYL. 1)
00011                  *              4:                      HEAD 1
00012                  *           BEFORE NEXT STEP, LOAD A SCRATCH FLOPPY
00013                  *              5: CYLINDER ZERO ADJUSTMENT (400 X SEEK BETWEEN CYL 0 AND 1)
00014                  *           BEFORE NEXT STEP, LOAD ALIGNMENT FLOPPY AGAIN
00015                  *              6: CHECK ALIGNMENT HEAD 0
00016                  *              7:                 HEAD 1
00017                  *
00018                  *            > 7: STOP, UNLOAD THE HEADS
00019                  * TO START PRESS RUN BUTTON
00020                  ************************************************************
00021  0000                    RES      /40
00022  0080  FFFF              DATA     /FFFF,0
       0082  0000
00023        0003      ADR     EQU      3
00024  0084  208F      START   INH
00025  0086  0101              LDK      A1,1                    DEFAULT SELECTION PROG 1
00026  0088  207F      INPUT   HLT
00027  008A  4FC3              SST      A7,ADR                  RESET READY INT JUST IN CASE
00028  008C  2107              ANK      A1,7                    MASK VALUE 1 TILL 7
00029  008E  8204              LDR      A2,A1
00030  0090  580A              RB(Z)    INPUT                   WRONG BIT
00031  0092  1A01              SUK      A2,1                    PROG 1?
00032  0094  5016              RF(Z)    PROG1
00033  0096  1A01              SUK      A2,1                    2?
00034  0098  5020              RF(Z)    PROG2
00035  009A  1A01              SUK      A2,1                    3?
00036  009C  5022              RF(Z)    PROG3
00037  009E  1A01              SUK      A2,1                    4?
00038  00A0  502C              RF(Z)    PROG4
00039  00A2  1A01              SUK      A2,1                    5?
00040  00A4  502E              RF(Z)    PROG5
00041  00A6  1A01              SUK      A2,1                    6?
00042  00A8  503E              RF(Z)    PROG6
00043                  *
00044                  *****HEAD 1 ALIGNMENT CHECK*****
00045                  *
00046  00AA  570E      PROG7   RF       PROG2
00047                  *
00048                  *****HEAD 0 ALIGNMENT*****
00049                  *
00050  00AC  0200      PROG1   LDK      A2,0                    READ HEAD 0
00051  00AE  049B              LDK      A4,/9B                  SEEK CYL 38
00052  00B0  44C3              CIO      A4,1,ADR                EXEC SEEK COMM
00053  00B2  4FC3              SST      A7,ADR
00054  00B4  5C04              RB(NA)   *-2
00055  00B6  42C3              CIO      A2,1,ADR                EXEC READ COMM
00056  00B8  5F32              RB       INPUT
00057                  *
00058                  *****HEAD 1 ALIGNMENT*****
00059                  *
00060  00BA  8220      PROG2   LDKL     A2,/4000                READ HEAD 1
       00BC  4000
00061  00BE  5F12              RB       PROG1+2
00062                  *
00063                  *****INDEX TO BURST HEAD 0 ADJUST*****
00064                  *
00065  00C0  0200      PROG3   LDK      A2,0                    READ HEAD 0
00066  00C2  0407              LDK      A4,7                    SEEK CYL 1
00067  00C4  44C3              CIO      A4,1,ADR
00068  00C6  4FC3              SST      A7,ADR
00069  00C8  5C04              RB(NA)   *-2
00070  00CA  42C3              CIO      A2,1,ADR                READ
00071  00CC  5F46              RB       INPUT
00072                  *
00073                  *****INDEX TO BURST CHECK HEAD 1*****
00074                  *
00075  00CE  8220      PROG4   LDKL     A2,/4000                READ HEAD 1
       00D0  4000
00076  00D2  5F12              RB       PROG3+2
00077                  *
00078                  *****CYLINDER 0 ADJUSTMENT*****
00079                  *
00080  00D4  8220      PROG5   LDKL     A2,800                  400 TIMES REPEAT SEEK
       00D6  0320
00081  00D8  0403              LDK      A4,3                    SEEK CYL 0
00082  00DA  44C3              CIO      A4,1,ADR
00083  00DC  4FC3              SST      A7,ADR
00084  00DE  5C04              RB(NA)   *-2
00085  00E0  340C              XRK      A4,/C                   SEEK CYL 3, 0, 3, ETC.
00086  00E2  1A01              SUK      A2,1
00087  00E4  5C0C              RB(NZ)   PROG5+6                 400 TIMES ?
00088  00E6  5F60              RB       INPUT                   NEXT STEP
00089                  *
00090                  *****HEAD 0 ALIGNMENT CHECK*****
00091                  *
00092  00E8  5F3E      PROG6   RB       PROG1
00093                          END      START
```

```
00000                           IDENT    F1SEEK
00001                   * SEEK TEST FOR F1M-Z (FLOPPY CU 1MB)
00002                   * SEEKS BETWEEN CYL 00 AND 32
00003                   * DRIVE 0 ONLY. STATUS IN A5
00004                   * IF SEEKING, YOU HEAR THE REGULAR MOVEMENT
00005                   *
00006                   * REG A4 IS PRESET BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
00007                   *             /0003    0 0 0 0 0 0 0 0 0 0  0  0  0  0  1  1
00008                   *                                       -----------------
00009                   *                                       SEEK CYLINDER NUMBER
00010          0003     DA       EQU      3
00011    0000           DA       RES      /40
00012    0080  FFFF     DATA     DATA     /FFFF
00013    0082  0000              DATA     0
00014    0084  0403     START    LDK      A4,3
00015    0086  207F              HLT
00016    0088  20BF              INH
00017    008A  44C3     RET      CIO      A4,1,DA              SEEK
00018    008C  5C04              RB(4)    *-2
00019    008E  4DC3              SST      A5,DA                STATUS
00020    0090  5C04              RB(4)    *-2
00021    0092  8514              LDR      A5,A5                SET CR ACCORDING STATUS
00022    0094  5104              RF(1)    ST
00023    0096  3480              XRK      A4,/80               CHANGE CYL 00 - 32, ETC
00024    0098  5F10              RB       RET
00025    009A  207F     ST       HLT
00026                           END      START


00000                           IDENT    F1LOOP
00001                   *
00002                   * PROGRAM TO WRITE AND READ A SECTOR CONTINUOUSLY (CU 1MB)
00003                   * WRITE BUFFER /200 UP UNTIL /27E
00004                   * READ BUFFER /300 UP UNTIL /37E
00005                   * DRIVE 0 ONLY.  REG A5 CONTAINS STATUS
00006                   *
00007                   *    PRESET A1: BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
00008                   *             /0001  0 0 0 0 0 0 0 0 0  0  0  0  0  0  1
00009                   *              =CIO    -                I-----------I     -
00010                   *                    HEAD               SECTORNO.         WRITE
00011                   *
00012                   *           A2: BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
00013                   *            /C040  1 1 0 0 0 0 0 0 0 1  0  0  0  0  0  0
00014                   *              =WER1   -                I--------------------I
00015                   *                    WRITE                BLOCK LENGTH
00016                   *
00017                   *           A3: BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
00018                   *            /0200  0 0 0 0 0 0 1 0 0 0  0  0  0  0  0  0
00019                   *              =WER2 I-----------------------------------I
00020                   *                                BUFFER  ADDRESS
00021                   *
00022                   *           A4: BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
00023                   *            /0003  0 0 0 0 0 0 0 0 0 0  0  0  0  0  1  1
00024                   *            =SEEK                I-----------------I
00025                   *                                   CYL NUMBER
00026                   *
00027                   * CHECK CORRECT RUNNING:STOP PROGRAM , COMPARE IF /200 AND ON
00028                   * EQUALS /300 AND ON.
00029                   *    NOTE: DISCETTE FORMAT 0,SS,SD  26 SECTORS,64 WORDS/SECTOR
00030                   * ERROR: STATUS STOP AT /BC (/00BE AT HHP):A5 CONTAINS STATUS WORD
00031                   *
00032          0003     DA       EQU      3
00033    0000           DA       RES      /40
00034    0080  FFFF     DATA     DATA     /FFFF
00035    0082  0000              DATA     0
00036    0084  0101     START    LDK      A1,1                 PRESET REG
00037    0086  8220              LDKL     A2,/C040
         0088  C040
00038    008A  8320              LDKL     A3,/200
         008C  0200
00039    008E  0403              LDK      A4,3
00040    0090  207F              HLT
00041    0092  20BF              INH
00042    0094  44C3              CIO      A4,1,DA              SEEK
00043    0096  5C04              RB(4)    *-2
00044    0098  4DC3              SST      A5,DA                STATUS
00045    009A  5C04              RB(4)    *-2
00046    009C  8514              LDR      A5,A5
00047    009E  511C              RF(1)    ST                   STATUS FAULT
00048    00A0  7206     RET      WER      A2,DA+DA
00049    00A2  7307              WER      A3,DA+DA+1
00050    00A4  41C3              CIO      A1,1,DA              PREPARE WRITE (OR READ)
00051    00A6  5C04              RB(4)    *-2
00052    00A8  4DC3              SST      A5,DA                STATUS
00053    00AA  5C04              RB(4)    *-2
00054    00AC  8514              LDR      A5,A5
00055    00AE  510C              RF(1)    ST                   STATUS FAULT
00056    00B0  3101              XRK      A1,1
00057    00B2  8220              XRKL     A2,/4000             CHANGE WRITE TO READ,VICE VERSA
         00B4  4000
00058    00B6  8320              XRKL     A3,/0100
         00B8  0100
00059    00BA  5F1C              RB       RET
00060    00BC  207F     ST       HLT
00061                           END      START
```

17 MINI FIXED DISC (X1250) - CONTROL UNIT P827-140 (MDDZ)

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17.1 X1250-CONTROL UNIT IDENTIFICATIONS

Type number : P827-140 (MDD-FXD)

Testprogram : BZ1250
Channel : IOPZR/MIOP, Break connection 1A05, Interrupt 1C05
Devices type : Philips X1250, 6 Mbytes capacity formatted, 4 max. (P827-001)
Transfer rate : 2 M bits/sec

Recording
method : Modified Frequency Modulation (MFM).
Power (CU) : +5V ±5%, 2.4A

12NC code on the sticker on the board.

MDD (FXD): 5111 199 6950X (5322 216 25424)

X = Modification level

17.2 INSTALLATION DETAILS

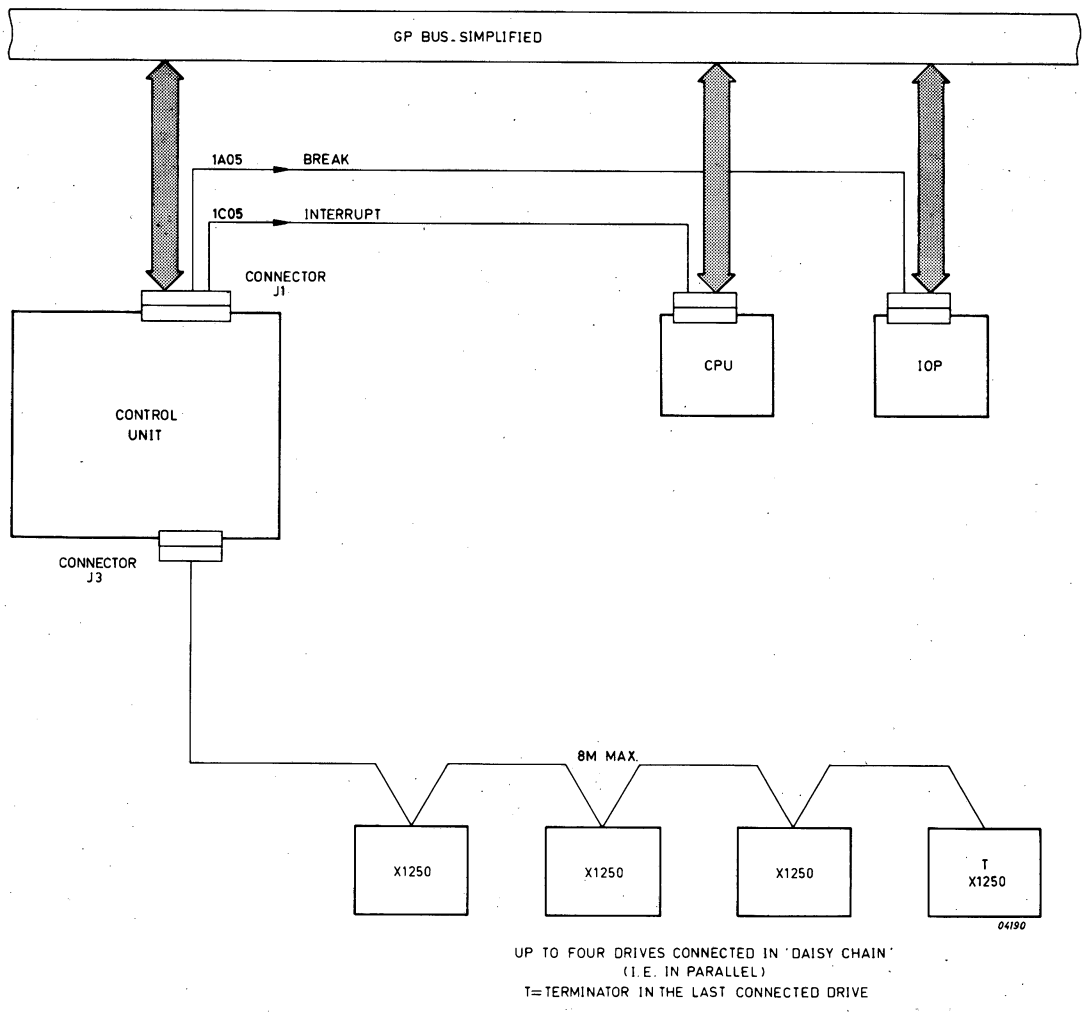


Figure 17.1 POSITION OF CU IN THE SYSTEM

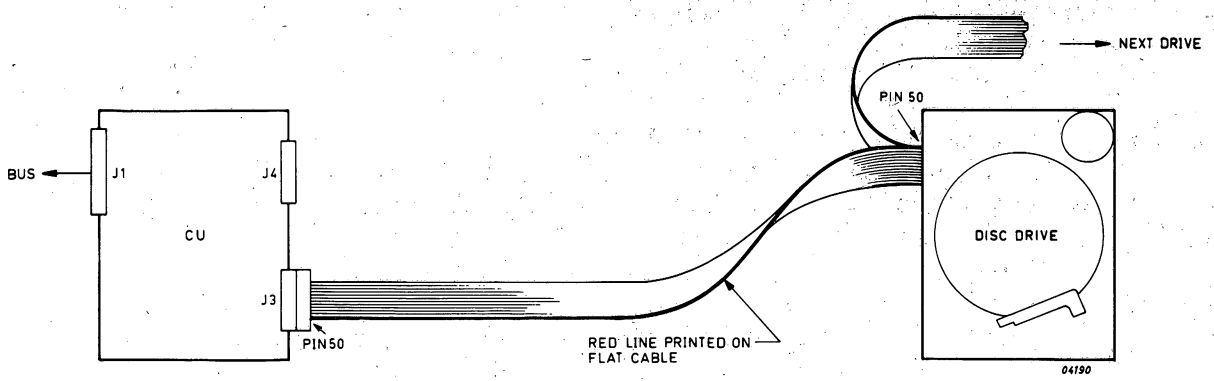
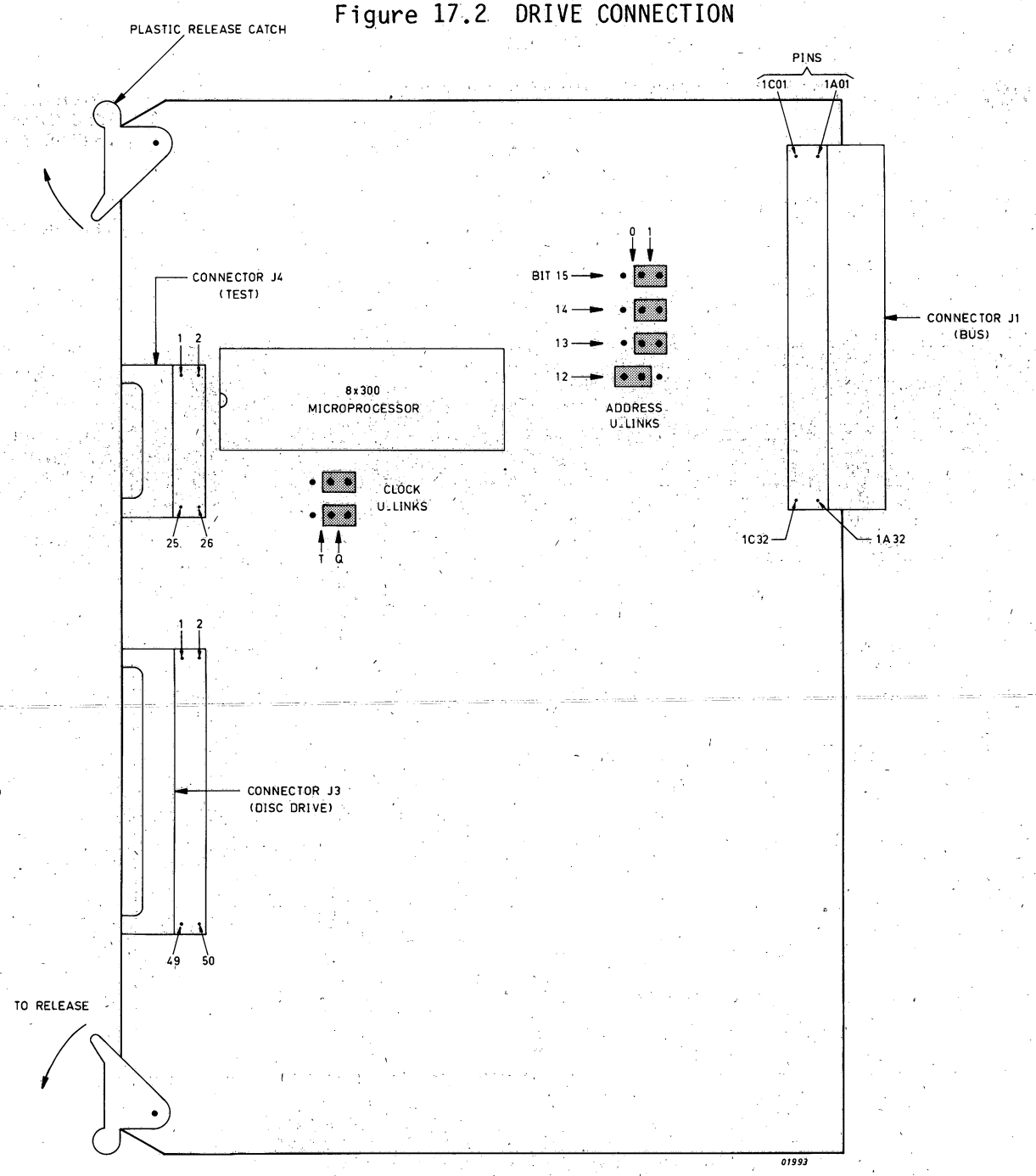


Figure 17.2 DRIVE CONNECTION



ADDRESS U-LINKS : ADDRESS SHOWN IS 0111 (7 STANDARD)
CLOCK U-LINKS : U-LINKS SHOWN FOR NORMAL OPERATION OF CARD (Q)

Figure 17.3 U-LINK SETTINGS CU

Strap setting X125Ø:

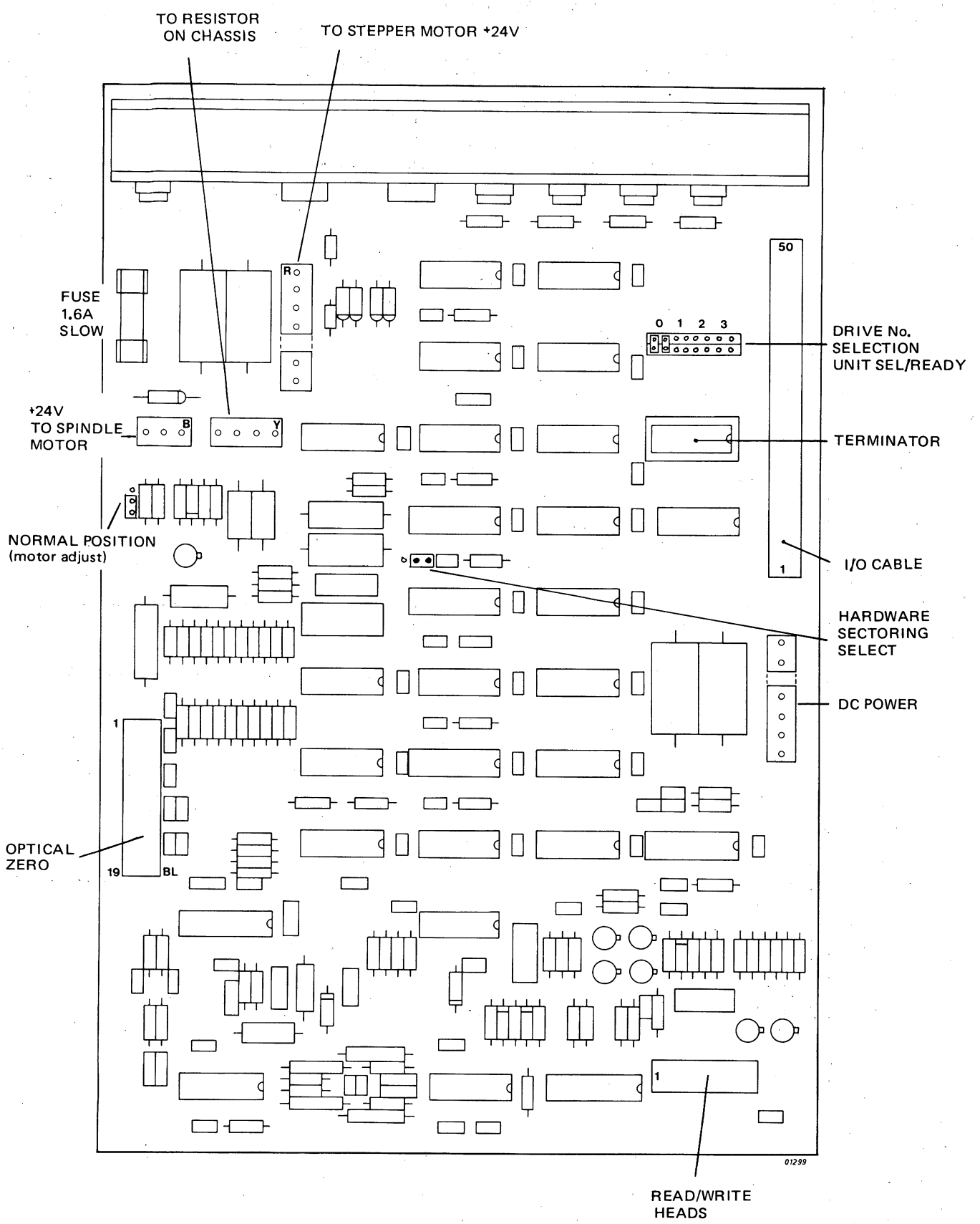


Figure 17.4 U-LINK SETTING X1250

17.3 INTERFACE CONNECTIONS

Pin Number	Signal Mnemonic	Signal Function
3J02	RDLN	Serial data input from disc
3J04	-	not used
3J06	TRØN	Track zero detect
3J08	SECN	Sector pulse
3J10	LWCN	Low write current select
3J12	STEPN	┐ Each pulse of STEPN moves the disc head one
3J14	DIRN	┘ track in the direction specified by DIRN
3J16	WEN	Write enable
3J18	WDLN	Serial data output to disc
3J20,22,24,26	SELON-3N	Drive selection signal from CU
3J28,30,32,34	RDYON-3N	Drive ready signal from drive
3J36,38	-	not used
3J40	SLHN	Select lower head
3J42	-	not used
3J44	WF	not used
3J46	WFR	not used
3J48,50	-	not used

Table 17.1 CONNECTIONS TO DISC DRIVE (CONNECTOR J3)

Pin Number	Signal Mnemonic	Signal Function
4J01,3	5V	Power Supply
4J05-21 (odd nos.)	RAD0-8	PROM address lines
4J02-16 (even nos.)	DATA7-0	CU internal bus lines
4J18	CPXV1	┐ Test input for microprocessor clock
4J20	CPXV2	┘
4J22,24	0V	Power supply return

Table 17.2 TEST CONNECTIONS (CONNECTOR J4)

DRIVE INTERFACE

LINE FUNCTION	PIN No.	
Ground	201	A
Read data/clock composite	202	B
Ground	203	C
Not to be used	204	D
Ground	205	E
Track 000	206	F
Ground	207	H
Index (optional sector pulse)	208	J
Ground	209	K
Low write current	210	L
Ground	211	M
Step	212	N
Ground	213	P
Direction	214	R
Ground	215	S
Write enable	216	T
Ground	217	U
Write data	218	V
Ground	219	W
Unit select 1	220	X
Ground	221	Y
Unit select 2	222	Z
Ground	223	AA
Unit select 3	224	BB
Ground	225	CC
Unit select 4	226	DD
Ground	227	EE
Unit ready interrupt 1	228	FF
Ground	229	HH
Unit ready interrupt 2	230	JJ
Ground	231	KK
Unit ready interrupt 3	232	LL
Ground	233	MM
Unit ready interrupt 4	234	NN
Ground	235	PP
Not to be used	236	RR
Ground	237	SS
Not to be used	238	TT
Ground	239	UU
Select lower head	240	VV
Ground	241	WW
Not to be used	242	XX
Ground	243	YY
Write fault	244	ZZ
Ground	245	AB
Write fault reset	246	AC
Ground	247	AD
Not to be used	248	AE
Ground	249	AF
Not to be used	250	AH

DESIGNATIONS FOR 'AMP' CONNECTORS

PL 100 - DC POWER CABLE

LINE FUNCTION	PIN No.
NOT USED	101
+5V d.c.	102
GROUND	103
+24V d.c.	104
NOT USED (Keyed)	105
+24V RETURN	106
ON-OFF WR. INH.	107

PL 300 - STEPPER MOTOR DRIVE

LINE FUNCTION	PIN No.
MOTOR DRIVE 01	301
MOTOR DRIVE 02	302
CATHODE D15	303
MOTOR DRIVE 03	304
NOT USED	305
MOTOR DRIVE 04	306
CATHODE D14	307

Track numbering is as follows:

Inner Track = Track No. 000
Outer Track = Track No. 230

Table 17.3 LINE FUNCTIONS

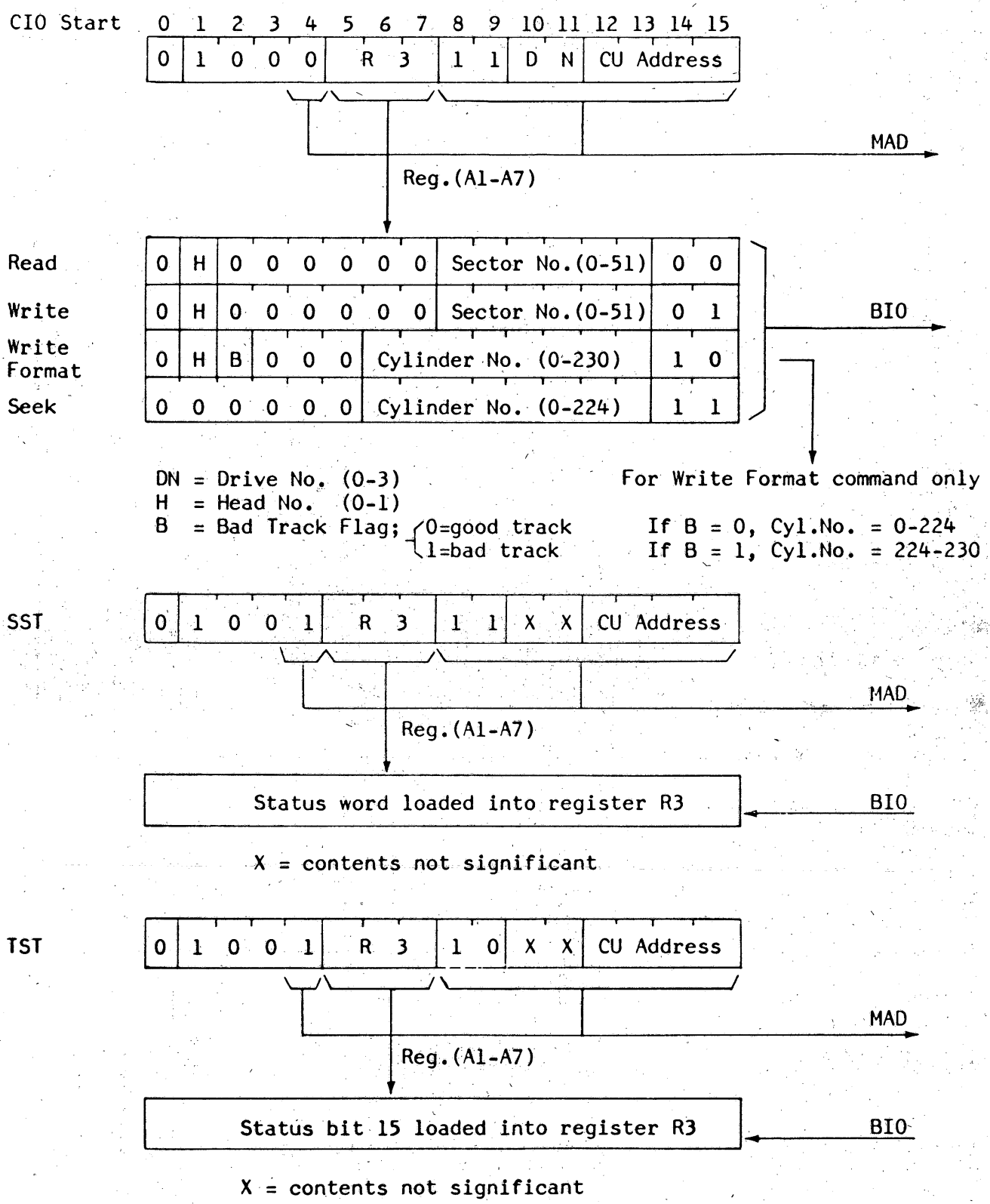
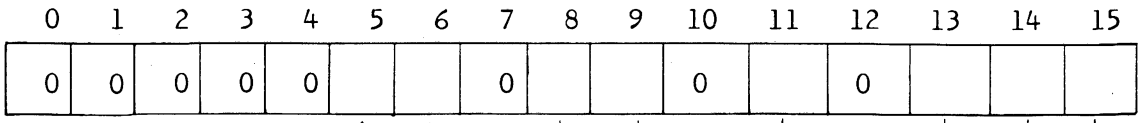


Figure 17.5 INSTRUCTION/COMMAND WORD FORMATS

17.4.1 STATUS WORD



SECTOR NOT FOUND
Set if a sector is not found during a Read or Write command. This can occur if there is no identifier with the searched sector number (formatting error or disc erasure) or if the searched identifier is read with a CRC error.

Drive No.	
0	00
1	01
2	10
3	11

DRIVE NOT OPERABLE
Set if the drive selected in a CIO command is not operable or becomes inoperable during execution of a CIO command.

THROUGHPUT ERROR
Set if IOP does not answer a break request within 6.5 uS.

SEEK ERROR
Set if the head is not correctly positioned, after verification, at the end of a Seek command. Set if it is not possible to read at least one identifier during the initial Read Identifier function of a Write Format command.
Set if the Seek to Replacement Track function in the case of a bad track during a Read or Write command is not correctly performed.

DATA FAULT
Set if data is read with a CRC error.

PROGRAM ERROR
Set if the sector no. in a Read or Write command is >51
Set if the cylinder no. in Seek or Write Format command is >230
Set if the IOP sends an INR command during a Write command or an OTR during a Read command.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Seek						*	*					**				*
Write						*	*					*			*	*
Read							*					*		*	*	*
Write							*					**				*
Format																

Sector Not Found
Seek Error
Drive No.
Program Error — Cylinder No. greater than 230**
Sector No. greater than 51*
Data Fault
Throughput Error
Not Open

TEST STATUS COMMAND - TST

This command may be used before any CIO command, to test if the CU is busy. The command is always accepted. When the command is received the CU sets BIO line 15 of the bus if it is busy (ie is presently executing a command) or does nothing if it is not busy.

17.4.2 TRACK LAYOUT

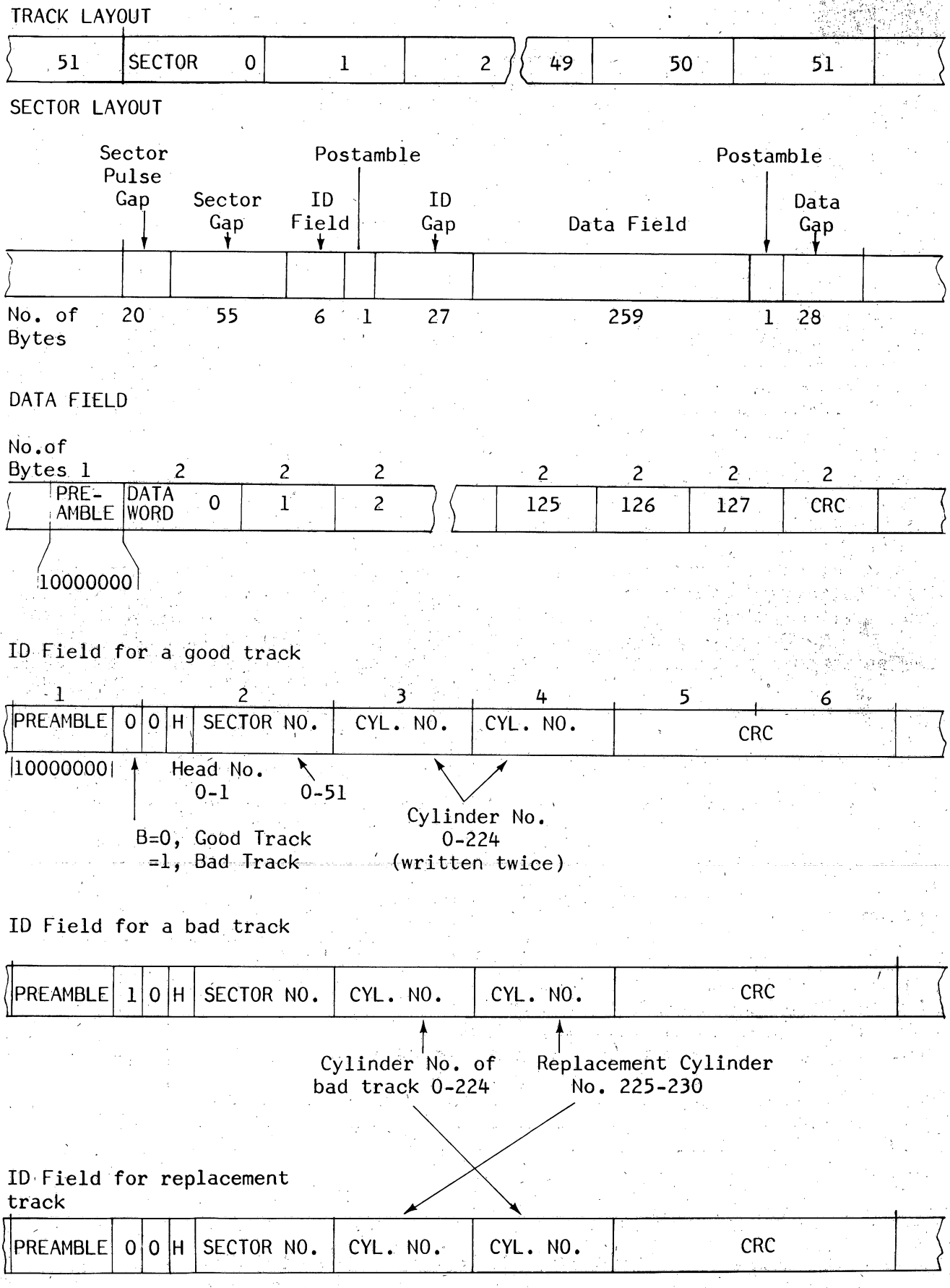


Figure 17.6 DATA LAYOUT ON DISC

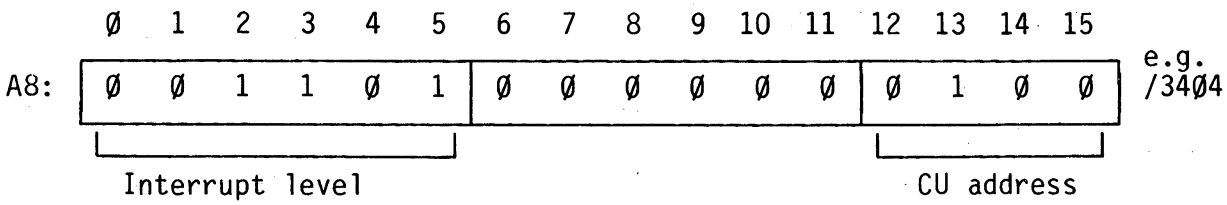
17.5 SHORT DESCRIPTION TESTPROGRAMS

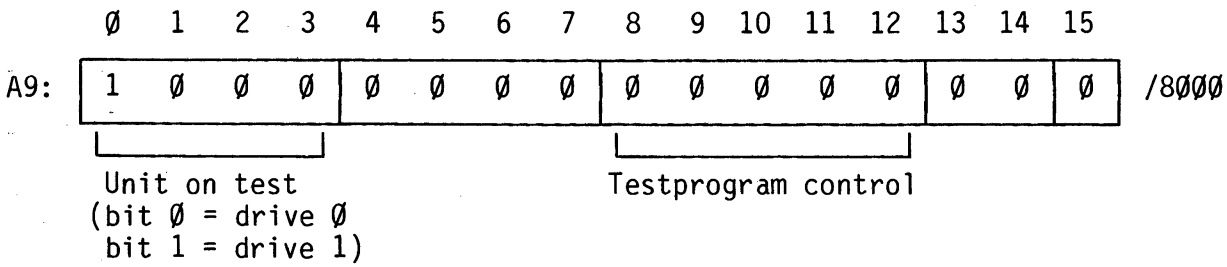
TESTPROGRAM BZ125Ø

```
**********************************************
* Warning: Customer data will be overwritten. *
**********************************************
```

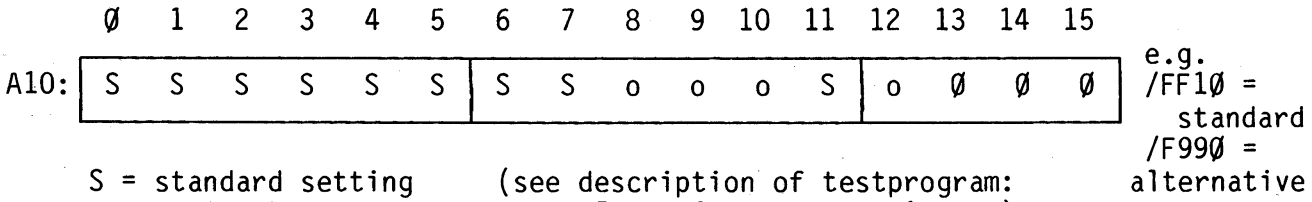
Procedure:

- IPL
  Program displays /7ØØ (= restart point, stop after interrupt)
  Change contents of registers:





Checks to be executed:

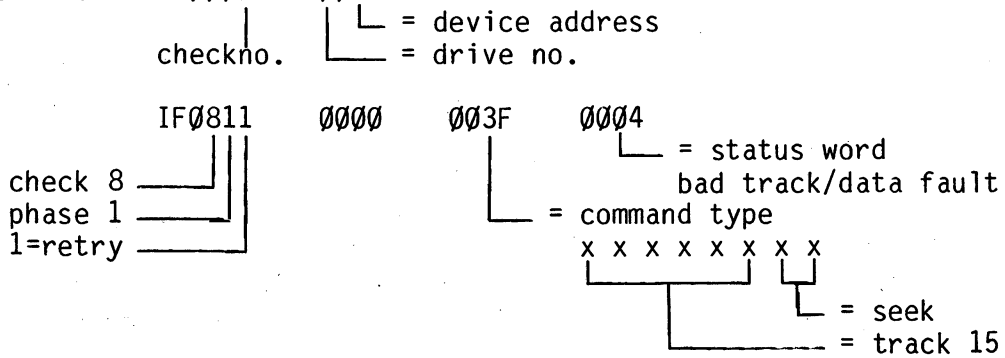


S = standard setting
o = optional setting

(see description of testprogram: Test 5 and 6 take about ¼ hour)

Note: Check 8 = bad track check
* bad track pattern will be written
* 6 bad tracks gives "bad disc"

Switch on RTC
Information stop /5EØ
Error: Program stops at /5FØ
Information on terminal: IFØØØx DØØ4



BZ125Ø tested:
The program is divided into 13 checks:

Check Ø - Test CU
Check 1 - Format all the discs
Check 2 - 5Ø random seeks
Check 3 - Write from cylinder Ø to 224
Check 4 - Read from cylinder Ø to 224
Check 5 - Write the disc with a pattern choosen by operator
Check 6 - Read the disc, pattern written in ch. Ø5
Check 7 - Test "program error"
Check 8 - Read the disc, if a bad status, a write format with
a bad track is sent
Check 9 - "Seek" or "write" format command
Check A - "Write" or "Read" command
Check B - Write format with bad track test
Check C - Chaining sectors test

Procedure	5111 991 1Ø151	= Procedure BZ125Ø	5111 991 Ø9222
		with addendum PTS8ØØØ	5111 991 11381
Listing	5111 991 1Ø161		
Program	5111 199 65621		

17.6 SHORT ROUTINES

```
                        IDENT    MDSEEK
                    *
                    * THIS PROGRAM SEEKS BETWEEN CYL 00 AND 32
                    * SEEK TEST FOR X1250
                    * DRIVE 0 ONLY.  STATUS IN A5
                    * IF SEEKING, YOU HEAR THE REGULAR MOVEMENT
                    *
                    * REG A4 IS PRESET: BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
                    *             /0003     0 0 0 0 0 0 0 0 0 0  0  0  0  0  1  1
                    *                                        I------------------I
                    *                                          SEEK CYLINDER NO
                    *  STATUS ERROR: STOP AT /9C (HHP /009E)
                    *
        0004        DA       EQU      4
0000                         RES      /40
0080    FFFF        DATA     DATA     /FFFF
0082    0000                 DATA     0
0084    0403        START    LDK      A4,3                    PRESET REG
0086    207F                 HLT
0088    20BF                 INH
008A    44C4        RET      CIO      A4,1,DA                 SEEK
008C    5C04                 RB(4)    *-2
008E    4DC4                 SST      A5,DA                   STATUS
0090    5C04                 RB(4)    *-2
0092    A520                 ANKL     A5,/0617                CLEAN STATUS
0094    0617
0096    5104                 RF(1)    ST                      STATUS ERROR
0098    3480                 XRK      A4,/80                  CHANGE CYL 00 INTO 32 AND VICE VERSA
009A    5F12                 RB       RET
009C    207F        ST       HLT
                             END      START



                        IDENT    MDLOOP
                    *
                    * PROGRAM TO WRITE AND READ A SECTOR CONTINUOUSLY
                    *         WRITE BUFFER /200 UP UNTIL /2FE
                    *         READ BUFFER /300 UP UNTIL /3FE
                    * DRIVE 0 ONLY .  REG A5 CONTAINS STATUS
                    *
                    *      A1:        BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
                    *          /0001      0 0 0 0 0 0 0 0 0 0  0  0  0  0  0  1
                    *          =CIO         I               I-------------I     I
                    *                      HEAD              SECTORNO.       WRITE
                    *
                    *      A2:        BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
                    *          C080       1 1 0 0 0 0 0 0 1 0  0  0  0  0  0  0
                    *          =WER1        I               I-------------------I
                    *                     WRITE              BLOCK LENGTH
                    *
                    *      A3:        BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
                    *        /0200        0 0 0 0 0 0 1 0 0 0  0  0  0  0  0  0
                    *          =WER2      I-----------------------------------I
                    *                                BUFFER  ADDRESS
                    *
                    *      A4:        BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
                    *        /0003        0 0 0 0.0 0 0 0.0 0  0  0. 0  0  1  1
                    *          =SEEK                    I-----------------I
                    *                                     CYL NUMBER
                    *
                    * CHECK CORRECT RUNNING: STOP PROGRAM, COMPARE IF /200 AND ON
                    * EQUALS /300 AND ON.
                    *
0000                         RES      /40
0080    FFFF        DATA     DATA     /FFFF
0082    0000                 DATA     0
0084    0101        START    LDK      A1,1                    PRESET REG
0086    8220                 LDKL     A2,/C080
0088    C080
008A    8320                 LDKL     A3,/200
008C    0200
008E    0403                 LDK      A4,3
0090    207F        HLT      HLT
0092    20BF                 INH
0094    44C4                 CIO      A4,1,4                  SEEK
0096    5C04                 RB(4)    *-2
0098    4DC4                 SST      A5,4                    STATUS
009A    5C04                 RB(4)    *-2
009C    8514                 LDR      A5,A5                   SET CR ACCORDING STATUS
009E    511C                 RF(1)    ST                      STATUS ERROR
00A0    7208        RET      WER      A2,8
00A2    7309                 WER      A3,9
00A4    41C4                 CIO      A1,1,4                  START WRITE (OR READ)
00A6    5C04                 RB(4)    *-2
00A8    4DC4                 SST      A5,4                    STATUS
00AA    5C04                 RB(4)    *-2
00AC    8514                 LDR      A5,A5
00AE    510C                 RF(1)    ST                      STATUS ERROR
00B0    3101                 XRK      A1,1
00B2    B220                 XRKL     A2,/4000                CHANGE WRITE TO READ, VICE VERSA
00B4    4000
00B6    B320                 XRKL     A3,/0100
00B8    0100
00BA    5F1C                 RB(7)    RET
00BC    207F        ST       HLT
                             END      START
```

18 CARTRIDGE DISC DRIVE CONTROL UNIT P824-140 (CDDZ)

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18.1 DISC CONTROL UNIT - IDENTIFICATIONS

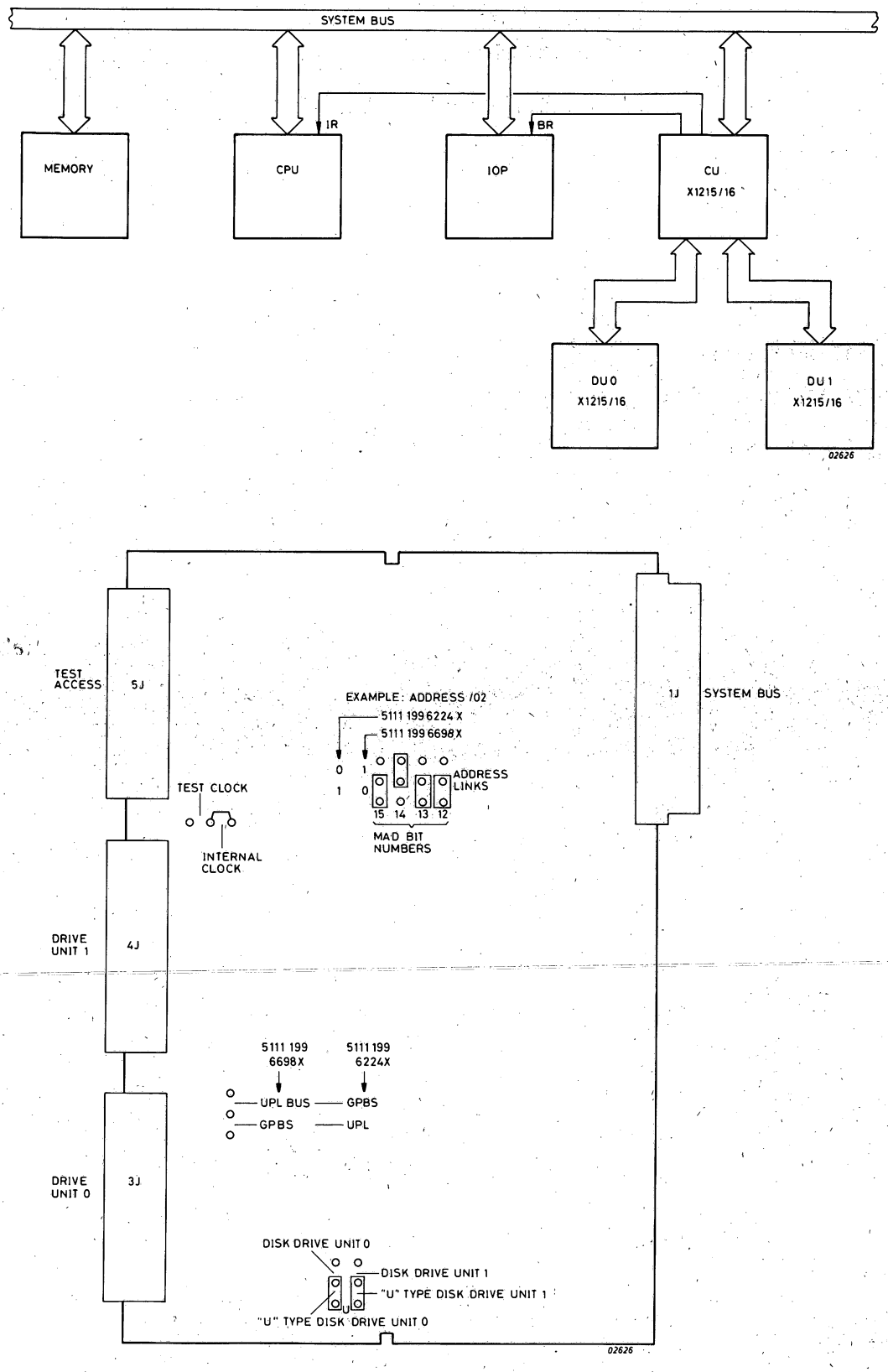
Type number	: P824-140 (CDDZ)
Test programs	: X1215: BZCDD1 X1216: BZ1216
Channel	: Hardware channel MIOP, IOPZR
Break-connection	: 1A05
Interrupt-connection	: 1C05
Devices	: 2x X1215 (2.7 Mb) - P824-012 or 2x X1216 (5.4 Mb) - P824-014
Power Consumption	: 5 Volt, 2.9 Amp

12NC code on the sticker on the board:

CDDZ: 5111 199 6698x (5322 216 25617)

X = Modification level.

18.2 INSTALLATION DETAILS



NOTE: A "U" TYPE DISK DRIVE UNIT IS ONE WHICH STOPS ON AN ERROR AND WHICH RESTARTS AUTOMATICALLY AFTER AN ERROR CONDITION HAS BEEN RECTIFIED

Figure 18.1 C.U. IN SYSTEM AND U-LINK SETTING

Pin No.	Signal	Function
J3-01	GND.	
02	CONN	Cylinder On Not
03	GND.	
04	URN	Unit Ready Not
05	GND.	
06	USA1N	Unsafe Action 1
07	GND.	
08	USA2N	Unsafe Action 2
09	GND.	
10	ATON	(Pin 10 is connected but signal ATON is not used)
11	GND.	
12	IPFON	Index Pulse Fixed Not
13	GND.	
14	IPCON	Index Pulse Cartridge Not
15	GND.	
16	SPFON	Sector Pulse Fixed Not
17	GND.	
18	SPCON	Sector Pulse Cartridge Not
19	GND.	
20	RDON	READ DATA Not
21	GND.	
22	AL0ON	Address Line 0 Not
23	GND.	
24	AL1ON	Address Line 1 Not
25	GND.	
26	AL2ON	Address Line 2 Not
27	GND.	
28	AL3ON	Address Line 3 Not
29	GND.	
30	AL4ON	Address Line 4 Not
31	GND.	
32	AL5ON	Address Line 5 Not
33	GND.	
34	AL6ON	Address Line 6 Not
35	GND.	
36	AL7ON	Address Line 7 Not
37	GND.	
38	AHOON	Address Line High Not
39	GND.	
40	CSON	Cylinder Select Not
41	GND.	
42	USLON	Unit Select Not
43	GND.	
44	HSON	Head Select Not
45	GND.	
46	CTSON	Control Select Not
47	GND.	
48	STOPO	Stop
49	GND.	
50	WDLON	WRITE DATA Not

CSON	MSON	CTSON
1	0/1	Write Enable
2	2/3	Read Enable
4	-	Seek
8	-	-
16	-	Erase Enable
32	-	Seek (NOT USED)
64	-	Seek-To-Zero
128	-	-
256	-	-

Table 18.1 DRIVE UNIT 0 - INTERFACE CONNECTOR J3

Pin No.	Signal	Function
J4-01	GND.	
02	CONN	Cylinder On Not
03	GND.	
04	URN	Unit Ready Not
05	GND.	
06	USA1N	Unsafe Action 1
07	GND.	
08	USA2N	Unsafe Action 2
09	GND.	
10	AT1N	(Pin 10 is connected but signal AT1N is not used)
11	GND.	
12	IPF1N	Index Pulse Fixed Not
13	GND.	
14	IPC1N	Index Pulse Cartridge Not
15	GND.	
16	SPF1N	Sector Pulse Fixed Not
17	GND.	
18	SPC1N	Sector Pulse Cartridge Not
19	GND.	
20	RD1N	READ DATA Not
21	GND.	
22	AL01N	Address Line 0 Not
23	GND.	
24	AL11N	Address Line 1 Not
25	GND.	
26	AL21N	Address Line 2 Not
27	GND.	
28	AL31N	Address Line 3 Not
29	GND.	
30	AL41N	Address Line 4 Not
31	GND.	
32	AL51N	Address Line 5 Not
33	GND.	
34	AL61N	Address Line 6 Not
35	GND.	
36	AL71N	Address Line 7 Not
37	GND.	
38	AH01N	Address Line High Not
39	GND.	
40	CS1N	Cylinder Select Not
41	GND.	
42	USL1N	Unit Select Not
43	GND.	
44	HS1N	Head Select Not
45	GND.	
46	CTS1N	Control Select Not
47	GND.	
48	STOP1	Stop
49	GND.	
50	WDL1N	WRITE DATA Not

CS1N	MS1N	CTS1N
1	0/1	Write Enable
2	2/3	Read Enable
4	-	Seek
8	-	-
16	-	Erase Enable
32	-	Seek (NOT USED)
64	-	Seek-To-Zero
128	-	-
256	-	-

Table 18.2 DRIVE UNIT 1 - INTERFACE CONNECTOR J4

PIN NUMBER CU	PIN NUMBER DRIVE
1	32
2	29
3	5
4	2
5	37
6	34
7	7
8	3
9	31
10	28
11	38
12	35
13	27
14	24
15	33
16	30
17	26
18	23
19	4
20	1
21	51
22	48
23	50
24	47
25	49
26	46
27	57
28	54
29	56
30	53
31	55
32	52
33	64
34	60
35	63
36	59
37	43
38	40
39	13
40	10
41	39
42	36
43	14
44	11
45	21
46	17
47	62
48	58
49	12
50	8

Table 18.3 CABLE CDDZ - Drive X1215/6:

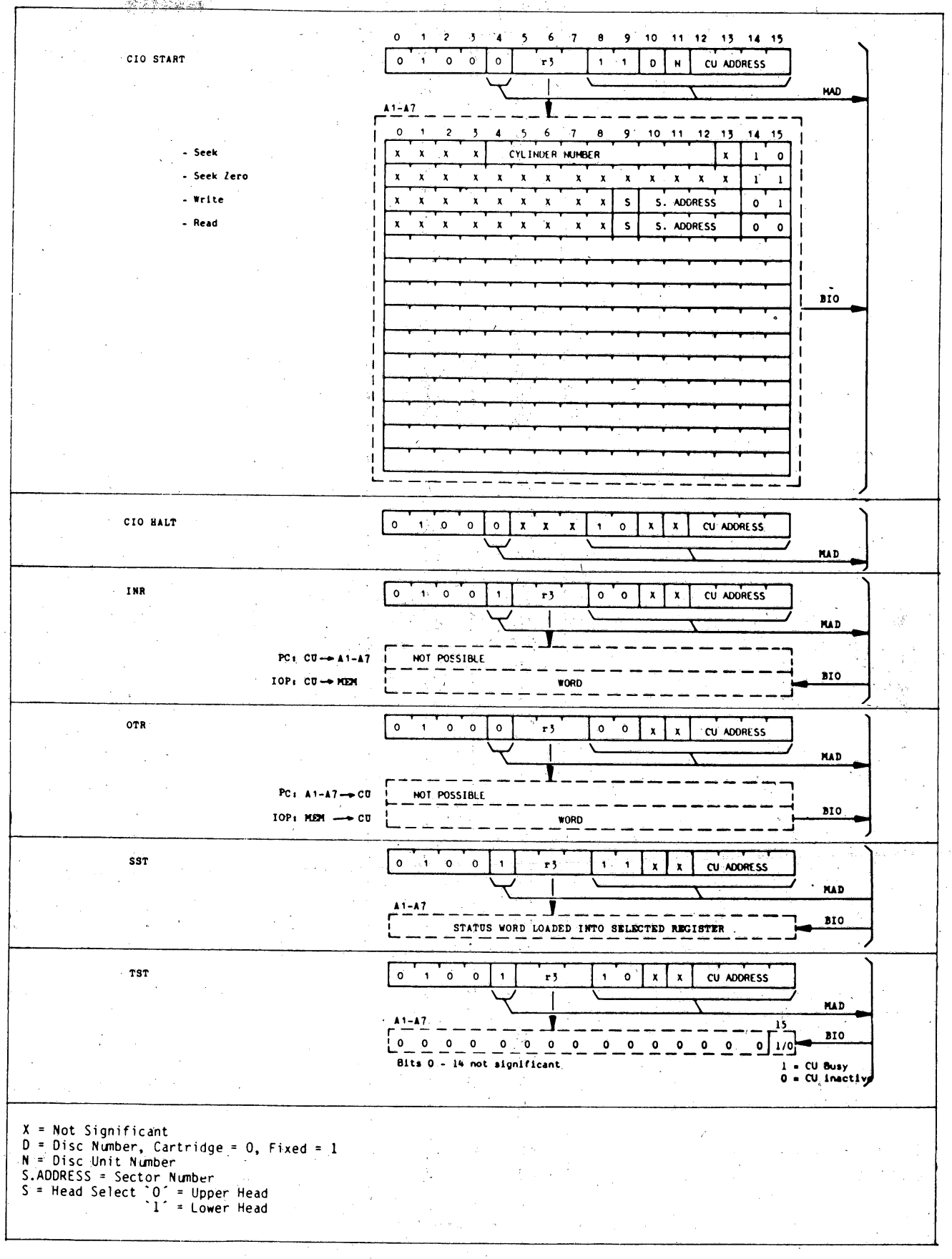
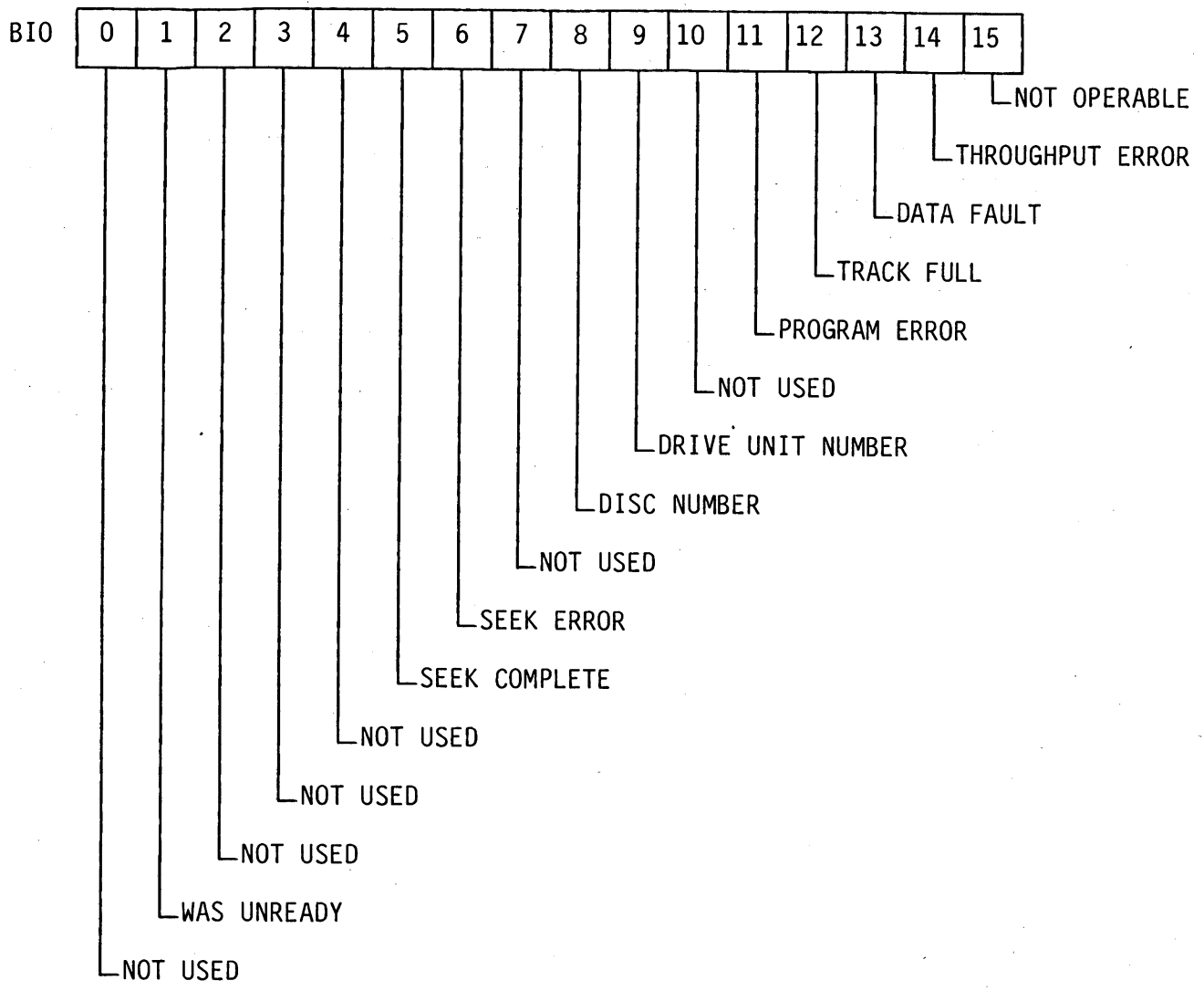


Figure 18.2 INSTRUCTION/COMMAND-WORD FORMATS

18.4.1 STATUS WORD



Bit 15 Not Operable - is set if the drive (indicated in bit 9) is not operable.

Bit 14 Throughput Error - is set during a write operation if both words in the Input Data Buffer have been written to disk and serialization of the current word is completed before the IOP has answered the exchange data request with an OTR. It is set during a read operation if neither word in the Read Data Buffer have been transferred to memory and deserialization of the current word has ended before the IOP has answered the exchange data request with an INR.

Bit 13 Data Fault - is set when the LRC check fails at the end of a read operation.

Bit 12 Track Full - is set after a read or write command if the sector given inside the command is reached again after one revolution, without signal end of transfer from the IOP.

Bit 11 Program Error - is set if the CU receives an OTR command during a read operation or an INR during a write operation.

Bit 9 Drive Unit Number - is set for drive number 1.

Bit 8 Disk Number - is set for the fixed disk. The disk number is valid only after a read or write operation, after a seek or ready interrupt bit 8 will always be zero.

Bit 6 Seek Error - is set if an error has been detected or the drive becomes inoperable during a seek operation.

Bit 5 Seek Complete - is set if the seek operation is complete whether or not errors were detected.

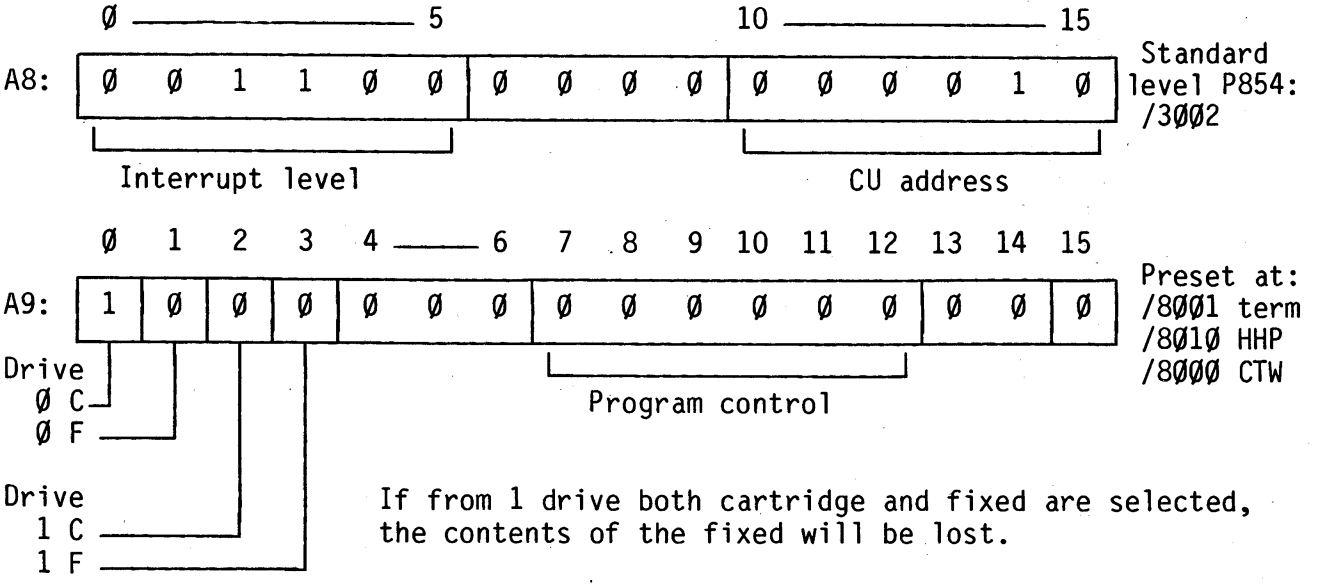
Bit 1 Was Unready - is set if during scanning a change of status has occured from not operable, to operable.

18.5 SHORT DESCRIPTION TEST-PROGRAM

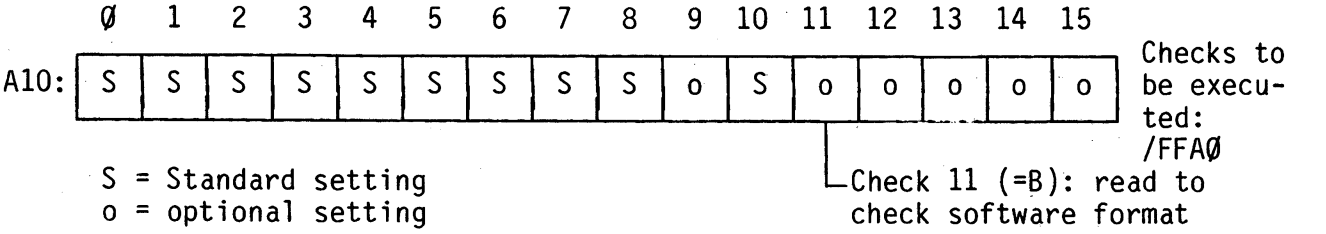
TESTPROGRAM BZCDD1 8K for P824-012 (2,7Mb)
BZ1216 for P824-014 (5,4Mb)

Procedure:

- IPL
  Program displays /7ØØ (= restart point and normal end)
  Rwitch on RTC (PF/AR also possible)
- ==== Load Scratch Cartridge! ====



C = Cartridge
F = Fixed



Error stop at /5FØ
Interrupts return to /7ØØ
Information stop at /5EØ

For more information see official description of testprogram.

BZCDD1 and BZ1216 - tested

Checks Ø through B
These times are only given as an identification and can vary according to the CPU and memory type.

CHECK	DURATION FOR ONE DISC	STANDARD	
CHKØØ	3 mn	Yes	Saving fixed disc on mobile disc (Software format)
CHKØ1	5 s	Yes	Test of controller status
CHKØ2	20 s	Yes	Seek test with timing check
CHKØ3	40 s	Yes	Write and read test on one cylinder
CHKØ4	2 mn	Yes	Write and read test of all disc sector
CHKØ5	1 s	Yes	Read all sector track Ø with chaining command
CHKØ6	1 s	Yes	Write all sector track Ø with chaining command
CHKØ7	1 mn	Yes	Read test of all disc sectors (compatibility test)
CHKØ8	1 mn	Yes	Seek test - checking the identifier
CHKØ9		No	Seek error - not operable and head selection test
CHKØA	3 mn	Yes	Restituting fixed disc
CHKØB	1 mn	No	Read to check one disc (Software format)

Service Routine
It permits seeks, writes or reads to be executed. It starts in /2ØØØ after having initialized some registers. See official testprogram description.

Procedure 5111 991 11341 = Procedure BZ1216 5111 991 11Ø32
with addendum PTS8ØØØ 5111 991 11381
Listing 5111 991 11251
Program 5111 199 62481

18.6 SHORT ROUTINES

```
          DATE  80-03-13        IDENT    SEEK

00000                           IDENT    SEEK
00001                  * PROGRAM USABLE INSTEAD OF AN EXERSISER
00002
00003                  *        LOAD START CYLINDER IN REG A1
00004                  *        LOAD LAST CYLINDER IN REG A2
00005                  *        LOAD STEPPING INCREMENT IN REG A3
00006                  *        LOAD TIME DELAY IN REG A6
00007                  *        DISC DRIVE 0 IS ADDRESSED  OTHERWISE CHAGE DEVICE ADDRESSES
00008
00009                           AORG     /80
00010  0080  FFFF               DATA     /FFFF
00011  0082  0000               DATA     0
00012  0084  207F       START   HLT
00013  0086  20BF               INH
00014  0088  8404       CIO     LDR      A4,A1
00015  008A  3C43       CIO1    SLL      A4,3
00016  008C  1402               ADK      A4,2
00017  008E  44C2               CIO      A4,1,2
00018  0090  4DC2               SST      A5,2
00019  0092  5C04               RB(4)    *-2
00020  0094  E718               ECR      A7,A6
00021  0096  1F01               SUK      A7,1
00022  0098  5E04               RB(6)    *-2
00023  009A  ED20               CWK      A5,/400
       009C  0400
00024  009E  5002               RF(0)    CONT
00025  00A0  207F               HLT                              STATUS ERROR SEE A5
00026  00A2  3C63       CONT    SRL      A4,3
00027  00A4  940C               ADR      A4,A3
00028  00A6  EC08               CWR      A4,A2
00029  00A8  5922               RB(1)    CIO
00030  00AA  5F22               RB       CIO1
00031
00032                           EJECT
00033                  *EXAMPLE
00034                  *FOR CERTAIN ADJUSTMENTS SEEK FROM 0 TO 64 IN LOOP
00035                  *LOAD THE REGISTERS AS FOLLOWS:
00036                  *        LOAD A1 WITH 0
00037                  *        LOAD A2 WITH 64 DEC = /40
00038                  *        LOAD A3 WITH 64 DEC = /40
00039                  *        LOAD A6 WITH  /40 ( MAX VALUE IN A6 = /80)
00040                  *                 (/40= 64 DEC IS ABOUT A DELAY OF 64 MSEC)
00041
00042                  *        LOAD START ADDRESS IN A0
00043                  *        PUSH  MC AND RUN
00044
00045                  *NOTE    WITH INST YOU CAN STOP THE PROGRAM AND IT IS
00046                  *        POSSIBLE TO CHANGE THE PARAMETERS, PUSH RUN AND
00047                  *        THE PROGRAM WILL RUN FOR THE CHANGED PARAMETERS
00048
00049                           END      START
```

```
00000                          IDENT    DISCTS                FOR P800
00001                    *PROGRAM FOR READING AND WRITING ON DISC
00002                    *PUT THE PATTERN YOU WANT READ AND WRITE IN A5, BEFORE RUNNING THE PROGRAM
00003                    *IF THE PROGRAM STOPS YOU FIND THE WRITTEN WORD IN A3 AND THE READ WORD IN A4
00004                    *IN A2 IS THE POSITION OF THE WORDS IN THE DATA BUFFERS
00005                    *AFTERWARDS YOU FIND THE STATUS IN A6.
00006                    *
00007                    *
00008                          AORG     /80
00009          0002      DA    EQU      /02                   DEVICE ADDR. DISC
00010          0004      ER1   EQU      /04                   FIRST EXTERNAL REGISTER
00011          0005      ER2   EQU      /05                   SECOND EXTERNAL REGISTER
00012                    *
00013                    *MAIN PROGRAM
00014   0080   FFFF           DATA     /FFFF
00015   0082   0000           DATA     0
00016   0084   207F      START HLT
00017   0086   87A0           LDKL     A15,EOS               LOAD STACKPOINTER
        0088   0780
00018   008A   8120           LDKL     A1,INTROU             ADDR. INTERRUPTROUTINE
        008C   00F4
00019   008E   8141           ST       A1,/20
        0090   0020
00020   0092   0200      LOAD  LDK      A2,0
00021   0094   8549      STORE ST       A5,DATAIN,A2          WRITE BUFFER
        0096   00FA
00022   0098   1202           ADK      A2,2
00023   009A   EA20           CWK      A2,/19A
        009C   019A
00024   009E   5C0C           RB(4)    STORE
00025   00A0   8120           LDKL     A1,/C0CD              WER CONTROL WORD 1
        00A2   C0CD
00026   00A4   7104           WER      A1,ER1
00027   00A6   8120           LDKL     A1,DATAIN             WER CONTROL WORD 2
        00A8   00FA
00028   00AA   7105           WER      A1,ER2
00029   00AC   0101           LDK      A1,1
00030   00AE   41C2           CIO      A1,1,DA               START WRITE
00031   00B0   5C04           RB(4)    *-2
00032   00B2   4F82      WAIT TST      A7,DA
00033   00B4   EF20           CWK      A7,0
        00B6   0000
00034   00B8   5C08           RB(4)    WAIT
00035   00BA   8120           LDKL     A1,/80CD              WER CONTROL WORD 1
        00BC   80CD
00036   00BE   7104           WER      A1,ER1
00037   00C0   8120           LDKL     A1,DATAOT             WER CONTROL WORD 2
        00C2   043A
00038   00C4   7105           WER      A1,ER2
00039   00C6   0100           LDK      A1,0
00040   00C8   41C2           CIO      A1,1,DA               START READ
00041   00CA   5C04           RB(4)    *-2
00042   00CC   4F82      WAITAG TST    A7,DA
00043   00CE   EF20           CWK      A7,0
        00D0   0000
00044   00D2   5C08           RB(4)    WAITAG
00045   00D4   0200           LDK      A2,0
00046   00D6   8348      TEST  LD       A3,DATAIN,A2          COMPARE WRITE AND
        00D8   00FA
00047   00DA   8448           LD       A4,DATAOT,A2          READ BUFFER
        00DC   043A
00048   00DE   EB10           CWR      A3,A4                 OK?
00049   00E0   540C           RF(4)    HALT                  NO STOP
00050   00E2   1202           ADK      A2,2                  YES GO ON
00051   00E4   EA20           CWK      A2,/19A
        00E6   019A
00052   00E8   5C14           RB(4)    TEST
00053   00EA   8F20           ABL(7)   LOAD
        00EC   0092
00054   00EE   207F      HALT  HLT                            DATA ERROR
00055   00F0   8F20           ABL(7)   LOAD
        00F2   0092
00056                    *
00057                    *INTERRUPT ROUTINE
00058   00F4   4EC2      INTROU SST     A6,DA                 AFTERWARDS STATUS IN A6
00059   00F6   5C04           RB(4)    *-2
00060   00F8   F03E           RTN      A15
00061   00FA           DATAIN RES      /1A0
00062   043A           DATAOT RES      /1A0
00063   077A           STACK  RES      3
00064   0780           EOS    RES      1
00065                          END      START
```

```
        DATE  80-03-13          IDENT    DKPROG

00000                           IDENT    DKPROG
00001
00002                   *       THIS PROGRAM TESTS READING AND WRITING ON DISC IN
00003                   *       PROGRAMMED CHANNEL
00004
00005                   ****************TAKE OFF BREAKLINE*****************
00006
00007
00008                   *       LOAD WORD TO WRITE IN REGISTER A2
00009                   *       LOAD START ADDRESS (/0086) IN A0 AND PUSH RUN
00010
00011                           AORG     /80
00012
00013  0080  FFFF               DATA     /FFFF
00014  0082  0000               DATA     0
00015                   *       WRITE ROUTINE
00016
00017  0084  207F       START   HLT
00018  0086  20BF               INH
00019  0088  0101               LDK      A1,1                WRITE COMMAND ON SECTOR ZERO
00020  008A  41C2               CIO      A1,1,2              START CONTROLLER
00021  008C  4202               OTR      A2,0,2              WRITE A2 CONTENTS ON DISC
00022  008E  5C04               RB(4)    *-2
00023  0090  4182               CIO      A1,0,2              STOP CONTROLLER
00024  0092  4CC2               SST      A4,2                GET STATUS
00025  0094  5C04               RB(4)    *-2
00026  0096  207F               HLT                          CHECK STATUS IN A4
00027                   *                                    SOMETIMES THROUGHPUT ERROR IS GIVEN
00028                   *                                    BECAUSE CIO HALT WAS JUST TO LATE
00029
00030
00031                   *       READ ROUTINE
00032  0098  20BF               INH
00033  009A  0100               LDK      A1,0                READ COMMAND ON SECTOR ZERO
00034  009C  41C2               CIO      A1,1,2              START CONTROLLER
00035  009E  4B02               INR      A3,0,2              READ WORD
00036  00A0  5C04               RB(4)    *-2
00037  00A2  4182               CIO      A1,0,2              STOP CONTROLLER
00038  00A4  4CC2               SST      A4,2                GET STATUS
00039  00A6  5C04               RB(4)    *-2
00040  00A8  207F               HLT                          STATUS IN A4
00041                                                        READ WORD IN A3
00042  00AA  5F28               RB       START
00043
00044
00045                           END      START
```

19 MAGNETIC TAPE CONTROL UNIT P831-060 (MTCU)

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19.1 MAGNETIC TAPE CONTROL UNIT - IDENTIFICATIONS

Type Number : P-831-060 (MTCU)
Testprogram : BMAGT2
Channel : Hardware Channel (IOP, MIOP, IOPZR)
Break Connection 3A41
Devices :

FORMATTER:

P831-010 - F849-20/13.9
P831-020 - F849-36/25.02
P831-030 - F649-60.30.5/1600

DRIVES:

P-831-002 - 6840/9/25 ips, NRZ
P-831-004 - 6840/9/45 ips, NRZ
P-831-006 - 6640/9/37.5 ips, PE

It is possible to use the units Pertec 8000 and 7000, but they are not mentioned in the catalogue.

Power Consumption: 5 Volt, 2.7 Amp.

12NC number on the sticker on the baord:

MTCU: 5111 199 7246x (5322 216 25214)

19.2 INSTALLATION DETAILS

See Chapter 13 for connection of MTCU to P854 systems.

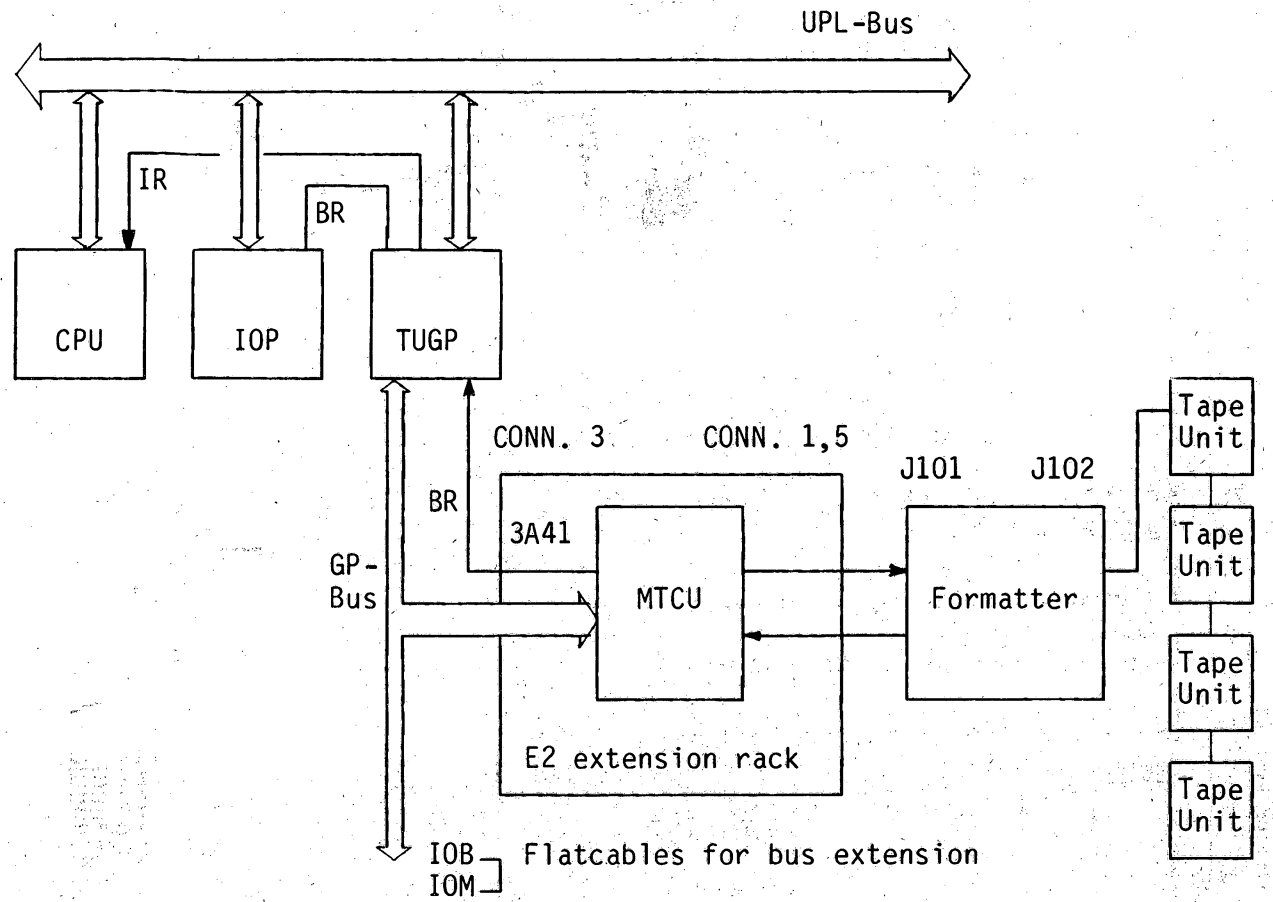


Figure 19.1 MAGNETIC TAPE CONTROL UNIT - SYSTEM CONFIGURATION

Configuration Description

The minimum configuration is:

- A basic cabinet plus Power supply with:
  . UPL CPU
  . Memory
  . IOP
  . TUGP
- An E2 extension cabinet with a Magnetic Tape Control unit.
- Magnetic Tape Peripheral(s) and Formatter.
- GP Bus cables (IOB and IOM), Break cable for E2 rack, GP Bus terminator.

Note: Selection switch, on NRZI- or PE-Write Cards in Formatter, must always be on position "0".

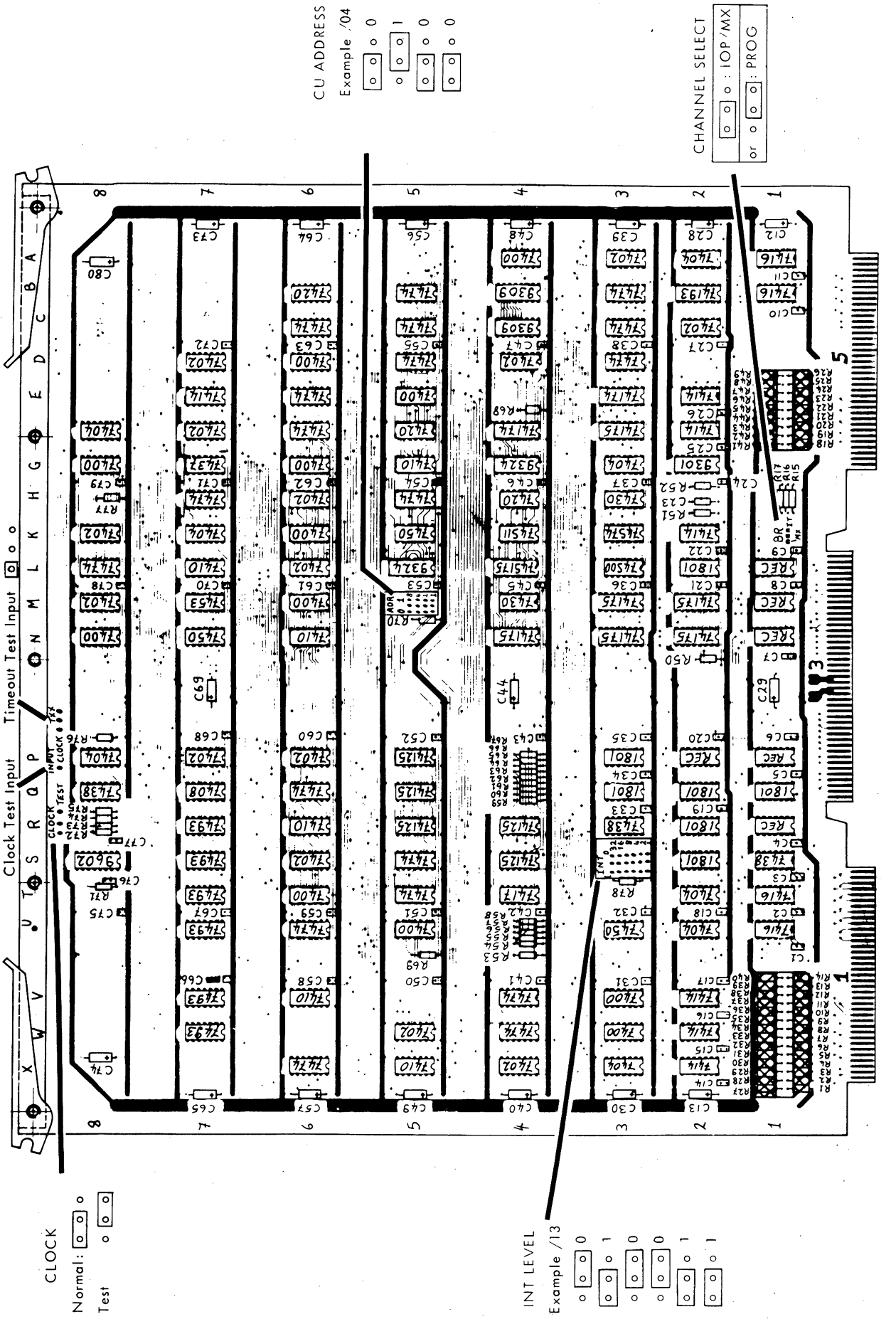


Figure 19.2 CARD LAYOUT

19.3 INTERFACE CONNECTIONS

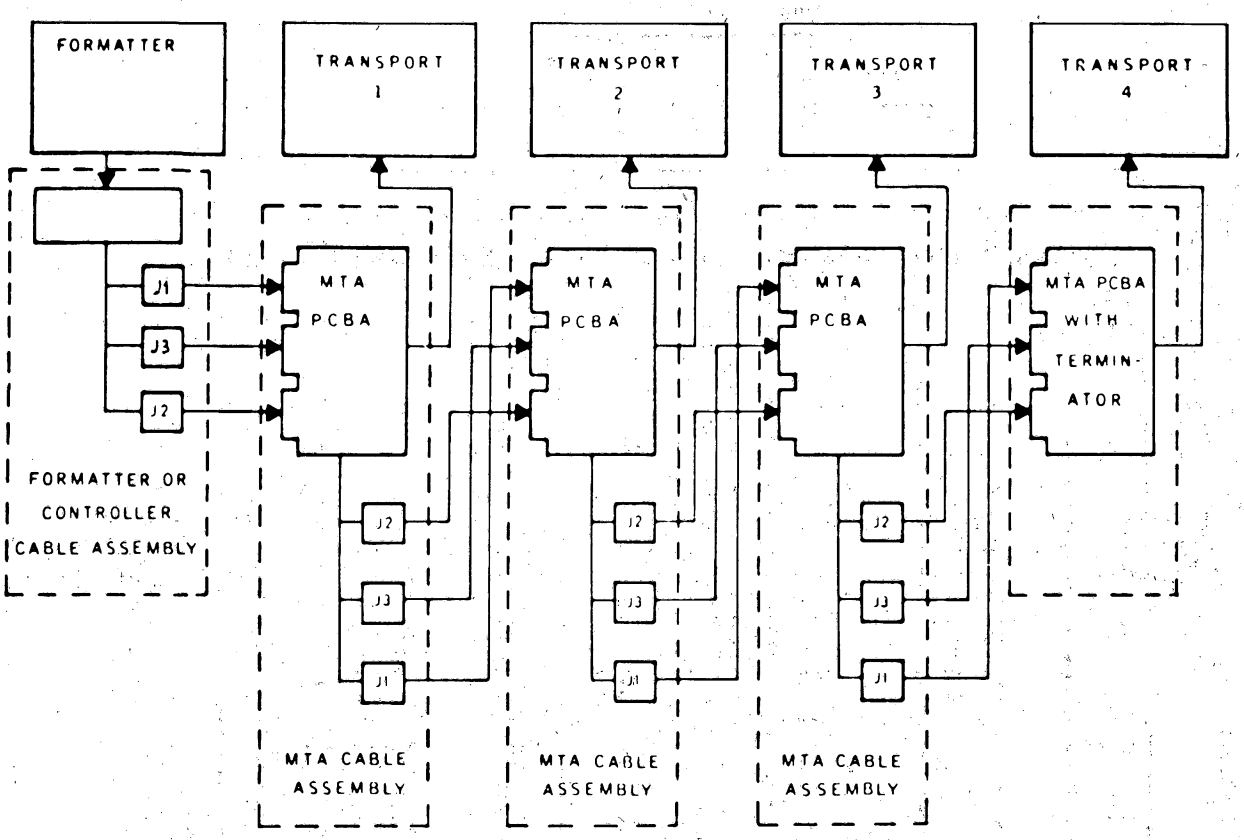


Figure 19.3 MTA SYSTEM DIAGRAM

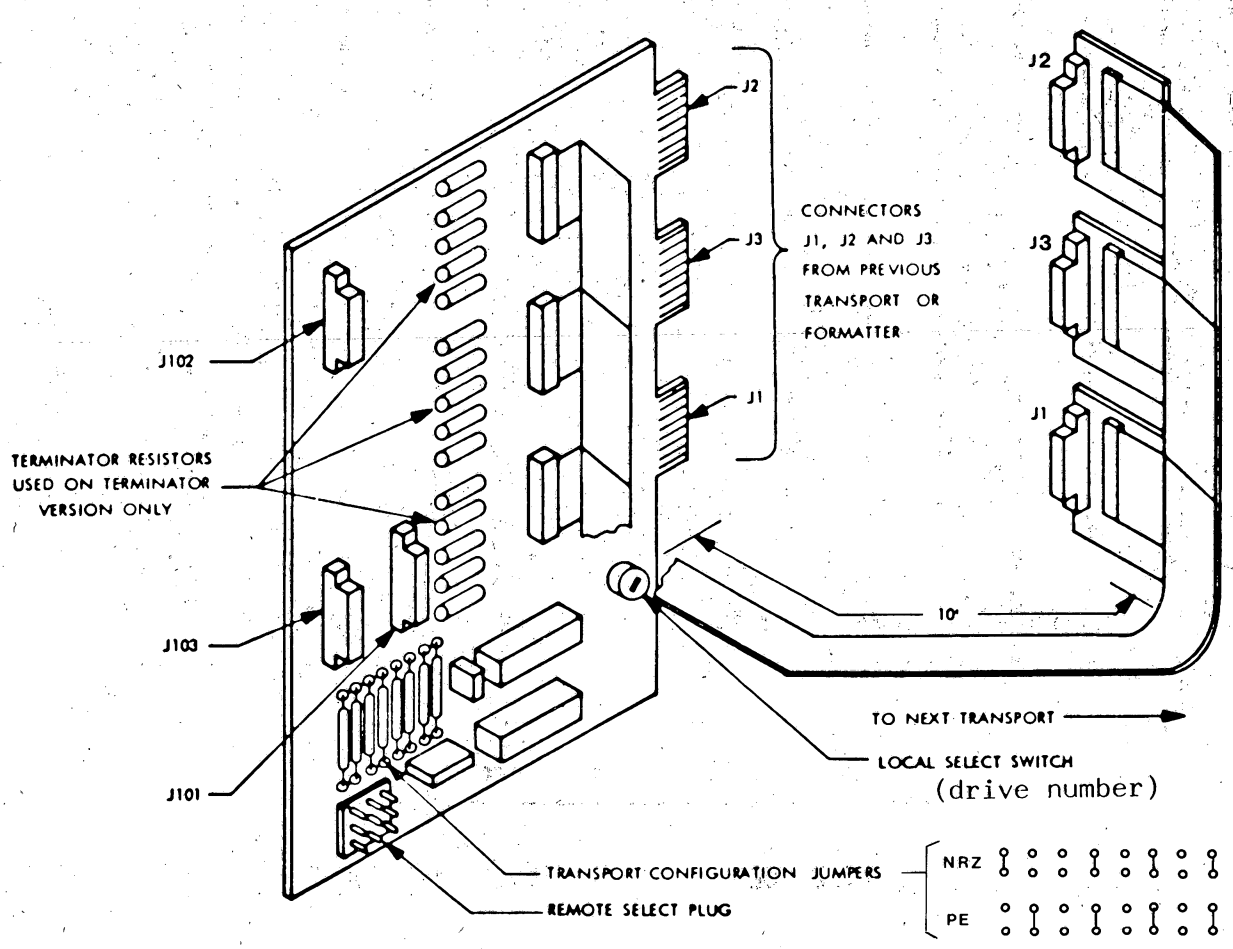


Figure 19.4 MTA CABLE ASSEMBLY

Formatter mating connector: 2VH50 - 1JV5
Controller mating connector

CU Connector 1		Signal	Formatter Card Connector J101		
Live Pin	Ground Pin		Live Pin	Ground Pin	
1301	1B03	IFPTN ←	A28	A29	file protected
A01	A03	IONLN ←	A27	A26	on line
A02	A03	IRDYN ←	B27	B26	ready
B02	B03	INRZN ←	A31	A32	NRZ drive
B04	B05	IFBYN ←	B22	B23	formatter busy
B06	B07	ICERN ←	B25	B26	corrected error (only PE)
B08	B09	IHERN ←	A24	A23	hard error
B10	B11	IFMKN ←	A25	A26	file mark read
B12	B13	IRSTRN ←	B36	B35	read strobe
A05	A04	IDBYN ←	A22	A23	Data busy
NRZ:checkchar's A07	A06	ICCGIDTN ←	B24	B23	PE: identification burst
A09	A08	IEOTN ←	A30	A29	end of tape
A11	A10	ILDPN ←	B30	B29	load point
A13	A12	IWSTRN ←	A34	A35	write strobe
B25	B26	IGON →	A03	A02	go
A27	A26	ILOLN →	A10	B15	load on line command
B28	B29	IOFLN →	A12	A11	off-line command
A29	A28	IREWN →	B12	B11	rewind command
B30	B31	IERASEN →	B07	B08	erase command
A31	A30	IREVN →	B04	B05	reverse/forwards
B32	B33	IWFMN →	B06	B05	write file mark comm.
A33	A32	IWRTN →	A04	A05	write/read
B34	B35	IPARN →	B10	B11	parity
A35	A34	IDENTN →	A09	A08	write identif. burst
B36	B37	ILWDN →	B13	B14	last word
A37	A36	IFEN →	A13	A14	formatter enable

Table 19.1 DEVICE INTERFACE, CONNECTOR 1

CU Connector 5		Signal	Formatter Card Connector J101		
Live Pin	Ground Pin		Live Pin	Ground Pin	
5A33	5A34	ITAD1N →	B03	B02	transport address
B34	B33	ITAD0N →	A01	A02	
B32	B31	IW7N →	A21	A20	write data lines
A31	A32	IW6N →	B21	B20	
B30	B29	IW5N →	A19	A20	
A29	A30	IW4N →	B19	B20	
B28	B27	IW3N →	A18	A17	
A27	A28	IW2N →	B18	B17	
B26	B25	IW1N →	A16	A17	
A25	A26	IW0N →	B16	B17	
B13	B12	IR8N ←	A36	A35	read data lines
A12	A13	IR7N ←	A42	A41	
B11	B10	IR6N ←	B42	B41	
A10	A11	IR5N ←	A40	A41	
B09	B08	IR4N ←	B40	B41	
A08	A09	IR3N ←	A39	A38	
B07	B06	IR2N ←	B39	B38	
A06	A07	IR1N ←	A37	A38	
B05	B04	IR0N ←	B37	B38	

Table 19.2 DEVICE INTERFACE, CONNECTOR 5

Transport J103 Live	Transport J103 Ret		MTA II J3* Live	MTA II J3* Ret		Formatter J102 Live	Formatter J102 Ret	Signal
1	A	→	1	A	→	B1	B2	READ DATA PARITY (IRDP)
2	B	→	2	B	→	A1	A2	READ DATA STROBE (IRDS)**
3	C	→	3	C	→	B3	B2	READ DATA 0 (IRD0)
4	D	→	4	D	→	A3	A2	READ DATA 1 (IRD1)
8	J	→	8	J	→	A6	A5	READ DATA 2 (IRD2)
9	K	→	9	K	→	B7	A8	READ DATA 3 (IRD3)
10	L	→	10	L	→	A7	A8	NRZI (INRZ)
11	M	→	11	M	→	B9	B8	7-, 9-TRACK (I7TR/I9TR)**
12	N	→	12	N	→	A9	A8	SINGLE (ISGL)
13	P	→	13	P	→	B10	B11	SPEED (ISPD)
14	R	→	14	R	→	A10	A11	READ DATA 4 (IRD4)
15	S	→	15	S	→	B12	B11	READ DATA 5 (IRD5)
17	U	→	17	U	→	B13	B14	READ DATA 6 (IRD6)
18	V	→	18	V	→	A13	A14	READ DATA 7 (IRD7)

Note: The following pins provide +5v and ground from the Formatter to the MTA assemblies.

			5	E	←	A48	B48	
			6	F	←	A49	B49	
			7	H	←	A50	B50	

*Read signals applied to J3 are also applied in parallel to J10 for application to other MTA II PCBAs in the daisy-chain. Refer to Schematic No. 103914.

**Relevant to NRZI Operation Only.

Table 19.3 READ SIGNALS, TRANSPORT TO FORMATTER VIA MTA II

Formatter J102 Live	Formatter J102 Ret		MTA II J2* Live	MTA II J2* Ret		Transport J102 Live	Transport J102 Ret	Signal
B15	B14	→	A	1	→	A	1	WRITE DATA STROBE (IWDS)
B16	B17	→	C	3	→	C	3	WRITE AMPLIFIER RESET (IWARS)
B18	B17	→	E	5	→	E	5	READ THRESHOLD 1 (IRTH1)
A18	A17	→	F	6	→	F	6	READ THRESHOLD 2 (IRTH1)
A21	A20	→	L	10	→	L	10	WRITE DATA PARITY (IWDP)
B22	B23	→	M	11	→	M	11	WRITE DATA 0 (IWD0)
A22	A23	→	N	12	→	N	12	WRITE DATA 1 (IWD1)
B24	B23	→	P	13	→	P	13	WRITE DATA 2 (IWD2)
A24	A23	→	R	14	→	R	14	WRITE DATA 3 (IWD3)
B25	B26	→	S	15	→	S	15	WRITE DATA 4 (IWD4)
A25	A26	→	T	16	→	T	16	WRITE DATA 5 (IWD5)
B26	B26	→	U	17	→	U	17	WRITE DATA 6 (IWD6)
A27	A26	→	V	18	→	V	18	WRITE DATA 7 (IWD7)
						J101		
A42	A41	→	B	2	→	J	2	SELECT 1 (ISLT1)**
B43	B44	→	D	4	→	J	16	SELECT 2 (ISLT2)**
A43	A44	→	H	7	→	J	17	SELECT 3 (ISLT3)**

*Write signals applied to J2 are also applied in parallel to J12 for application to other MTA II PCBAs in the daisy-chain. Refer to Schematic No. 103914.

**Provided through Select Switch

Table 19.4 WRITE SIGNALS, FORMATTER TO TRANSPORT VIA MTA II

Formatter J102 Live	Formatter J102 Ret		MTA II J1* Live	MTA II J1* Ret		Transport J101 Live	Transport J101 Ret	Signal
A28	A29	→	B	2	→	B	2	OVERWRITE (IOVW)
B30	B29	→	C	3	→	C	3	SYNCHRONOUS FORWARD Command (ISFC)
A30	A29	→	D	4	→	D	4	DATA DENSITY SELECT (IDDS)**
B31	B32	→	E	5	→	E	5	SYNCHRONOUS REVERSE Command (ISRC)
A31	A32	←	F	6	←	F	6	DATA DENSITY INDICATOR (IDDI)*
B33	B32	→	H	7	→	H	7	REWIND Command (IRWC)
B34	B35	→	K	9	→	K	9	SET WRITE STATUS (ISWS)
A34	A35	→	L	10	→	L	10	OFF-LINE Command (IOFC)/REWIND UNLOAD (IRWU)***
B36	B35	←	M	11	←	M	11	ON-LINE (IONL)
A36	A35	←	N	12	←	N	12	REWIND (IRWD)
B37	B38	←	P	13	←	P	13	FILE PROTECT (IFPT)
A37	A38	←	R	14	←	R	14	LOAD POINT (ILDP)
A39	A38	←	T	16	←	T	16	READY (IRDY)
B40	B41	←	U	17	←	U	17	END OF TAPE (IEOT)
B42	B41	→	J	8	→	J	8	SELECT 0 (ISLT0)****

*Control signals applied to J1 are also applied in parallel to J11 for application to other MTA II PCBAs in the daisy-chain. Refer to Schematic No. 103914.

**Relevant to NRZI Operation Only.

***REWIND UNLOAD operation applies to T9000 series transports only.

****Provided through Select Switch.

Table 19.5 CONTROL SIGNALS, TRANSPORT/MTA II/FORMATTER

19.4 HARDWARE-SOFTWARE INTERFACE DETAILS

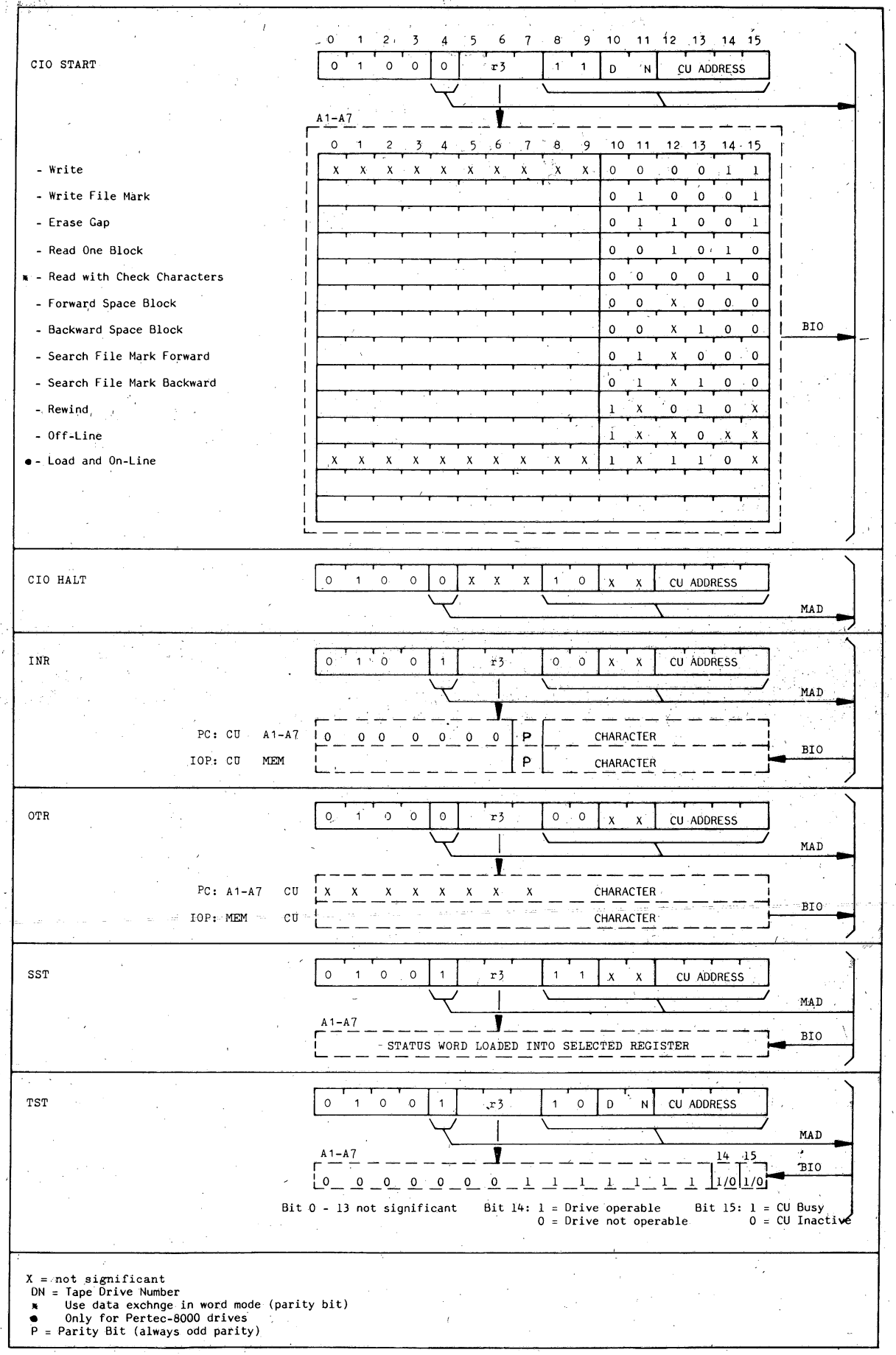
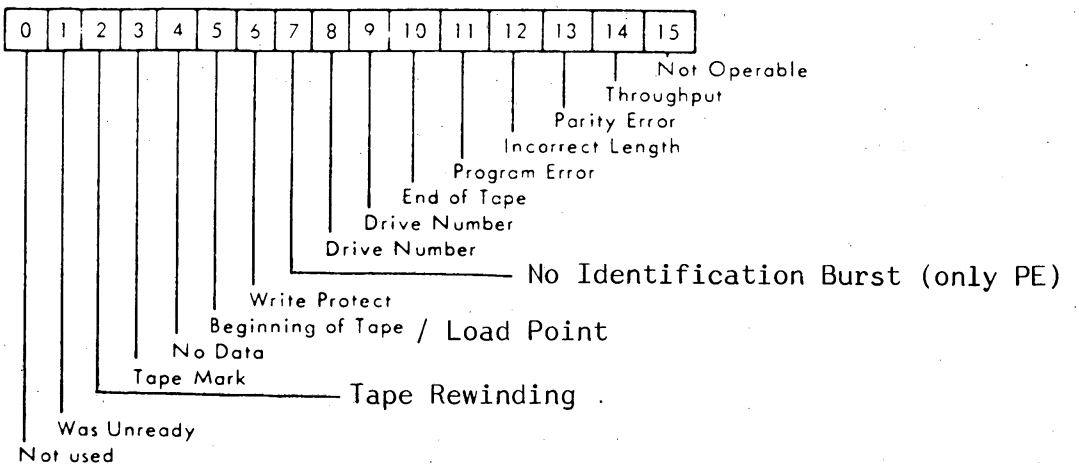


Figure 19.5 INSTRUCTION / COMMAND-WORD FORMATS

19.4.1 STATUS WORD



--15 Not Operable is set if the transport or formatter are not ready to receive a command. Some possible couses of this status are:

- Interlocks are not made
- Initial load is not complete
- The transport is not on line
- The formatter power is off

--14 Throughtput Error is set during Read or Write commands if the channel does not respond to a data request (BR) within the allowed time. The THRF flip-flop (logic f) is set if the data strobe (WSTR/RSTR) for a new character is received from the formatter while the CU is still in Exchange state to transfer the previous character.

--13 Data Fault is set during a Read, Write or Search command if a read error is detected by the formatter for any of the following reasons:

NRZI Mode
- Vertical parity error on data character
- Longitudinal parity error
- CRC parity error (detected during read forward commands only)

PE Mode
- False preamble detection
- False postamble detected
- Buffer overflow
- Multichannel dropout (with WRITE also single channel dropout)
- Parity error without associated channel dropout

--12 The Incorrect Length is set during a Read command with data transfer if the block length on the tape is different from the specified block length.

--11 Program Error

- An INR command is received from the channel during a Write data operation:
- An OTR command is received from the channel during a Read data operation:
- An invalid command code is received on BIO10-15 during a CIO-Start command:

BIOF	10	11	12	13	14	15	
	0	-	1	1	1	1	
	0	0	-	-	0	1	INVALID CODES
	0	-	-	1	-	1	
	0	1	-	-	1	-	
	0	-	-	1	1	1	

--10 End of Tape is set if the EOT mark is detected during any CIO-Start command in the forward direction.
If the EOTF is set during a forward Search File Mark command, the HALTF flip-flop is set and the operation stops.

--8,9 Tape Unit Address indicate the current tape transport address.

MAD TADF Status BIO	10-11 1-0 8-9	Tape Unit
	0 0	0
	0 1	1
	1 0	2
	1 1	3

--7 No Identification Burst is set if the identification burst is not detected during a forward command from the load point on a phase-encoded transport.

--6 File Protected/Write Unable is set whenever the CU receives a Write, Write File Mark or Erase Gap command for a transport that is file protected.

--5 Load Point is set if the transport is at load point when any backward command is received.
(Search or Space backward, Rewind, Load-and-On-Line).

--4 No Data if no data is detected within 20 seconds after sending the command to the transport. Note: No Data, ais also set if blocks are written or read, which are longer than 20 seconds in time.

--3 File Mark is set if a File Mark is detected during any Read, Space, Block or Search File Mark command.

- For NRZI-tapes, if an error is detected in the first character, and this character is followed by one other character only, the CU terminates the operation at the end of the first block, and sets bit 3 (File Mark) and bit 13 (Data Fault).

--2 Tape Rewinding. This status bit is set if the selected tape transport is executing a Rewind command.

--1 Tape was Not Ready is set when the tape transport changes from not-ready state of the completion of a Rewind operation or when an in-operable unit becomes operable.

19.5 SHORT DESCRIPTION TESTPROGRAM

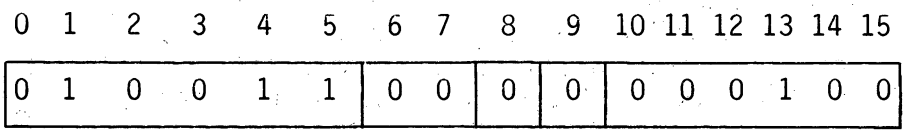
TESTPROGRAM BMAGT2 8K

1. IPL
   The program stops at /700 (restart address and normal end).

2. Switch on RTC (PF/AR also possible).

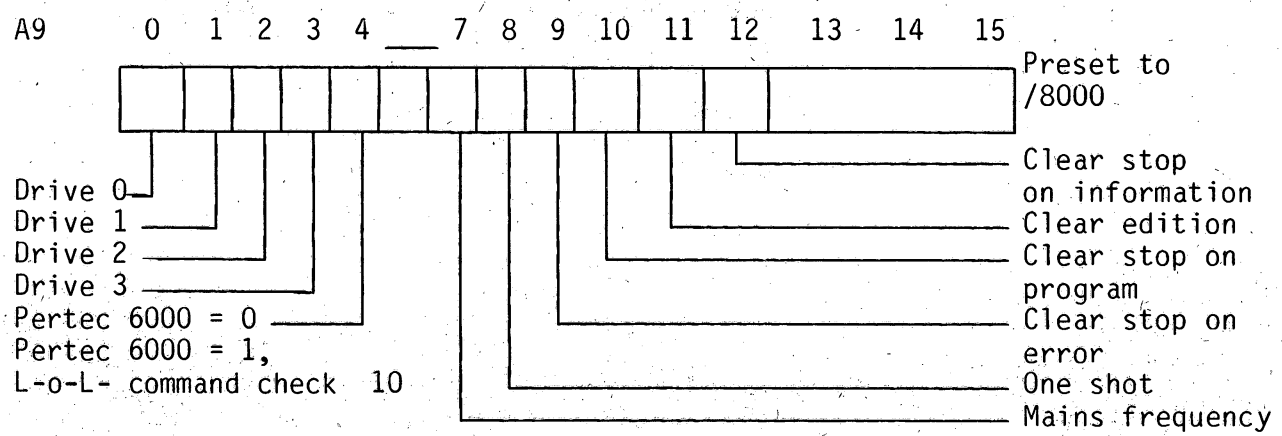
3.

A8

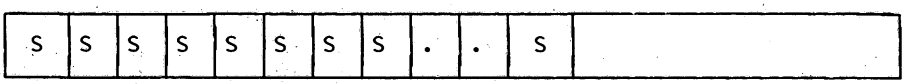


Standard levels:
P854: /4C04
CU-A: /04
Int. Level: /13

A9

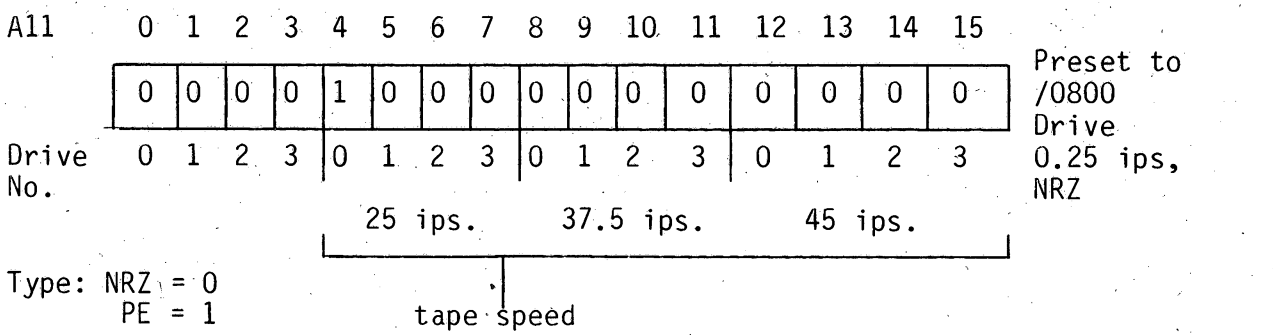


A10



S = Standard setting
. = Optional setting

A11



4. Depress MC, RUN

   Error stop at /5F0
   Restart after power-off at /6EA
   Interrupts return to /700
   Information stop at /5E0

For more information see official description of the testprogram.

BMAGT2 tested:

```
If ØØØØ  check Ø  : Controller Test 1st part
If ØØØ1  check 1  : Controller Test 2nd part
If ØØØ2  check 2  : Status bit test
If ØØØ3  check 3  : Write test with various lengths and patterns
If ØØØ4  check 4  : Reads and controls data written in check 3
If ØØØ5  check 5  : Space block Test
If ØØØ6  check 6  : File Mark (FM) Test
If ØØØ7  check 7  : Erase Function Test
If ØØØ8  check 8  : Status Test with operator action
                    (Write Unable; off line: not operable)
If ØØØ9  check 9  : End of tape test (status bit)
If ØØØA  check A
```

Procedure 5111 991 11351 = Procedure BMAGT2 5111 991 Ø8654
with addendum PTS8ØØØ 5111 991 11381

Listing 5111 991 11261
Program 5111 199 62471

19.6 SHORT ROUTINES

```
          DATE  80-03-13        IDENT    WRITE


00000                           IDENT    WRITE
00001                    *
00002                    *
00003          0000      BEGIN    EQU      *
00004                           RORG     BEGIN+/80
00005                    *
00006                    *
00007                    *       LOAD THE TEST PATTERN IN REGISTER A8
00008                    *
00009                    *       LOAD THE WER PARAMETERS FOR THE WRITE ROUTINE IN REGISTER A7
00010                    *
00011  0080  FFFF                DATA     /FFFF
00012  0082  0000                DATA     0
00013  0084  207F       START    HLT
00014  0086  20BF                INH
00015                    *
00016                    *       THIS ROUTINE LOADS THE OUTPUT BUFFER WITH THE TEST PATTERN
00017                    *
00018  0088  8620                LDKL     A6,WRTBUF            LOAD THE BUFFER ADDRESS IN A6
       008A  00B6  R
00019  008C  80B9       STPAT    STR      A8,A6                STORE TEST PATTERN
00020  008E  1602                ADK      A6,2                 UPDATE BUFFER ADDRESS AND
00021  0090  EE20                CWK      A6,/121A             COMPARE FOR BUFFER FULL
       0092  121A
00022  0094  5C0A                RB(NE)   STPAT                IF NOT FULL CONTINUE LOADING
00023                    *
00024                    *       THIS ROUTINE WRITES BLOCKS OF DATA ON TAPE
00025                    *
00026  0096  7708       WRITE1   WER      A7,/8                SEND WRITE CODE TO IOP
00027  0098  8620                LDKL     A6,WRTBUF            LOAD BUFFER ADDRESS AND
       009A  00B6  R
00028  009C  7609                WER      A6,/9                SEND TO IOP
00029  009E  0603       WRITE2   LDK      A6,3                 LOAD WRITE A BLOCK COMMAND
00030  00A0  46C4                CIO      A6,1,/4              AND SEND TO MAG TAPE "1"
00031  00A2  5C04                RB(NA)   *-2
00032  00A4  4CC4                SST      A4,/4                GET STATUS AFTER TRANSFER
00033  00A6  5C04                RB(NA)   *-2
00034  00A8  A420                ANKL     A4,/7F3F             SAVE BITS SET
       00AA  7F3F
00035  00AC  EC20                CWK      A4,0                 AND CHECK FOR ANY BITS SET
       00AE  0000
00036  00B0  5002                RF(E)    *+4                  IF NO CONTINUE
00037  00B2  207F                HLT                           IF YES HALT STATUS IN A4
00038  00B4  5F20                RB       WRITE1
00039                    *
00040  00B6              WRTBUF   RES      2050                 WRITE BUFFER
00041                           END      START
```

```
          DATE  80-03-13        IDENT    READ

00000                           IDENT    READ
00001                    *
00002                    *      THIS PROGRAM READS BLOCKS OF DATA FROM TAPE
00003                    *      AND THEN CHECKS IT AGAINST THE EXPECTED PATTERN
00004                    *
00005         C000       BEGIN  EQU      *
00006                           RORG     BEGIN+/80
00007                    *
00008                    *
00009                    *      LOAD THE EXPECTED PATTERN IN REGISTER A10
00010                    *
00011                    *
00012                    *      LOAD THE NUMBER OF CHARACTERS PER BLOCK IN REGISTER A8
00013                    *
00014                    *
00015                    *      LOAD THE WER PARAMETERS FOR A READ COMMAND IN REGISTER A7
00016                    *
00017                    *
00018  0080  FFFF                DATA     /FFFF
00019  0082  0000                DATA     0
00020  0084  207F       START    HLT
00021  0086  20BF                INH
00022                    *
00023                    *      THIS ROUTINE READS A BLOCK OF DATA FROM TAPE
00024                    *
00025  0088  7708       READ     WER      A7,/8                SEND READ PARAMETERS TO THE IOP
00026  008A  8620                LDKL     A6,RDBUF             LOAD BUFFER ADDRESS
       008C  00C6  R
00027  008E  7609                WER      A6,/9                AND SEND TO IOP
00028  0090  060A                LDK      A6,/A                LOAD READ A BLOCK COMMAND
00029  0092  46C4                CIO      A6,1,/4              AND SEND TO MAG TAPE UNIT
00030  0094  5C04                RB(NA)   *-2
00031  0096  4CC4                SST      A4,/4                GET STATUS WHEN BLOCK READ
00032  0098  5C04                RB(NA)   *-2
00033  009A  A420                ANKL     A4,/7F3F
       009C  7F3F
00034  009E  EC20                CWK      A4,0                 AND CHECK FOR ANY STATUS BITS SET
       00A0  0000
00035  00A2  500A                RF(E)    *+12                 IF NO CONTINUE
00036  00A4  7E08                RER      A6,/8                CHECK IF ALL THE BLOCK HAS BEEN READ
00037  00A6  EE20                CWK      A6,0
       00A8  0000
00038  00AA  5002                RF(E)    *+4                  IF YES CONTINUE
00039  00AC  207F                HLT                           IF NO HALT STATUS IN A4
00040                    *
00041                    *      THIS ROUTINE COMPARES DATA READ WITH DATA WRITTEN
00042                    *
00043  00AE  81A0                LDKL     A9,RDBUF             LOAD ADDRESS OF READ BUFFER
       00B0  00C6  R
00044  00B2  8502                LDR      A5,A8                GET BLOCK LENGTH FROM A8
00045  00B4  EAA6       COMP1    CWR*     A10,A9               COMPARE DATA READ WITH DATA EXPECTED
00046  00B6  5002                RF(E)    *+4                  IF EQUAL CONTINUE
00047  00B8  207F                HLT                           IF NOT HALT
00048  00BA  91A0                ADKL     A9,2                 UPDATE ADDRESS IN A9
       00BC  0002
00049  00BE  9D20                SUKL     A5,2                 DECREMENT BLOCK LENGHT COUNTER
       00C0  0002
00050  00C2  5C10                RB(NZ)   COMP1                IF NOT ZERO DO ANOTHER COMPARE
00051  00C4  5F3E                RB       READ                 READ NEXT BLOCK
00052                    *
00053  00C6              RDBUF    RES      2050                 READ BUFFER
00054                           END      START
```

```
00000                           IDENT    MTTEST                ON PROGRAMMED CHANNEL
00001                  *TEST FOR ALL TAPEDRIVES
00002
00003                  *REPLACE HLTS AS FOLLOWS AND THE PROGRAM WIL
00004                  *WRITE DO BACKSPACE AND READ THE SAME BLOCK
00005                  *        HLT      ON ADDR. /009E        BY/0104
00006                  *        HLT      ON ADDR. /00A8        BY/5700
00007
00008                  *FOR RUNNING IN LOOP REPLACE ALSO
00009                  *        HLT      ON ADDR. /00CE        BY/5700
00010
00011
00012                  *WRITE TEST
00013                           AORG     /80
00014  0080  FFFF               DATA     /FFFF
00015  0082  0000               DATA     0
00016  0084  20BF       START   INH
00017  0086  8320               LDKL     A3,/FF                NUMBER OF CHARACTERS 256
       0088  00FF
00018  008A  02FF               LDK      A2,/FF                CHAR. ALL ONES
00019  008C  0103               LDK      A1,3                  WRITE COMMAND
00020  008E  41C4               CIO      A1,1,4                START CONTR. DRIVE 0
00021  0090  4204               OTR      A2,0,4                WRITE CHAR.
00022  0092  5C04               RB(4)    *-2
00023  0094  1B01               SUK      A3,1                  UPD. CHAR COUNTER
00024  0096  5C08               RB(4)    *-6                   NEXT OTR
00025  0098  4184               CIO      A1,0,4                STOP CONTROLLER
00026  009A  4CC4               SST      A4,4                  STATUS TO A4
00027  009C  5C04               RB(4)    *-2
00028  009E  207F               HLT                            STATUS IN A4
00029
00030                  *TAPE COMMANDS ROUTINE;
00031
00032                  *LOAD REGISTER A1 WITH:
00033                  *        REWIND   /0024
00034                  *        ERASE    /0019
00035                  *        WFM      /0011
00036                  *        FWD SPACE                      /0000
00037                  *        BWD SPACE                      /0004
00038                  *        SFM FWD  /0010
00039                  *        SFM BWD  /0014
00040                  *        OFF LINE /0020
00041
00042  00A0  20BF       TCR     INH
00043  00A2  41C4               CIO      A1,1,4                START FOR DRIVE 0
00044  00A4  4CC4               SST      A4,4                  STATUS TO A4
00045  00A6  5C04               RB(4)    *-2
00046  00A8  207F               HLT                            STATUS IN A4
00047
00048
00049                  *READ TEST  ONLY TO EXECUTE AFTER WRITE TEST
00050
00051  00AA  20BF       RT      INH
00052  00AC  0300               LDK      A3,0                  RESET CHARACTER COUNTER
00053  00AE  0500               LDK      A5,0                  RESET READ REGISTER
00054  00B0  8220               LDKL     A2,/1FF               EXPECTED CHAR WITH PARITY
       00B2  01FF
00055  00B4  010A               LDK      A1,/A                 READ COMMAND
00056  00B6  41C4               CIO      A1,1,4                START CONTR DRIVE 0
00057  00B8  4D04       INR     INR      A5,0,4                READ CHAR
00058  00BA  5C04               RB(4)    *-2
00059  00BC  ED08               CWR      A5,A2                 CHARACTER SAME?
00060  00BE  5412               RF(4)    DATAF                 NO GO TO FAULT
00061  00C0  1301               ADK      A3,1                  INCREMENT CHARACTER COUNTER
00062  00C2  EB20               CWK      A3,/FF                ARE THERE 256 ALREADY?
       00C4  00FF
00063  00C6  5C10               RB(4)    INR                   NEXT CHAR.
00064  00C8  4184               CIO      A1,0,4                STOP CONTROLLER
00065  00CA  4CC4       SST     SST      A4,4                  STATUS TO A4
00066  00CC  5C04               RB(4)    *-2
00067  00CE  207F               HLT                            STATUS IN A4
00068  00D0  5F4E               RB       START                 TO WRITE TEST
00069  00D2  207F       DATAF   HLT                            RECEIVED CHAR IN A5,
00070                                                           EXPECTED IN A2, FOR STATUS PUSH RUN
00071  00D4  5F0C               RB       SST
00072
00073
00074                  *IF PROGRAM LOOPS ON INR; LESS CHARACTERS IN THE BLOCK THAN EXPECTED
00075                  *NUMBER OF CHARACTERS IN A3
00076
00077                           END      START
```

20 CARD READER CONTROL UNIT P840-103 (CRLPZ) LINE PRINTER CONTROL UNIT

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20.1 CRLPZ IDENTIFICATIONS

Typenumber : P840-103
Testprogram : BCR1, for Card Reader P806-102
BLP1, for Line Printer P809-002 (X1415) or P809-004 (X1415)
I/O-channel : Card Reader, program channel or multiplex channel.
Break Connection : 1A05
Interrupt Connection: 1C05
: Line Printer, program channel or multiplex channel.
Break Connection : 1A04
Interrupt Connection: 1C04
Devices : Card Reader; Documation M300 (300 cards/min.)
Line Printer; Philips X1415, X14125 (200, 400 lines/min.)

Power Consumption : +5V, 1A

12NC number on the sticker on the board:

CRLPZ: 5111 199 7067X (5322 216 25318)

X = modification level

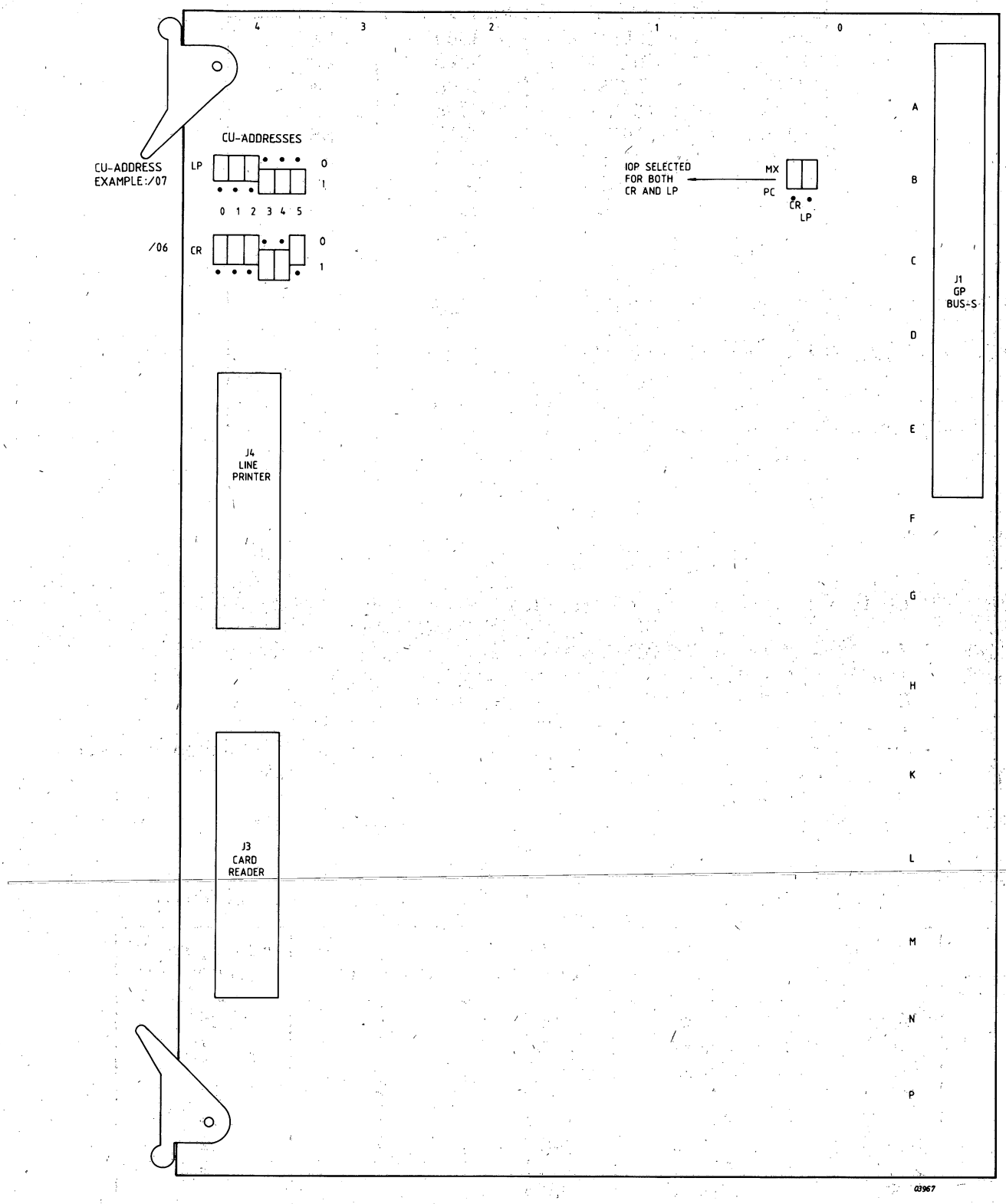


Figure 20.1 U-LINK SETTING

20.3 INTERFACE CONNECTIONS

CU Signal	Interface Signal	CU Connector	CR Connector
FNP	IPFN	3J09	KK
FHESF	IHESFN	3J23	JJ
FCP	ICIRN	3J08	MM
FSTR	IDSN	3J06	AA
FERRN	ITRN	3J11	HH
POC	IRCN	3J13	LL
SBI007	ICL01N	3J01	D
SBI008	ICL02N	3J14	K
SBI009	ICL03N	3J02	L
SBI01Ø	ICL04N	3J15	M
SBI011	ICL05N	3J03	N
SBI012	ICL06N	3J16	U
SB1013	ICL07N	3J04	V
SBI014	ICL08N	3J17	Y
SBI015	ICL09N	3J19	Z
SBI006	ICL10N	3J20	C
SBI005	ICL11N	3J21	B
SBI004	ICL12N	3J22	A

Table 20.1 CARD READER INTERFACE (CONNECTOR J3)

Line Printer to CU Signals (all active high)

ONLINE The line printer is operable.
DEMAND The line printer requests a data word.

CU to Line Printer Signals (all active high)

DATA 1-7 7 Data bits to the device, derived from BI015-9N.
PI Paper Instruction bit: high if the Data bits are for a paper instruction; low if the Data bits are for a print character. Derived from BI08N.
STROBE Data Strobe validates the PI/DATA lines to the device.

Cable for X1425 (400 lpm)

5111 199 7ØØ3Ø/ 6388Ø

CU Signal	Interface Signal	CU Connector	Old type LP Connector	New type LP Connector
FONLN	ONLINE	4J03	y	25
FDEMN	DEMAND	4J01	E	27
STRLPN	STROBE	4J07	j	21
BI008	PI	4J22	p	17
BI009	DATA 7	4J10	n	13
BI010	DATA 6	4J23	Z	11
BI011	DATA 5	4J11	V	9
BI012	DATA 4	4J24	R	7
BI013	DATA 3	4J12	L	5
BI014	DATA 2	4J25	F	3
BI015	DATA 1	4J13	B	1

Table 20.2 LINE PRINTER INTERFACE (CONNECTOR (J4)

USING DIFFERENT I.C.'s IN P450,X1150 OR P800 SYSTEM

Reader P.C. B.'s	IC location	IC used in P450, 1150	IC used in P800
clockcard (1)	C3	7416	7417
errorcard (2)	D6	7416	7417
synch. card (3)	-no-		
control card (6)	B3	7416	7417
	D4	7416	7417
	D6	7416	7417
	A4	7404 *	7417

* 7416 also possible

Interface P800 active low
Interface P450/X1150 active high

Table 20.3 DOCUMATION CARDREADER (M300) COMPATIBILITY

20.4 HARDWARE-SOFTWARE INTERFACE DETAILS

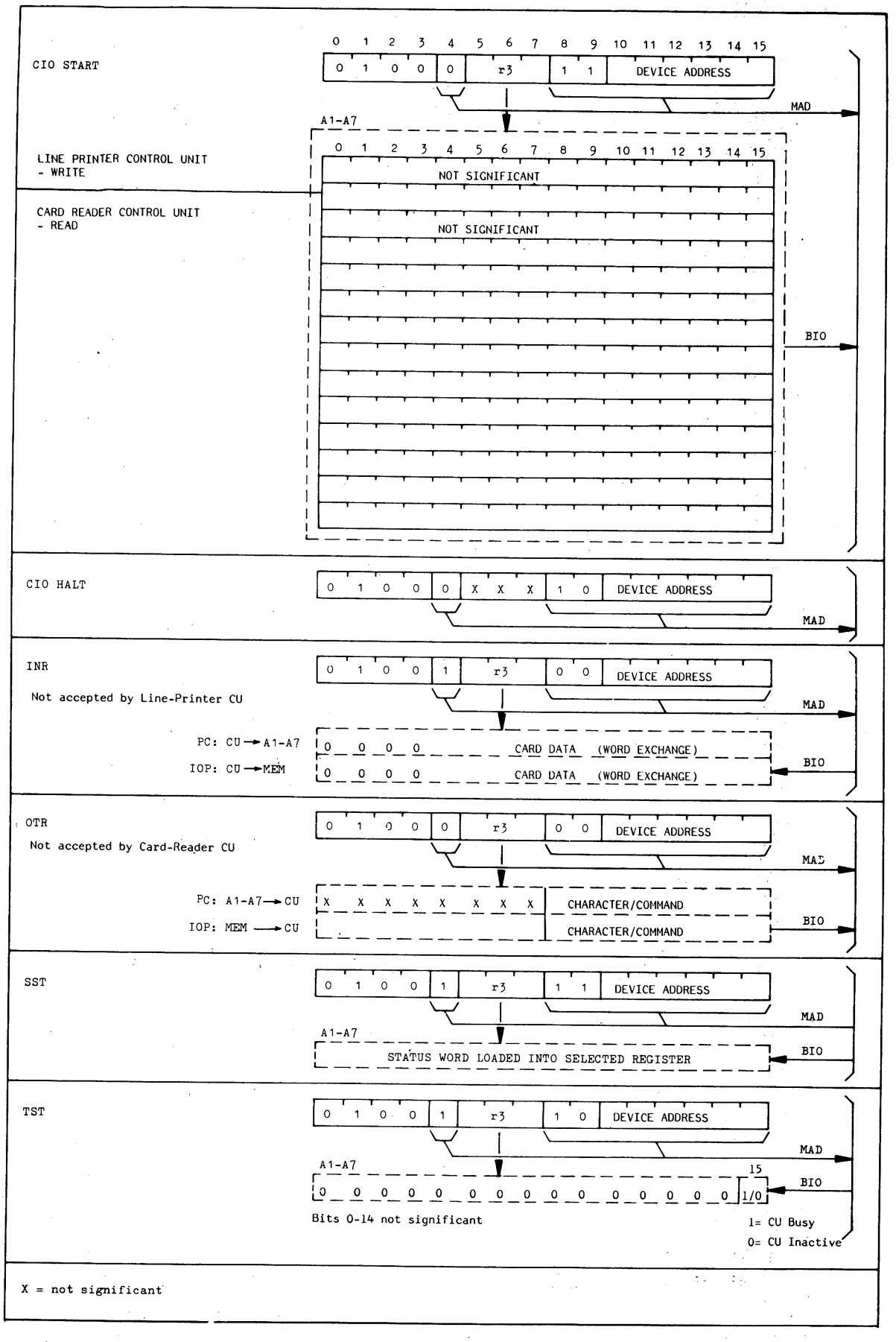


Figure 20.2 INSTRUCTION / COMMAND-WORD FORMATS

DATA and PRINT CONTROL CHARACTER CODE

BIO Lines	08	09	10	11	12	13	14	15
Code Bit Number	PI	7	6	5	4	3	2	1

When the value of PI is 0 the other seven bits represent either a printable character or a format control character.

VERTICAL FORMAT CONTROL CODE

BIO Lines	08	09	10	11	12	13	14	15
Code Bit Number	PI	7	6	5	4	3	2	1
Logic Value	1	1	X	0	0	Channel Number		

where --

- X is not significant.
- Channel Number indicates the channel number in the paper tape control loop.

BIO Lines	08	09	10	11	12	13	14	15
Code Bit Number	PI	7	6	5	4	3	2	1
Logic Value	1	1	X	1	Number of Lines			

where --

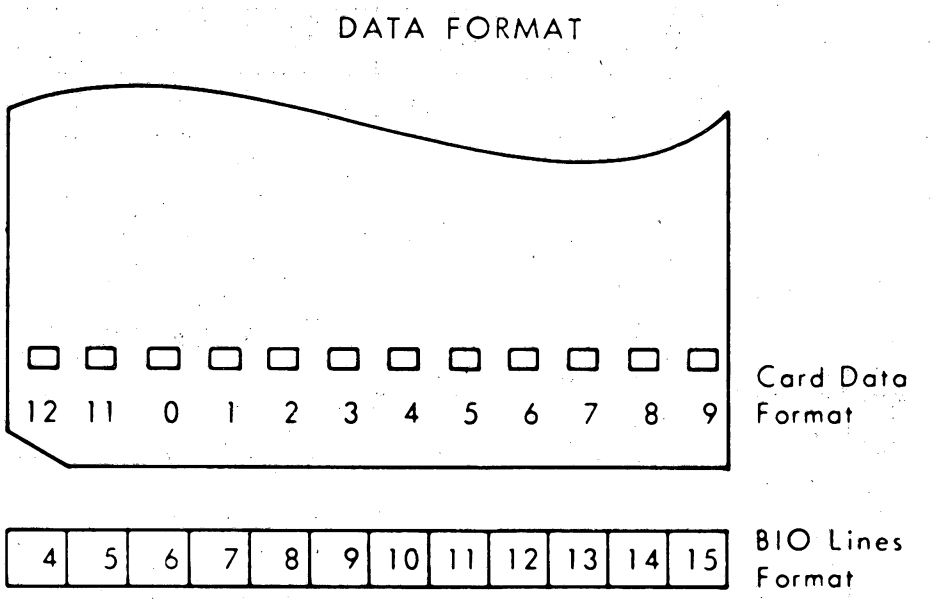
- X is not significant.
- Number of Lines indicates the number of lines to be skipped from 0 to 15.

Character Code

			b7	0	0	0	1	1
			b6	0	1	1	0	0
b4	b3	b2	b1 b5	0	0	1	0	1
0	0	0	0		Space	Ø	@	P
0	0	0	1		!	1	A	Q
0	0	1	0		"	2	B	R
0	0	1	1		#	3	C	S
0	1	0	0		$	4	D	T
0	1	0	1		%	5	E	U
0	1	1	0		&	6	F	V
0	1	1	1		'	7	G	W
1	0	0	0		(	8	H	X
1	0	0	1		)	9	I	Y
1	0	1	0	PF	*	:	J	Z
1	0	1	1		+	;	K	[
1	1	0	0	FF	,	<	L	◇
1	1	0	1	CR	-	=	M	]
1	1	1	0		.	>	N	^
1	1	1	1		/	?	O	♡

- PF Paper Feed: advances the paper one line and prints buffer-contents
- FF Form Feed : advances the paper to the top of the next sheet of paper and prints the buffer-contents
- CR Carriage Return: prints buffer-contents

Figure 20.3 CONTROL AND CHARACTER CODES LINE PRINTER



Note: A hole is a "1".

Figure 20.4 CARD DATA FORMAT

20.4.1 STATUS WORD

LP-CU

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Not Operable

CR-CU

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0	0		0		0		

Not Operable
Throughput Error
Incorrect Length
Hopper Empty/ Stacker Full

NOT OPERABLE

Bit 15 is set:
- If the Line Printer is inoperable, due to Switched-off/ not On-Line or Paper-Fault.
- If Card Reader is inoperable, due to Switched-off/ not On-Line or Pick-error / Stacker Full / Hopper-Empty.

THROUGHPUT ERROR

Bit 14 is set:
- If a new character is read and the CPU/IOP did not yet answer the data-request Interrupt/Break.

INCORRECT LENGTH

Bit 12 is set:
- If the number of data exchanges by CPU or IOP differs from the number of characters on the card.

HOPPER EMPTY / STACKER FULL

Bit 10 is set:
- If either of these conditions is true.

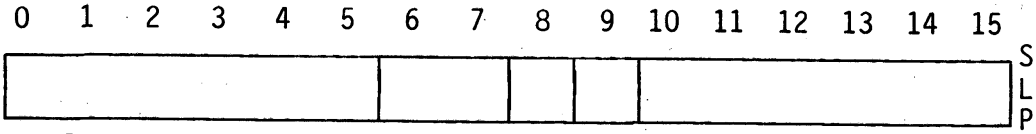
20.5 SHORT DESCRIPTION TESTPROGRAMS

TESTPROGRAM BLP1 4K

1. IPL
   Program stops at /700 (restart address and normal end).

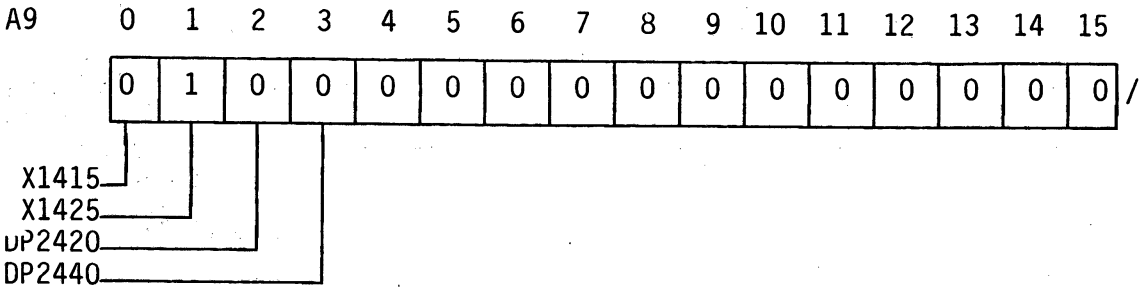
2. Switch on RTC (PF/AR also possible) P851: after program runs.

3. A8

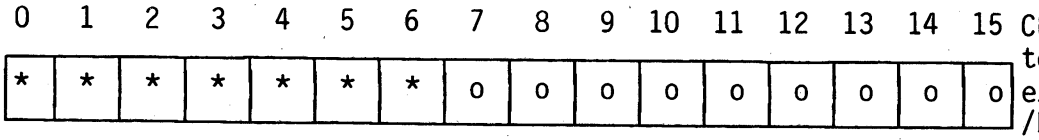


Standard Levels:
P851/4:
/3407
Int. Level:
/D

A9



A10



Checks to be executed
/FE00

* = Standard
o = Optional

Setting (X1415/25)

4. Depress MC, RUN

   Error stop at address /5F0
   Restart after power/off at /6EE
   Interrupts return to /700

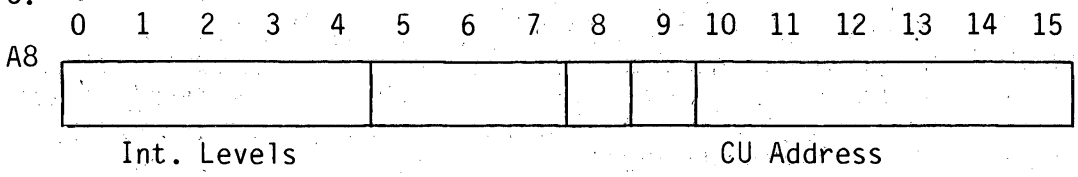
For more information see official description of testprogram.

TESTPROGRAM BCR1 4K

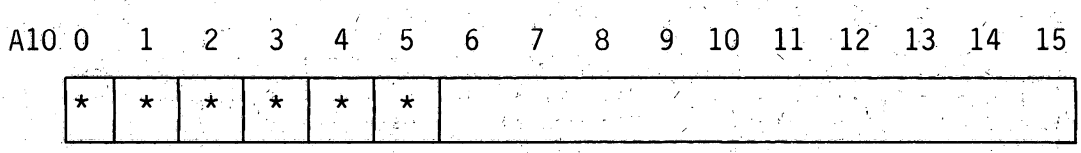
1. IPL
   Program stops at /700 (restart address and normal end).
   Set of special cards on the cardreader.

2. Switch on RTC (PF/AR also possible) P851: after program runs.

3.



Standard Levels: P851/P854 /3006 /5406 Int. Levels: /C- /15



Checks to be executed

* = Standard

4. Depress MC, RUN

   Error stop at /5F0
   Restart after power-off /6EE
   Interrupt returns to address /700

For more information see official description of testprogram.

20.6 SHORT ROUTINES

LINE PRINTER

This program is written for Programmed Channel operation so if the printer is normally used on the IOP Channel the CU must be connected to operate ont he Programmed Channel. The program can be loaded either with the IPL routine or by hand using the switches on the control panel. Once loaded the following routine should be used:

- Load register A6 with the ASCII character to be printed.
- Load register A7 with number of times you want the character printed on each line.
- Load register A0 with the Start address.
- Push the RUN button.

To stop the program push the INST button.

Program LINELP

Memory Address	Data	Program Instructions		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	Start	HLT	
0086	20BF		INH	
0088	0200		LDK	A2,0
008A	4BC7		SST	A3,/07
008C	42C7		CIO	A2,1,/07
008E	5C04		RB(NA)	* -2
0090	050A	OUTLF	LDK	A5,/0A
0092	4507		OTR	A5,0,/07
0094	5C04		RB(NA)	* -2
0096	4607	OUTCH	OTR	A6,0,/07
0098	5C04		RB(NA)	* -2
009A	1201		ADK	A2,1
009C	EA1C		CWR	A2,A
009E	5C0A		RB(NE)	OUTCH
00A0	0200		LDK	A2,0
00A2	5F14		RB	OUTLF

```
          DATE  80-03-13        IDENT    LPIOP

00000                           IDENT    LPIOP
00001                    *
00002                    *
00003                    *      THIS PROGRAM STORES TWO SELECTED CHARACTERS INTO A BUFFER
00004                    *      THEN PRINTS THEM AND STOPS WAITING NEW CHARACTERS TO BE SELECTED
00005                    *
00006                    *
00007         0000       BEGIN  EQU      *
00008                           RORG     BEGIN+/80
00009                    *
00010                    *
00011                    *      LOAD THE TWO CHARACTERS TO BE PRINTED IN REGISTER A3
00012                    *
00013                    *      PUSH THE RUN BUTTON
00014                    *
00015  0080  FFFF               DATA     /FFFF
00016  0082  0000               DATA     0
00017  0084  207F       START   HLT
00018  0086  20BF               INH
00019  0088  850C               LDR      A5,A3              LOAD DATA INTO A5
00020  008A  0100               LDK      A1,0               CLEAR CHAR COUNTER
00021  008C  8545       REPT    ST       A5,LPBUF,A1        STORE THE CONTENTS OF A5 INTO LPBUF
       008E  00B8  R
00022  0090  1102               ADK      A1,2               UPDATE LPBUF ADDRESS
00023  0092  E920               CWK      A1,78              AND CHECK IF LINE FULL
       0094  004E
00024  0096  5C0C               RB(NE)   REPT
00025  0098  8520               LDKL     A5,/0D0A           LOAD CARRIAGE RETURN LINE FEED CHARS
       009A  0D0A
00026  009C  8545               ST       A5,LPBUF,A1        AND STORE IN LPBUF
       009E  00B8  R
00027  00A0  8120               LDKL     A1,/4050           LOAD PARAMS FOR FIRST WER
       00A2  4050
00028  00A4  710E               WER      A1,/E              AND SEND TO IOP
00029  00A6  8120               LDKL     A1,LPBUF           LOAD FIRST ADDRESS OF LPBUF
       00A8  00B8  R
00030  00AA  710F               WER      A1,/F              AND SEND TO IOP
00031  00AC  0600               LDK      A6,0
00032  00AE  46C7               CIO      A6,1,/7            SEND START COMMAND TO PRINTER
00033  00B0  5C04               RB(NA)   *-2                TRY AGAIN IF NOT ACCEPTED
00034  00B2  4CC7               SST      A4,7               GET STATUS
00035  00B4  5C04               RB(NA)   *-2
00036  00B6  5F34               RB       START              GO AND WAIT FOR NEW DATA
00037                    *
00038  00B8              LPBUF   RES      80                 OUTPUT BUFFER
00039                           END      START
```

```
            DATE  82-05-05        IDENT    CRPROG


0000                              IDENT    CRPROG
0001                        *
0002                        *
0003                        *     THIS PROGRAM READS A CARD VIA THE PROGRAMMED CHANNEL AND STOPS SO THAT
0004                        *     CONTENTS OF THE BUFFER CAN BE CHECKED AGAINST THE PUNCHED HOLES IN THE
0005                        *     CARD
0006                        *
0007      0000              BEGIN   EQU      *
0008                              RORG     BEGIN+/80
0009                        *
0010                        *
0011                        *     LOAD THE CARD(S) TO BE READ INTO THE CARDREADER
0012                        *     AND START THE CARD READER
0013                        *
0014                        *     LOAD START ADDRESS(/0086) IN A0 AND PUSH THE RUN BUTTON
0015                        *
0016 0080 FFFF                    DATA     /FFFF
0017 0082 0000                    DATA     0
0018 0084 207F              START HLT
0019 0086 20BF                    INH
0020 0088 0200                    LDK      A2,0                 LOAD ZERO IN A2
0021 008A 0100                    LDK      A1,0                 CLEAR WORD COUNTER
0022 008C 8245 00B8 R       STORE ST       A2,BUFF,A1           STORE ZERO INTO BUFF ADDRESS
0023 0090 1102                    ADK      A1,2                 UPDATE WORD COUNT OF BUFF ADDRESS
0024 0092 E920 002A               CWK      A1,42                CHECK IF LAST WORD IS REACHED
0025 0096 5C0C                    RB(NE)   STORE                NO? GO AND STORE THE NEXT WORD
0026 0098 0100                    LDK      A1,0                 CLEAR CHARACTER COUNTER
0027 009A 0601                    LDK      A6,1
0028 009C 46C6                    CIO      A6,1,6               SEND CIO START COMMAND TO THE CARDREADER
0029 009E 5C04                    RB(NA)   *-2
0030 00A0 4D06              READ  INR      A5,0,6               GET CHARACTER FROM CU
0031 00A2 5C04                    RB(NA)   *-2
0032 00A4 8545 00B8 R             ST       A5,BUFF,A1           AND STORE IN BUFFER
0033 00A8 1102                    ADK      A1,2                 UPDATE BUFFER ADDRESS
0034 00AA E920 00A0               CWK      A1,/A0               CHECK IF LAST COLUMN READ
0035 00AE 5C10                    RB(NE)   READ                 NO? GO AND READ NEXT COLUMN
0036 00B0 4686                    CIO      A6,0,6               SEND STOP COMMAND TO CU
0037 00B2 4CC6                    SST      A4,6                 GET STATUS FROM CU
0038 00B4 5C04                    RB(NA)   *-2
0039 00B6 5F34                    RB       START                GO AND WAIT FOR NEXT RUN
0040                        *
0041 00B8                   BUFF  RES      42                   READ BUFFER
0042                              END      START


        SYMBOL TABLE

BEGIN   0000  R   BUFF    00B8  R   READ    00A0  R   START   0084  R
STORE   008C  R

        ASS.ERR.    0000
:EOF
PROG ELAPSED TIME:  00H-00M-10S-980MS-
```

CARD READER

This program is written to use the IOP channel. If the Card Reader normally operates on the Programmed Channel it will be necessary to connect the Break Request line on the CU. The program will read one card and stop; the data on the card can be checked by displaying the contents of the program buffer, BUFF. Once the program has been loaded either by the IPL routine or by hand using the control panel switches, it is only necessary to load the start address into register A0 and push the RUN button.

Program CRTEST

Memory Address	Data	Program Instructions		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	Start	HLT	
0086	20BF		INH	
0088	8120		LDKL	A1,/8050
008A	8050			
008C	710C		WER	A1,/0C
008E	8220		LDKI	A2,BUFF
0090	009E			
0092	720D		WER	A2,/0D
0094	43C6		CIO	A3,1,/06
0096	5C04		RB(NA	* -2
0098	4CC6		SST	A4,/06
009A	5C04		RB(NA)	* -2
009C	5F1A		RB	Start
009E		BUFF		

21 PAPER TAPE READER, PAPER TAPE PUNCH CONTROL UNIT P840-141 (TRPZ)

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21.1 TRPZ IDENTIFICATIONS

Name : TRPZ, control unit for paper Tape Reader and Paper Tape Punch.
Typenumber : P840-141
Testprogram : BPTR1 for PTR P801-001
BPTP1 for PTP P803-001
I/O-channel : PTR, program channel or multiplex channel.
Break Connection : 1A04
Interrupt Connection: 1C04
:PTP, program channel or multiplex.
Break Connection : 1A05
Interrupt Connection: 1C05
Devices : Digitronics 2540 EP (300 char./sec.), P801-001
Facit 4070 (75 char./sec.) P803-001

Power Consumption : +5V, 1.0A (L)

12NC number on the sticker on the board:

TRPZ: 5111 199 7295X (5322 216 25126)

X = Modification level

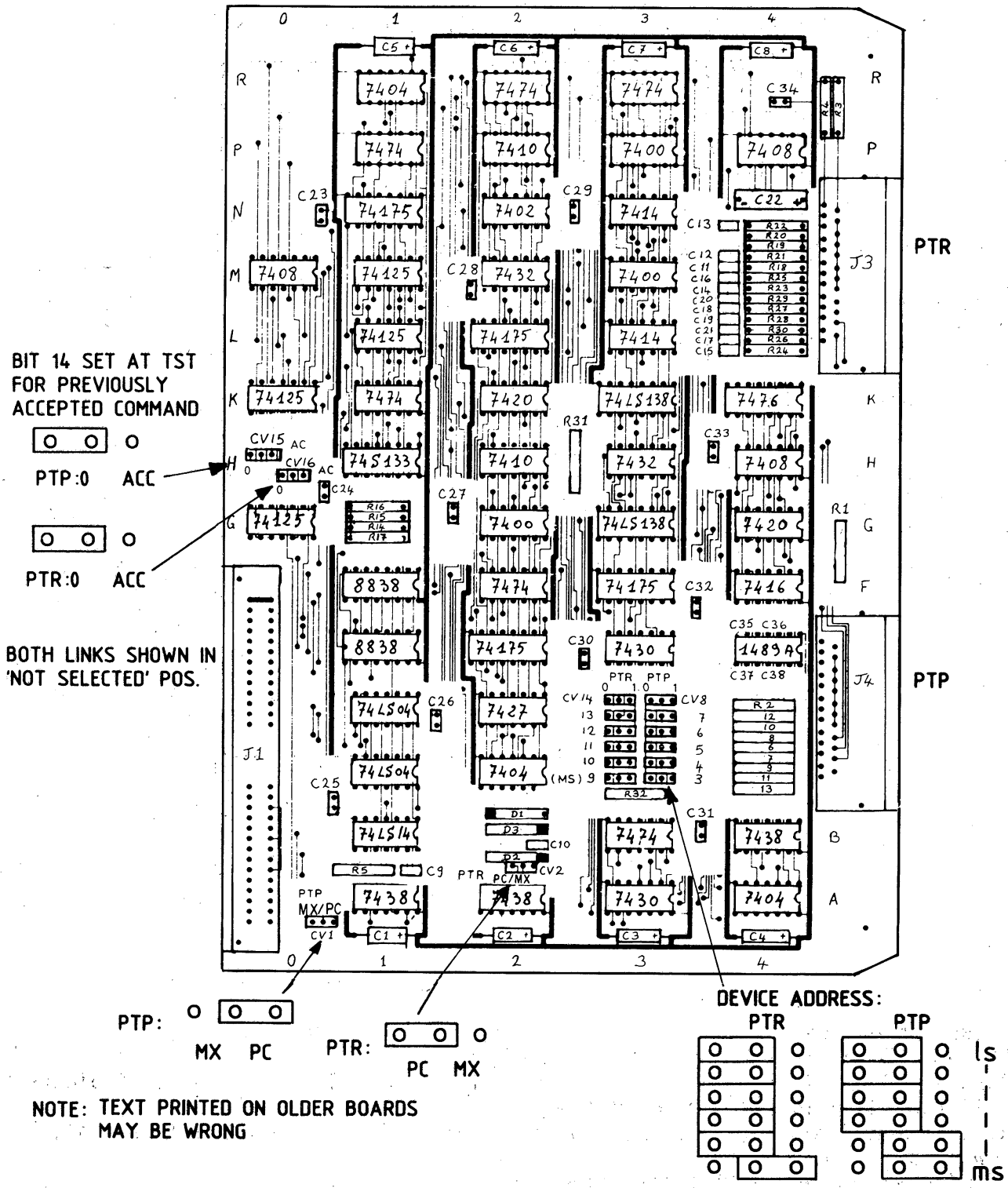


Figure 21.1 U-LINK SETTING TRPZ

21.3 INTERFACE CONNECTIONS

21.3.1 PAPER TAPE READER

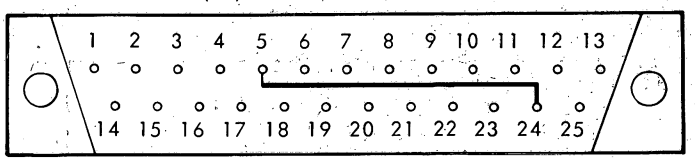
Signal	(3J) Card Connector	Reader Connector	Cable Colours (Twisted Pairs)
RCH1	1	D	Yellow/Brown
Ground	Ground	4	
RCH3	2	F	Yellow/Pink
Ground	Ground	6	
RCH5	3	J	Yellow/Green
Ground	Ground	8	
RCH7	4	L	Pink/Green
Ground	Ground	10	
SPKTB	6	N	Pink
0 volts	7	12	
EOT	8	AA	Blue
0 volts	22	23	
LTL	9	CC	Grey/Green
0 volts	23	25	
READY	11	W	Pink/Blue
0 volts	10	A	
FWD	13	18	Red
0 volts	12	9	
RCH2	14	E	White/Grey
0 volts	18	5	
RCH4	15	H	White/Green
0 volts	19	7	
RCH6	16	K	Pink/Grey
0 volts	20	9	
RCH8	17	M	Pink/Red
0 volts	21	11	
STOP	25	20	Grey
Ground	Ground	10	
0 volts	5		Copper Link between pins
0 volts	24		

Reader Interface
RCH1-8 - Data lines between device and TRPZ.
RSPKTB - Sprocket hole signal goes high when the hole is sensed to indicate to TPRZ that data is on the RCH1-8 lines.
RLTL - Load lever to hold the tape in position RLTL high (load lever up), RLTL low (load lever down).
READY - Indicates to TRPZ that power at the device is on.
REOT - This signal goes active high when end of tape has been read.
FWD and STOP - A CIO Start sets the R.Start/Stop F/F to enable FWD which enables the Reader device. A CIO Halt resets the F/F to enable STOP which halts the Reader.

Table 21.1 CONTROL UNIT TO DEVICE CONNECTIONS - PTR

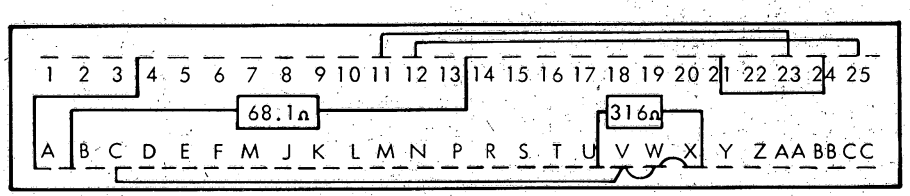
Connections Between 3J and Reader. Inside each connector special connections are made.

Control Unit End of Cable (3J)



A tinned copper wire (1.5mm dia.) forms the Logic Ground (0V). If a connector pin is not available one wire from each twisted pair is connected to Logic Ground.

Device End of Cable



Between pins U and X, 316Ω 1/4W resistor (2322 152 53161)

Between pins 13 and B, 68.1Ω 1/4W resistor (2322 152 56819), sleeved at each end.

Wire link between pins 25 and 12, length 60mm

Wire link between pins 23 and 11, length 55mm

Wire link between pins A and 04, length 25mm

Wire link between pins V and W, length 15mm

Wire link between pins W and X, length 15mm

Wire link between pins C and V, length 70mm

Wire link between pins 21 and 24, length 22mm

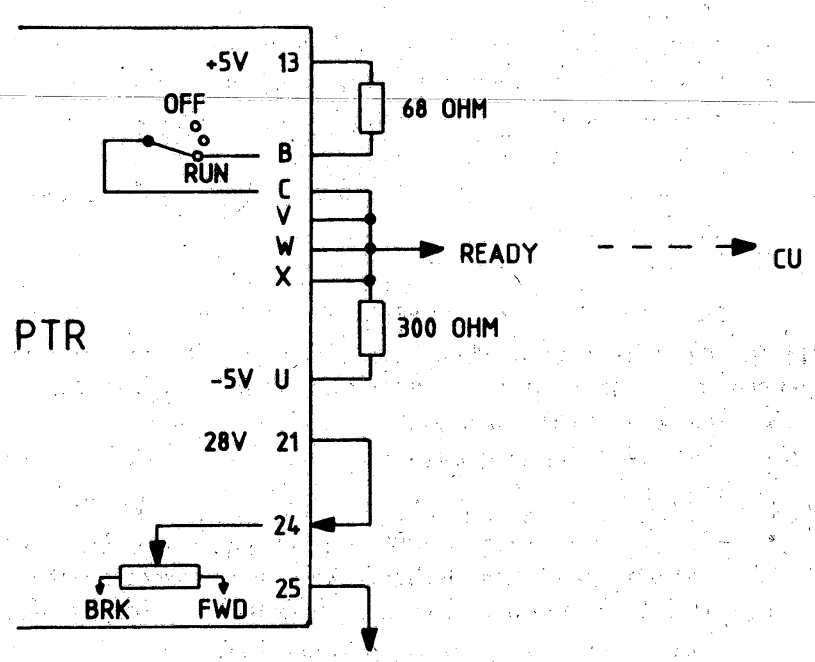


Figure 21.2 PTR CONNECTION

21.3.2 PAPER TAPE PUNCH

Signal	(4J) Card Connector	Punch Connector	Cable Colours (Twisted Pairs)
PCH1	13	1	Yellow/Brown
Ground	Ground	Ground	
PCH3	12	3	Yellow/Pink
Ground	Ground	Ground	
PCH5	11	5	Yellow/Green
Ground	Ground	Ground	
PCH7	10	7	Pink/Green
Ground	Ground	Ground	
PCH9	8	9	Pink
Ground	Ground	Ground	
PI	7	11	Blue
0 volts	6	Ground	
PTL	5	21	Grey/Green
0 volts	18	Ground	
PERR	4	20	Pink/Blue
0 volts	17	Ground	
POPE	3	24	Red
0 volts	16	Ground	
PR	1	12	White/Grey
0 volts	2	Ground	
PCH2	25	2	White/Green
0 volts	20	Ground	
PCH4	24	4	Pink/Grey
0 volts	19	Ground	
PCH6	23	6	Pink/Red
Ground	Ground	Ground	
PCH8	22	8	Grey
0 volts	21	Ground	
PSD	14	10	Red/Brown
Ground	Ground	Ground	
0 volts	9	14	Copper Link between pins
0 volts	15	25	to from Gnd. connection

Punch Interface

Punch interface signals are in both directions, see following paragraphs.

TRPZ → Punch.

- PCH1-8 — Data lines between TRPZ and device.
- PCH9 — Active high punches the sprocket feed hole.
- PI — Initiates the punching action at the device. PI is linked to PCH9 at TRPZ.
- PSD — Connected permanently to 0V to enable tape in the forward direction.

Punch → TRPZ. Signals received from the Punch are routed via Line Receivers type MC1488L. These receivers are permanently enabled so that when the signal is received it is inverted for the control logic.

- PERR — Punch Error is normally low but goes active high to indicate to TRPZ that the tape is jammed or broken.
- POPE — Punch Operable goes high when power at the device is on.
- PR — Punch Ready goes high when the punching of the previous character is complete and the device is ready to accept a new character
- PTL — Tape Low goes high to set the BIO Buffer Gates and enable BIO10 to go low when an SST instruction is executed.

Table 21.2 CONTROL UNIT TO DEVICE CONNECTIONS-PTP

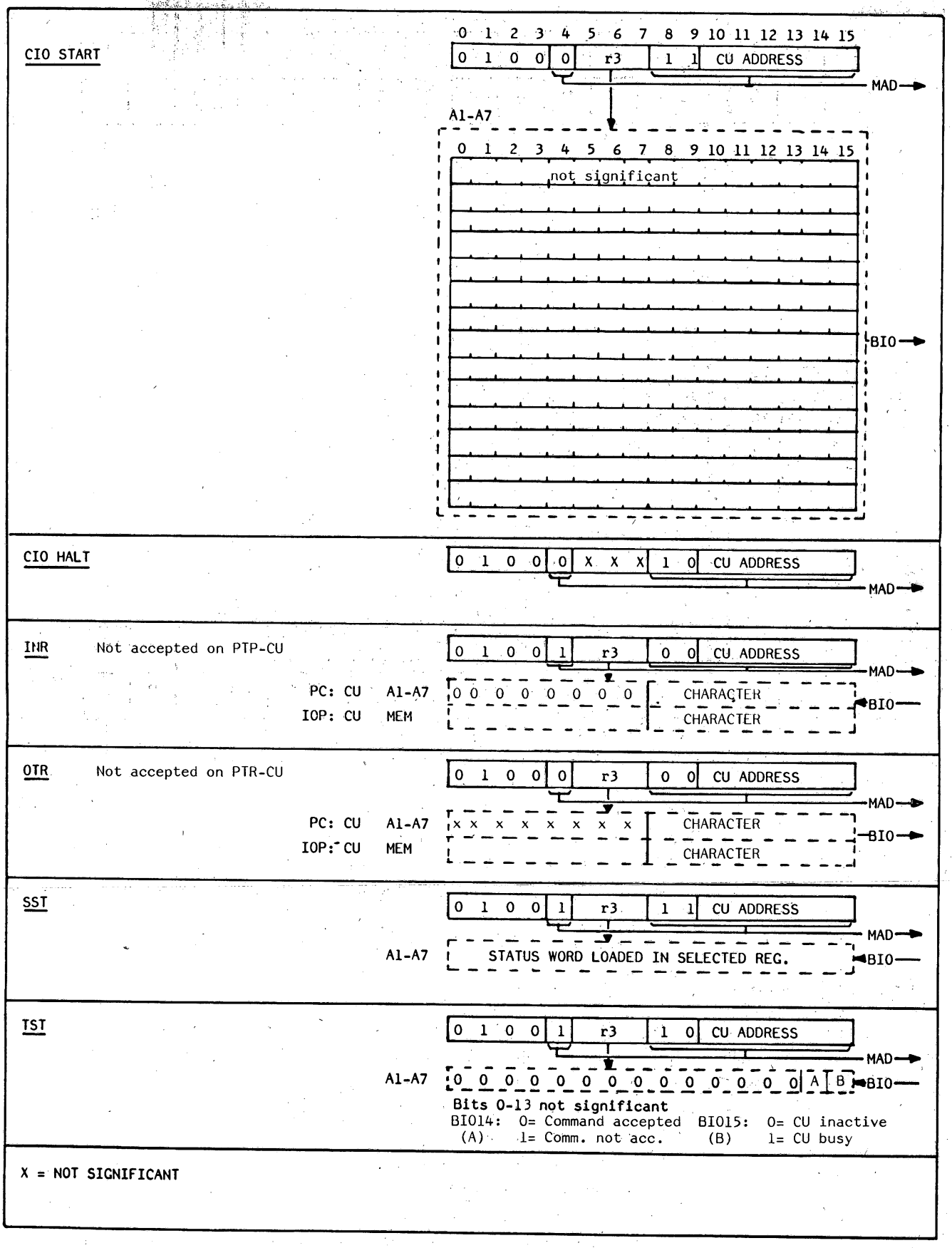
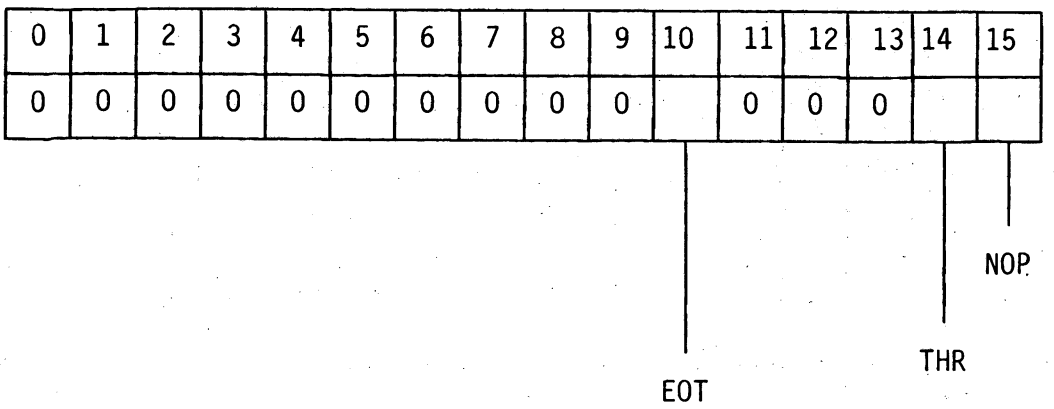


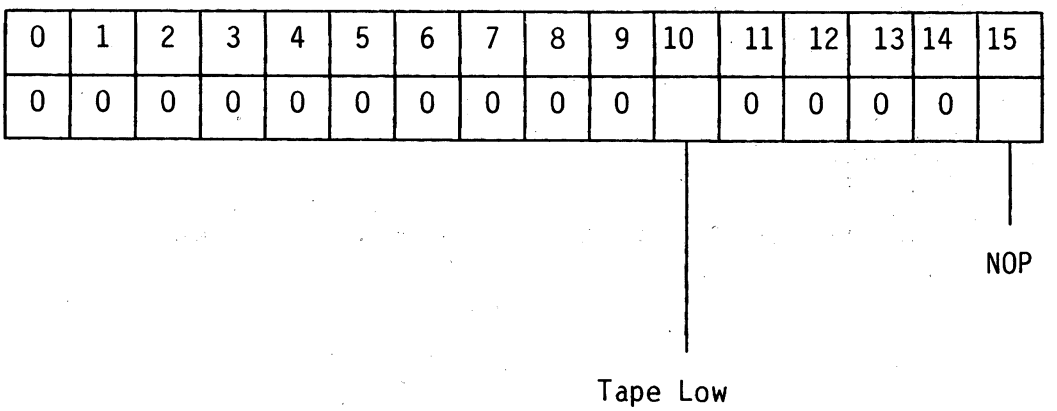
Figure 21.3 INSTRUCTION/COMMAND WORD FORMATS

21.4.1 STATUSWORD PTR



EOT: End of Tape
THR: Throughput Error
NOP: Not Operable device
- power off (not ready)
- load tape lever 'up'
- End of Tape

21.4.2 STATUSWORD PTP



NOP: Not Operable device
- power off
- tape jammed or broken

21.5 SHORT DESCRIPTION OF TESTPROGRAMS

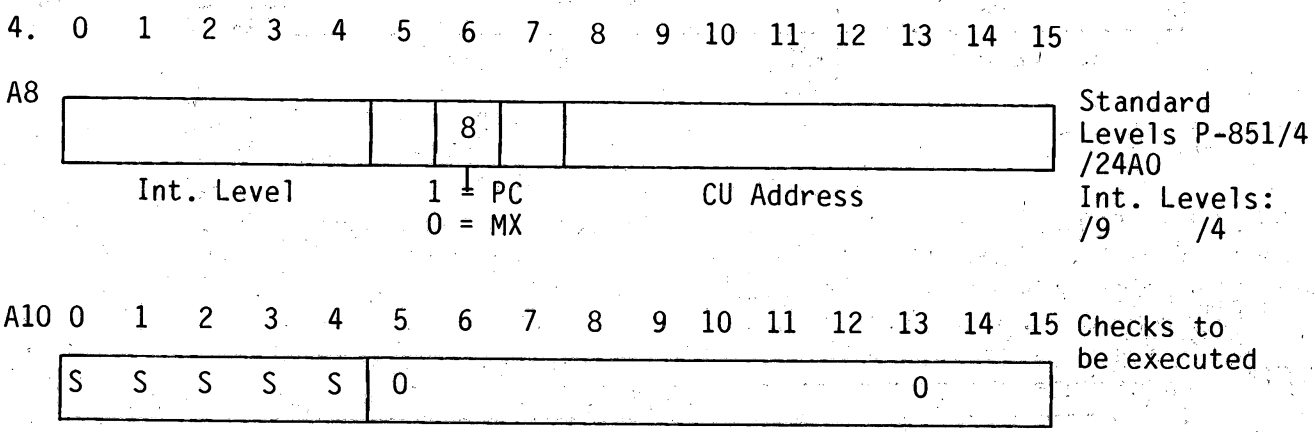
TESTPROGRAM BPTR1 4K

1. IPL
   Program stops at address /700 (restart address and normal end)

2. Switch on RTC (PA/AR also possible) P-851: After program runs.

3. Load PTP-Reference Tape.

4.



S = Standard setting

5. Depress MC, RUN

Error stop at address /5F0, Reg. A1 indicates fault.
Restart after power/off at address /6EA.
Interrupts return to address /700.

For more information see official description of testprogram.

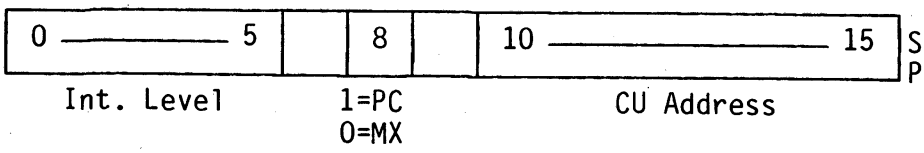
TESTPROGRAM BPTP 1 4K

1. IPL
   Program stops at address /700 (restart address and normal end).

2. Switch on RTC (PF/AR also possible) P-851: after program runs.

3. PTP

A8

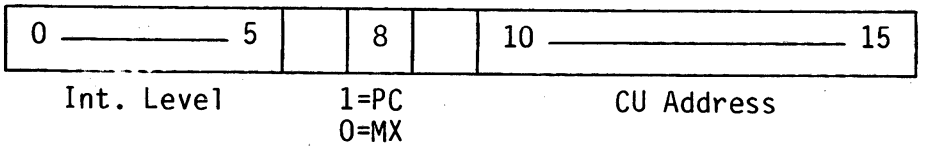


Standard Levels:
P851/4

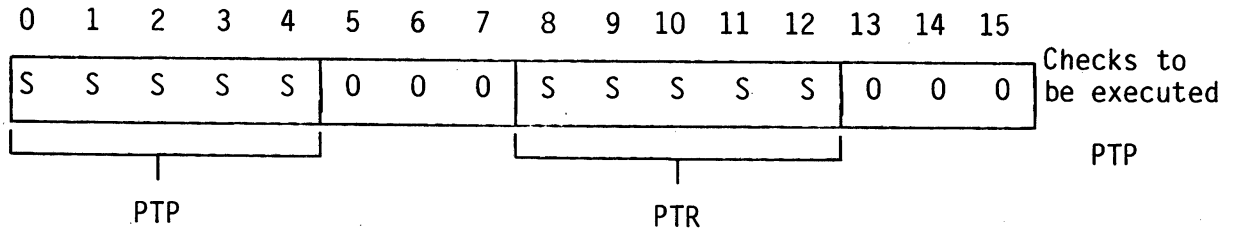
PTP /2880
Int. Level /A
PTR /24A0
Int. Level /9

PTR

A12



A10



Checks to be executed

PTP

S = Standard setting

4. Depress MC, RUN

   Tape will be punched, program will stop at address /5E0.

5. Load the punched reference tape in the Paper Tape Reader.

6. Depress RUN (RTC must be ON).

Error stop at address /5F0.
Restart after power-off at address /6E2.
Interrupts return to address /700.

For more information see official description of the testprogram.

PAPER TAPE READER

This peripheral and CU can be checked with the aid of a simple program called PTR if the standard test program either cannot be loaded or will not run.

PTR .

This program enables the engineer to read 80 characters from any piece of paper tape and then verify the transfer by checking the contents of the buffer area against the holes punched in the tape. The program can be loaded either by the IPL routine or by hand using the switches on the control panel and it will ignore blank tape. Once loaded it is only necessary to load the Start address in (/0086) register A0 and push the RUN button. The program will then read 80 characters from the tape and stop. If you wish to read another 80 characters just push the RUN button.

Program PTR

Memory Address	Data	Program Instructions		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	Start	HLT	
0086	20BF		INH	
0088	0750		LDK	A7,80
008A	0600		LDK	A6,0
008C	0501		LDK	A5,1
008E	45E0	PTR1	CIO	A5,1,/20
0090	5C04		RB(NA)	* -2
0092	4C20		INR	A4,0,/20
0094	5C04		RB(NA)	* -2
0096	45A0		CIO	A5,0,/20
0098	4BE0		SST	A3,/20
009A	5C04		RB(NA)	* -2
009C	EC21		CCK	A4,0
009E	0000			
00A0	5814		RB(Z)	PTR1
00A2	E459		SC	A4,BUFF,A6
00A4	00AE			
00A6	1601		ADK	A6,1
00A8	EF18		CWR	A7,A6
00AA	5C1E		RB(4)	PTR1
00AC	5F2A		RB	Start
00AE		BUFF	Start Address of Buffer Area	

PAPER TAPE PUNCH

This program enables an area of memory (selected by the engineer) to be punched out on paper tape. The program can be loaded either by the IPL routine or by hand using the control panel switches. Once loaded the following routine should be used:

- Load the starting address to be punched into register A7.
- Load the ending address of the area into register A8.
- Push the FEED HOLES button on the Tape Punch to provide a leader for the tape.
- Load the starting address of the program into register A0. (/0086)
- Push the RUN button.

The program will stop on /86 when the required area has been punched, then:

- Push the FEED HOLES button until 30cm of blank tape has been perforated.

Program PUNCH

Memory Address	Data	Program Instructions		
0080	FFFF		DATA	/FFFF
0082	0000		DATA	0
0084	207F	START	HLT	
0086	20BF		INH	
0088	811C		LDR	A1,A7
008A	8402		LDR	A4,A8
008C	1402		ADK	A4,2
008E	47F0		CIO	A7,1,/30
0090	E524	CONT	LCR	A5,A1
0092	4530		OTR	A5,0,/30
0094	5C04		RB(NA)	* -2
0096	1101		ADK	A1,1
0098	E910		CWR	A1,A4
009A	5C0C		RB(NE)	CONT
009C	4280		CIO	A2,0,/30
009E	4AF0		SST	A2,/30
00A0	5C04		RB(NA)	* -2
00A2	5F20		RB	START

22 SYNCHRONOUS/A-SYNCHRONOUS LINE CONTROL UNIT P845-160 (SALCU-Z)

SECTION	22.1	SALCU-Z IDENTIFICATIONS	PAGE 22-2
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	22.6	SHORT DESCRIPTION OF TESTPROGRAM	22-12
	22.7	SHORT ROUTINES	22-13

LIST OF ILLUSTRATIONS

FIGURE	22.1	U-LINK SETTING	22-4
	22.2	INTERFACE WIRING CU-TERMINAL (LOCAL)	22-10
	22.3	INTERFACE WIRING CU-CU (LOCAL)	22-10

LIST OF TABLES

TABLE	22.1	SALCUZ SOCKET 3 CONNECTIONS TO DCTE	22-9
	22.2	STANDARD CABLE SALCUZ	22-9

22.1 SALCUZ IDENTIFICATIONS

Typenumber	: P845-160	
Testprogram	: BZSAC1	
Channel	: PC or IOP	
	Interrupt Connection:	Transmitter 1C04
		Receiver 1C05
	Break Connection :	Transmitter 1A05
		Receiver 1A05
Devices	: 1 line, Full Duplex or Half Duplex	
Power Consumption	: +5VL, 1.5Amp	
	+12VL 50mA	
	-12VL 90mA	

12NC code on the sticker on the board:

5111 199 6694x (5322 216 25253)

X = Modification level

22.2 FACILITIES

- Synchronous or A-synchronous (start/stop) Line Control Unit.
- 1 line, Full Duplex or Half Duplex.
- Connection of modems with V24/V28 interface or local connection.
- Transfer rate selectable: A-synchronous 50 - 19,200 bps
  Synchronous 800 - 56,200 bps (internal clock)
- Word length 5 - 6 - 7 or 8 bits selectable.
- Parity (VRC) software controlled.
- Stopbits 1 - 1.5 - 2 selectable (A-synchronous)
- Echo mode selectable (SALCU Half Duplex, 4 wire connection)
- Break character detection (Half Duplex, input during output detected, A-synchronous only)
- Break generation possible ('0' = high for 220 msec., A-synchronous only)
- CT119 for connection of CT133 from PER 3100 CTW (A-synchronous only)
- Stop on Halt character code
- Connection of MODEM clock (CT114, 115) or internal clock (CT113) for local use or test. (Synchronous only)
- Transparancy mode selectable (Synchronous only)
- Use of Call Indicator (CT125) selectable
- Device address transmitter = odd receiver = even
  interrupt transmitter on pin 1C04 receiver on pin IC05
  break transmitter on pin 1A04 receiver on pin 1A05
- Programmed channel or IOP - channel selectable
  Note: -- WAIT MODE IS NOT POSSIBLE --

22.3 INSTALLATION DETAILS

Link:	A/S:	Setting:	Description:
TP		INT: 1 = o, 0 = o, 2 = o; EXT: 1 = o, 0 = o, 2 = o	Selection of the transmit baud rate freq. (internal or modem)
RP		INT: 1 = o, 0 = o, 2 = o; EXT: 1 = o, 0 = o, 2 = o	Selection of the receive baud rate freq. (internal modem)
192	A	no: o, o, o; yes: o, o, o	CT119 option operational
C1, C2, C3		See table below	Select Halt Character
25		yes: o, o, o; no: o, o, o	Calling indicator (CT125) option operational

C1 C2 C3 (1 / 0 / 2)	ASCII	EBCDIC
o o o / o o o / o o o	=	NACK
o o o / o o o / o o o	7	EOT
o o o / o o o / o o o	.	ACK
o o o / o o o / o o o	NACK	NL
o o o / o o o / o o o	CR	CR
o o o / o o o / o o o	EOT	PF
o o o / o o o / o o o	ACK	LC
o o o / o o o / o o o	ETX	ETX

Figure 22.1 U-LINK SETTING

RD,RC,RB,RA,RT

Position					local Linking	
o o o RD	o o o RC	o o o RB	o o o RA	1 o 2 RT	A	S
2	2	2	2	1	50	(800)*
2	2	2	1	1	75	(1200)*
2	2	1	2	1	110	(1760)*
2	2	1	1	1	134.5	(2152)*
2	1	2	2	1	150	(2400)*
X	X	X	X	2	200	(3200)*
2	1	2	1	1	300	(4800)*
2	1	1	2	1	600	(9600)*
2	1	1	1	1	1200	(19200)*
1	2	2	2	1	1800	(28800)*
1	2	2	1	1	2000	(32081)*
1	2	1	2	1	2400	(38400)*
1	2	1	1	1	3600	(57600)*
1	1	2	2	1	4800	
1	1	2	1	1	7200	
1	1	1	2	1	9600	
1	1	1	1	1	19200	

* If internal clock is used.

Note: A = Asynchronous Mode Only S = Synchronous Mode Only (local clock)
Only transfer rates indicated in section 1.3 Technical Data are qualified.

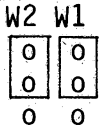
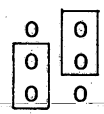
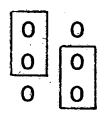
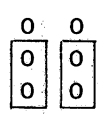
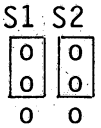
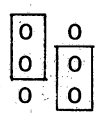
Link:	A/S:	Setting:	Description:
W2 W1		W2 W1 	Number of data bits per character
			8 bits
			6 bits
			7 bits
			5 bits
S1,S2	A	S1 S2 	2 stopbits
			1 stopbits

Figure 22.1 U-LINK SETTING - CONTINUED

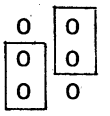
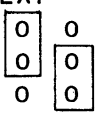
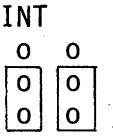
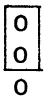
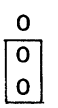
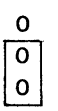
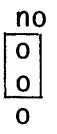
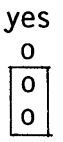
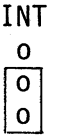
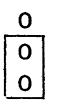
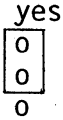
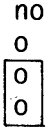
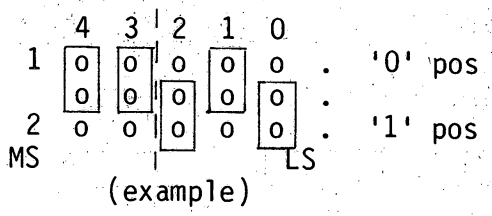
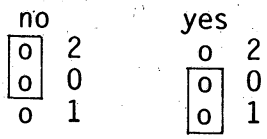
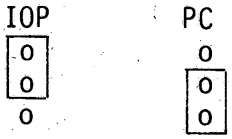
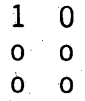
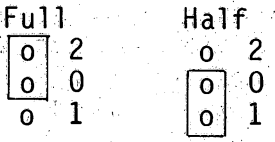
Link:	A/S:	Setting:	Description:
			1.5 stopbits
S1,S2	S	EXT 	Transparency Mode
		INT 	Internal Synchronization on SYN
MD		ASYN  SYN 	A-synchronous or Synchronous Mode
191	A	+12V  -12V 	Selection of the active level for CT119
COM		no  yes 	Comparator Operational for leading SYN transfer and HALT Char. detection
SYN	S	EXT 	Transparency Mode
		INT 	Internal Synchronization on SYN
134	S	CT114 	(Input) CT114 Modem
		CT113 	(Output) CT113 Local
BD		yes  no 	Break detection operational

Figure 22.1 U-LINK SETTING - CONTINUED

Link:	A/S:	Setting:	Description:
AD		 (example)	SALCU Address (Input) (shown /0A)
HC			Halt on preselected character
MO/PO			Channel in Output Mode
MI/PI			Channel in Input Mode
GEX			Internal clock pulse (shown: position for normal operation)
FH			Full or Half duplex mode

Note: A = Asynchronous Mode Only; S = Synchronous Mode Only

Figure 22.1 U-LINK SETTING - CONTINUED

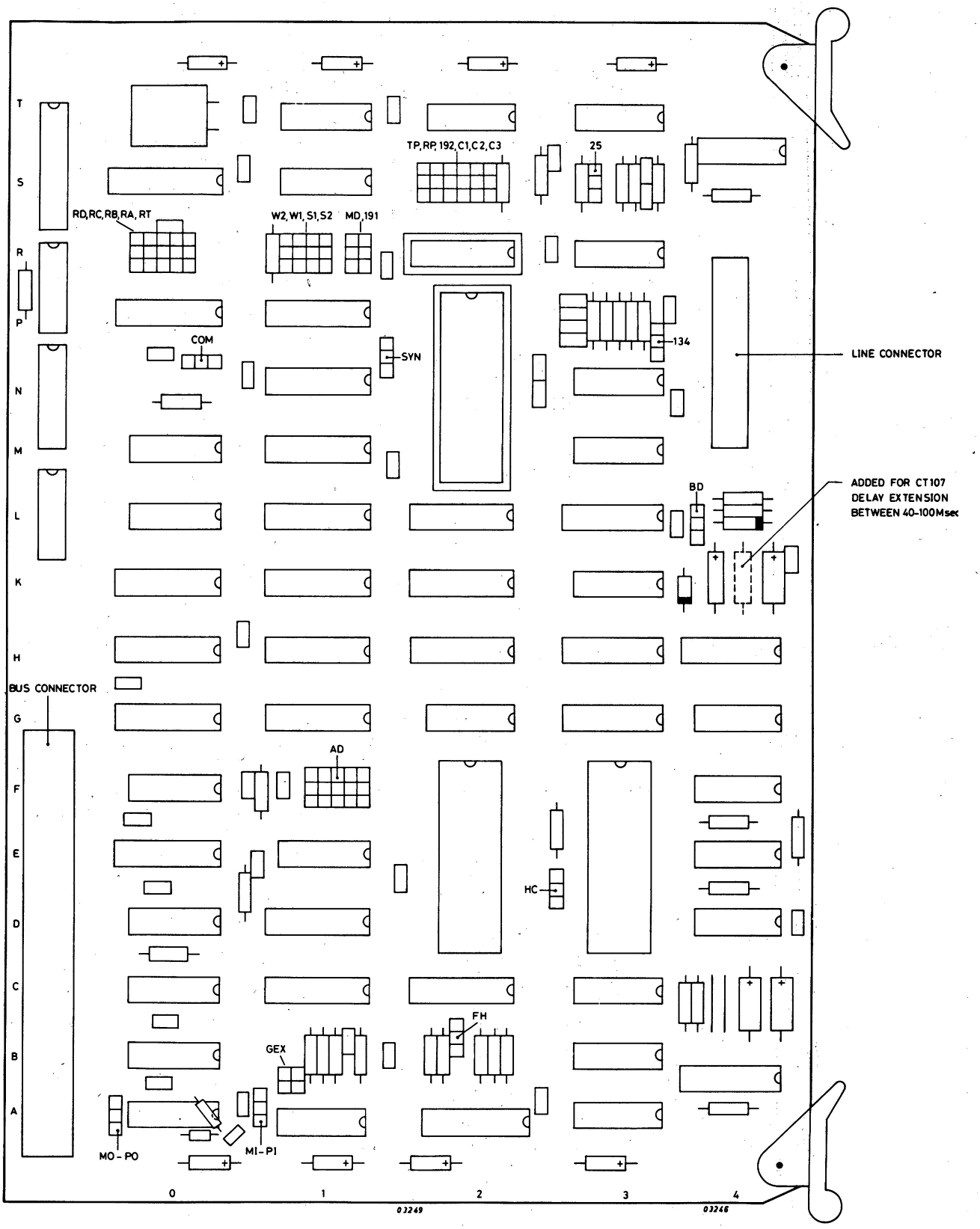


Figure 22.1 U-LINK SETTING - CONTINUED

22.4 INTERFACE CONNECTIONS

Available signals according V24 on SALCU-Z

Card (female)	Modem (male)	Signal Name	Signal Direction
1	1	CT101 mech. gnd	Bi-directional
7 - 25	7 - 25	CT102 logic gnd	Bi-directional
2	2	CT103 trx. data	Output to the DCTE
3	3	CT104 rec. data	Input to SALCUZ
4	4	CT105 req. to send	Output to the DCTE
5	5	CT106 ready f.s.	Input to SALCUZ
6	6	CT107 modem r.	Input to SALCUZ
20	20	CT108 connect m.	Output to the DCTE
8	8	CT109 carrier	Input to SALCUZ
15	15	CT113 m. clock	Output to the DCTE
15	15	CT114 trx. clock	Input to SALCUZ
17	17	CT115 rec. clock	Input to SALCUZ
16	16	CT119 backw. ch.	Input to SALCUZ
22	22	CT125 ring ind.	Input to SALCUZ

Table 22.1 SALCUZ SOCKET 3 CONNECTIONS TO DCTE

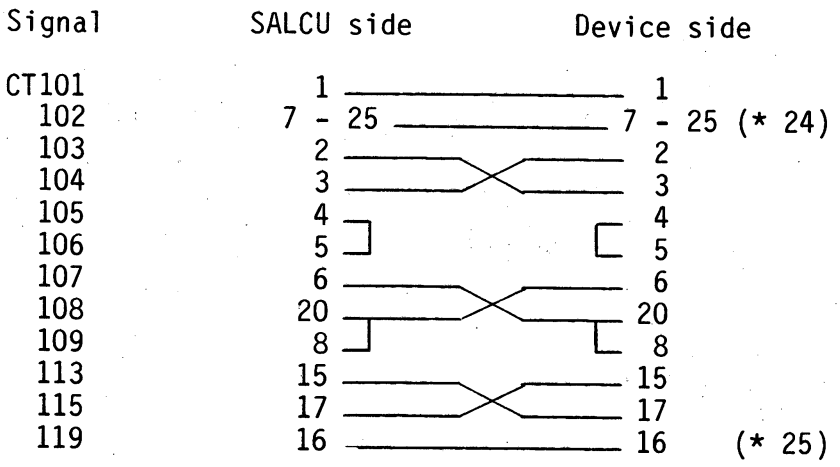
For SALCU-Z a standard cable is used.

Signal	Connector Panel Female	Modem Male
CT101	1	1
102	7 - 25	7 - 25
103	2	2
104	3	3
105	4	4
106	5	5
107	6	6
108	20	20
109	8	8
111	23	23
114	15	15
115	17	17
119	16	16
125	22	22

Note: CT111 is not controlled by SALCU.
Max. cable length is 15m.

Table 22.2 STANDARD CABLE SALCUZ

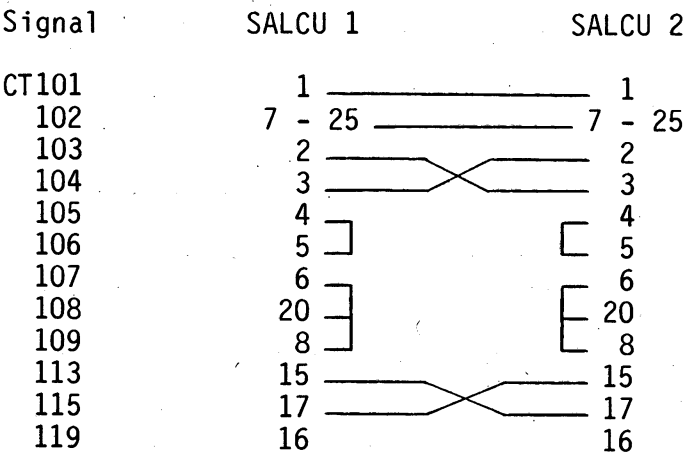
For a local connection, between CU and terminal, wiring could be made according:



(* = if RFR used on PER3100 typewriter)

Figure 22.2 INTERFACE WIRING CU-TERMINAL (LOCAL)

For local connection of two systems, wiring could be made according:

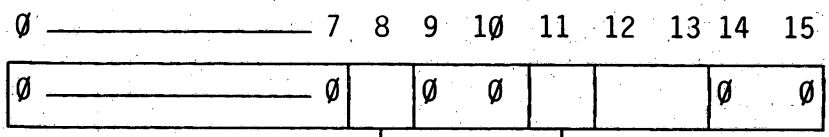


Note: U-link setting in this case RP ext
TP int
134 in 113 position

Figure 22.3 INTERFACE WIRING CU-CU (LOCAL)

Device address in = DA (rec)
Device address out = DA+1 (trx)

CIO start (in/out) BIO

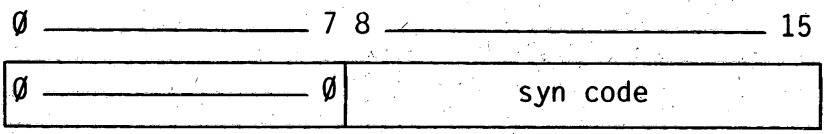


HD only (generate break (220ms)
(echo input)

X Ø = no parity
Ø 1 = even parity
1 1 = odd parity

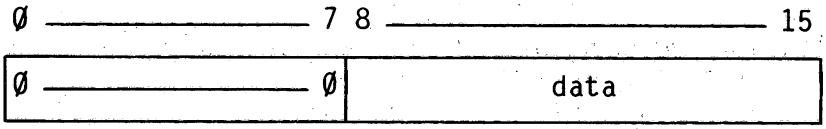
Notes: - CIO start-in must precede start out.
- generate break: only in idle or HD input.

OTR syn BIO
F = 1 (in/out)

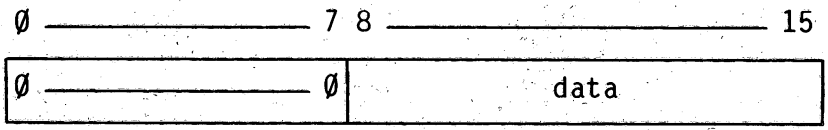


Synchronous mode only, immediately after 1st CIO start.

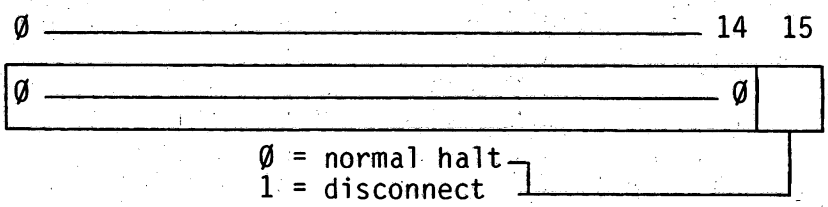
OTR data BIO
F = 0 (out)



INR data BIO
F = 0 (in)

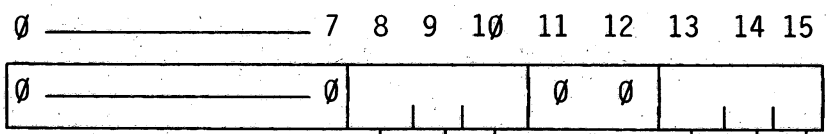


CIO halt (in/out) BIO



Notes: Normal halt at FD: CIO halt must be given for both input and output, before the next CIO start.
Disconnect : The specified device address must be 'input address'. The SALCU is reset immediately.

SST (in/out)



HD OUT: char. received (=break)
IN : ring indicator CT125
IN : carrier drops CT109
IN : parity error
IN : character loss (throughput)
modem not operable CT107

22.6 SHORT DESCRIPTION OF TESTPROGRAM

TESTPROGRAM BZSAC1

Transfer rate synchr. mode max. 4800 bps
a-synchr. mode max. 9600 bps

PROCEDURE:

- IPL
  Note: Connect loop plug! = CT 103-104 pin 2-3
  (Select local clock) CT 105-106- 4-5
  CT 108-107-109 2-6-8
- Switch on RTC, Lock (within 3 sec.)

Typewriter prints: Type in: example = standard configuration.

Initialization etc.
Standard checks etc.
Extra checks etc.

Standard checks?	Y
Address input?	0A
Nb of data bits?	07
Int input?	04
Int output	05
Channel?	P
Mode?	A
Error exit?	Y
Break detection?	N
Halt detection?	N
Reloop check?	N

- End of program, stop at address/0D00 = restart address

BZSAC1 tested:

IF 0000	(B)	Check 00 (standard)	Test I/O instruction
IF 0001	(B)	Check 01 ,,	Test sequensor
IF 0002	(B)	Check 02 ,,	Test interrupt in output mode
IF 0003	(B)	Check 03 ,,	Test input/output (1st part)
IF 0004	(B)	Check 04 ,,	Test input/output (2nd part)
IF 0005	(B)	Check 05 ,,	Test ODD/EVEN parity
IF 0006	(A)	Check 06 ,,	Test break emission
IF 0007	(A)	Check 07 ,,	Test throughput error
IF 0008	(A)	Check 08 ,,	Test break detection
IF 0009	(B)	Check 09 ,,	Test halt character
IF 000A	(A)	Check 10 (not standard)	Test CT119
IF 000B	(A)	Check 11 ,,	Test parity error detection and echo mode/visualisation
IF 000C	(B)	Check 12 ,,	Test CT105
IF 000D	(S)	Check 13 ,,	Test comparator inhibition
IF 000E	(S)	Check 14 ,,	Test transparency mode
IF 000F	(B)	Check 15 (standard)	Test multiplex

A = Asynchronous mode only
B = Both modes
S = Synchronous mode only

Procedure 5111 991 10071 = Procedure BZSAC1 5111 991 09304
with addendum PTS8000 5111 991 11381
Listing 5111 991 10081
Program 5111 199 65671

```
                        IDENT    SALCUT
                        *
                        * SALCU PROGRAM, TRX ONLY, A-SYNCHRONOUS
                        * CONNECT LOOPPLUG: CT108-107-109 (PIN 20-6-8) AND CT105-106 (PIN 4-5)
                        *
                        * LINE CHECKED WITH OSCILLOSCOPE:
                        *
                        *    '0'=+12V    I---I   I---I   I---I   I---I   I---I   I---I STOPBITS
                        *    '1'=-12V ---I   I---I   I---I   I---I   I---I   I---I
                        *                      1   0   1   0   1   0   1   0
                        *          =A2 BITN   15  14  13  12  11  10   9   8      /55='U'
                        *
                        *
                        * OR:  CONNECT CTW, 1 LINE OF CHARS 'U' IS PRINTED (USE CT108/7/5/6)
                        *
                        * INTERRUPT LEVEL 11 = /B
     001B               DA       EQU      /1B
0000                    RES      /40
0080  FFFF              DATA     DATA     /FFFF
0082  0000              DATA     0
0084  207F              START    HLT
0086  2840              ENB
0088  87A0              BEG      LDKL     A15,/120              STACKPOINTER
008A  0120
008C  8120              LDKL     A1,INTAD
008E  009A  R
0090  8141              ST       A1,/16                 START ADDR INT ROUTINE
0092  0016
0094  0104              LDK      A1,4
0096  410B              CIO      A1,1,DA
0098  5F02              RB       *                      WAITING FOR DATA INTERRUPT
                        *
                        *   INTERRUPT ROUTINE
                        *
009A  0255              INTAD    LDK      A2,/55                CHAR 'U'
009C  421B              OTR      A2,0,DA
009E  F03E              RTN      A15



                        IDENT    SALCLA
                        *
                        * LOOP, FULL DUPLEX, A-SYNCHRONOUS
                        * CONNECT LOOPPLUG: CT103-104  PIN 2-3, 105-106 PIN 4-5,
                        *                   CT108-107-109=PIN 20-6-8
                        * 7-BITS, EVEN PARITY
                        *
                        *  CHECK:1) STOP AFTER INR.(REPLACE '/5408' BY '/207F')
                        *           CHECK IF REC CHARACTER='U': A3 MUST CONTAIN /55.
                        *        2) CHECK OSCILLOSCOPE PICTURE.(SEE PROGRAM SALCUT)
                        *
                        *        DATA FAULT: STOP AT /0AE (HHP /0080)
                        *        STATUS FAULT: STOP AT /B2 OR /B8 (HHP /B4,/BA)
     001A               DAREC    EQU      /1A
     001B               DATRX    EQU      /1B
     000A               INTREC   EQU      10
     000B               INTTRX   EQU      11
0000                    RES      /40
0080  FFFF              DATA     DATA     /FFFF
0082  0000              DATA     0
                        * -- MAIN PROGRAM --
0084  207F              START    HLT
0086  2840              ENB
0088  0255              BEG      LDK      A2,/55                CHAR 'U'
008A  87A0              LDKL     A15,/120              STACKPOINTER
008C  0120
008E  8120              LDKL     A1,STAR               START ADDR INT ROUTINE REC
0090  00A6  R
0092  8141              ST       A1,/14
0094  0014
0096  8120              LDKL     A1,STAT               START ADDR INT ROUTINE TRX
0098  00B4  R
009A  8141              ST       A1,/16
009C  0016
009E  0104              LDK      A1,4
00A0  411A              CIO      A1,1,DAREC
00A2  411B              CIO      A1,1,DATRX            START I/O
00A4  5F02              RB       *                     WAIT FOR INTERRUPT
                        * -- INTERRUPT ROUTINE REC --

00A6  481A              STAR     INR      A3,0,DAREC
00A8  5408              RF(4)    *+/A
00AA  EB08              CWR      A3,A2
00AC  5002              RF(0)    ERR                   DATA FAULT
00AE  207F              HLT
00B0  F03E              ERR      RTN      A15                   EQUALITY RIGHT,RETURN
00B2  207F              HLT



                        *  INTERRUPT ROUTINE TRX --
00B4  421B              STAT     OTR      A2,0,DATRX
00B6  5002              RF(0)    *+4
00B8  207F              HLT
00BA  F03E              RTN      A15                   IF NO STATUS ERROR
```

```
                        IDENT    SALCLS
                    * LOOP ON SALCU, FULL DUPLEX, SYNCHRONOUS MODE
                    *CONNECT LOOPPLUG:CT103-104 (PIN 2-3),105-106 (4-5),108-107-109(20-6-8)
                    *        DATA: SYN - SYN - CHAR 'U'
                    *
                    * CHECK: STOP PROGRAM AFTER INR.(REPLACE /EC18 BY /207F)
                    *              CHECK IF REC CHAR ='U'.(REG A6 MUST CONTAIN /55)
                    *      -OR- CHECK WITH OSCILLOSCOPE
                    *
                    *     DATA FAULT: STOPS AT /B2 (B4 AT HHP)
                    *     STATUS FAULT KEEPS PROGRAM IN RUN,BUT DATA TRANSFER STOPS
                    *
                    *
                    * OSCILLOSCOPE PICTURE:

                    *  0  0 000 0  0 000  0 0 0 0
                    *   11 1     11 1    1 1 1 1
                    *   SYN      SYN      'U'CHAR
     001A           DAREC    EQU      /1A
     001B           DATRX    EQU      /1B
     000A           INTREC   EQU      10
     000B           INTTRX   EQU      11
0000                        RES      /40
0080 FFFF           DATA     DATA     /FFFF
0082 0000                    DATA     0
                    *
                    * -- MAIN PROGRAM --
0084 207F           START    HLT
0086 2840                    ENB
0088 87A0           BEG      LDKL     A15,/120            STACKPOINTER
008A 0120
008C 8120                    LDKL     A1,STAR             START ADDR INT ROUTINE REC
008E 00AC  R
0090 8141                    ST       A1,/14
0092 0014
0094 8120                    LDKL     A1,STAT             START ADDR INT ROUTINE TRX
0096 00C6  R
0098 8141                    ST       A1,/16
009A 0016
009C 0416                    LDK      A4,/16              SYN CHAR CODE
009E 8220                    LDKL     A2,/FFFD            CONTROL COUNTER
00A0 FFFD
00A2 030C                    LDK      A3,/C
00A4 43DA                    CIO      A3,1,DAREC          START REC
00A6 445A                    OTR      A4,1,DAREC          SYN
00A8 43DB                    CIO      A3,1,DATRX          START TRX
00AA 5F02                    RB       *                   WAIT FOR INTERRUPT


                    *
                    * -- INTERRUPT ROUTINE REC --
00AC 4E1A           STAR     INR      A6,0,DAREC
00AE EC18                    CWR      A4,A6
00B0 5002                    RF(0)    ON                  HLT IF DATA FAULT
00B2 207F                    HLT
00B4 439A           ON       CIO      A3,0,DAREC
00B6 8140                    LD       A1,/120
00B8 0120
00BA 190E                    SUK      A1,/E
00BC 8141                    ST       A1,/120             CHANGE RETURN ADDRESS
00BE 0120
00C0 4DDA                    SST      A5,DAREC
00C2 5C04                    RB(4)    *-2                 STATUS
00C4 F03E                    RTN      A15
                    *
                    * -- INTERRUPT ROUTINE TRX --
00C6 4FDB           STAT     SST      A7,DATRX            STATUS
00C8 500C                    RF(0)    RET2
00CA 1201                    ADK      A2,1
00CC 5004                    RF(0)    DAT
00CE 5204                    RF(2)    SYN
00D0 439B                    CIO      A3,0,DATRX
00D2 0455           DAT      LDK      A4,/55
00D4 441B           SYN      OTR      A4,0,DATRX
00D6 F03E           RET2     RTN      A15
```

23 HIGH LEVEL DATA LINK COMMUNICATION CONTROL UNIT P845-100 (HLCUZ)

SECTION	23.1	HLCU-Z IDENTIFICATIONS	PAGE 23-2
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	23.3	INSTALLATION DETAILS	23-4
	23.4	INTERFACE CONNECTIONS	23-4
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	23.6	SHORT DESCRIPTION OF TESTPROGRAM	23-9
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LIST OF TABLES

TABLE	23.1	STANDARD CABLE HLCUZ	23-5

23.1 HLCUZ IDENTIFICATIONS

Typenumber	: P845-100	
Testprogram	: BHLCU1	
Channel	: PC or IOP	
	Interrupt Connections:	Transmitter 1C05
		Receiver 1C04
	Break Connections :	Transmitter 1A05
		Receiver 1A04
Devices	: 1 line, Full Duplex or	Half Duplex
Power Consumption	: +5VL 1.9A	
	+5VL 50mA	
	12VL 90mA	

12NC code on the sticker on the board:

5111 199 6137x (5322 216 25311)

X = Modification level

23.2 FACILITIES

- High Level data link communication Control Unit
- V24/V28 MODEM interface, HDLC or SDLC protocol, remote or local connection
- 1 line, Full Duplex or Half Duplex
- Internal clock selectable for transfer rate 7.2k - 57.2k or 115.2kbps for local use or loop test. (CT113)
- NRZI data selectable (used for connection to IBM-systems)
- CT108 : selectable controlled -or- forced active
- 20 sec time out selectable for check on data (or status) reception
- Secondary station address links for remote IPL command reception (not for PTS 8400)
- CCITT Cyclic Redundancy Checkword (ECMA 40) as Frame Check Sequence
- Device address — transmitter = odd — receiver = even
  interrupt — transmitter on pin 1C05 — receiver on pin 1C04
  break — transmitter on pin 1A05 — receiver on pin 1A04

NRZI = Non Return on zero Inverted = change on zero bits

Control codes according HDLC on HLCU-Z:

	transmit	receive
flag	non-overlap	both types
abort	8 'one'-bits	7 or more 'one'-bits
idle	16 'one'-bits	15 or more 'one'-bits

23.3 INSTALLATION DETAILS

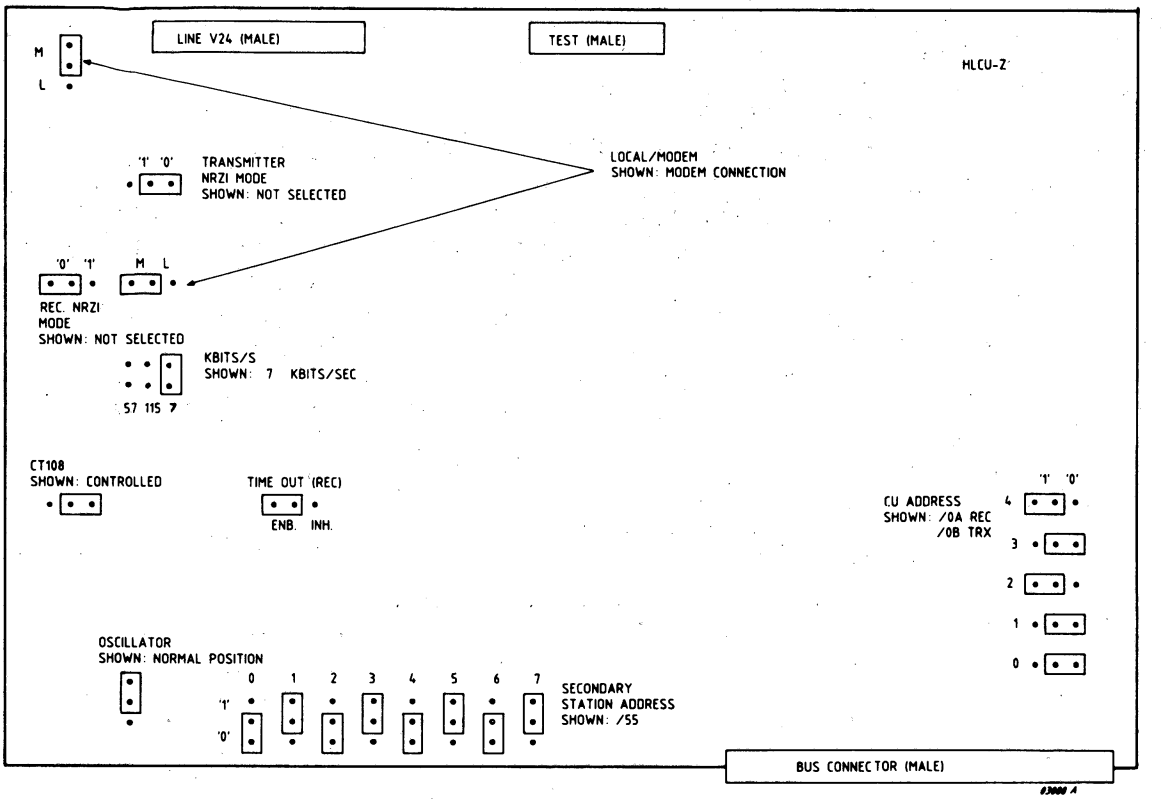


Figure 23.1 U-LINK SETTING

Note: If remote IPL, CT108 link must be in 'not controlled' position.
On later PCB's the time out link is fitted left of tr. NRZI link.

23.4 INTERFACE CONNECTIONS

V24 Interface

a) From C.U. to device		pin:
- CT103	: Data line (transmit)	2
- CT105	: Request to send	4
- CT108	: Connect data set to the line	20
- CT113	: Local clock pulse	15

b) From device to C.U.

- CT104	: Data line (receive)	3
- CT106	: Ready to send - Answer to CT105	5
- CT107	: Data set ready - Answer to CT108	6
- CT109	: Data channel received line signal detector	8
- CT114	: Transmitter clock pulse	15
- CT115	: Receiver clock pulse	17
- CT125	: Ring indicator	22

c) General

		pin:
- CT101	: Mechanical ground (shield)	1
- CT102	: Electrical ground	7

Bus Interface

IROON	: transm-interrupt	1C05
IR01N	: receiver interrupt	1C04
BROON	: transm break	1A05
BR01N	: receiver break	1A04
IPLN	: remote IPL	1C03

For HLCU-Z a standard cable is used.

Signal	Connector Panel Female	Modem Male	
CT101	1	1	
102	7 - 25	7 - 25	(15m max.)
103	2	2	
104	3	3	
105	4	4	
106	5	5	
107	6	6	
108	20	20	
109	8	8	
111	23	23	
114	15	15	
115	17	17	
119	16	16 (not used)	
125	22	22	

Table 23.1 STANDARD CABLE HLCUZ

For a local connection, between CU and terminal, wiring could be made according:

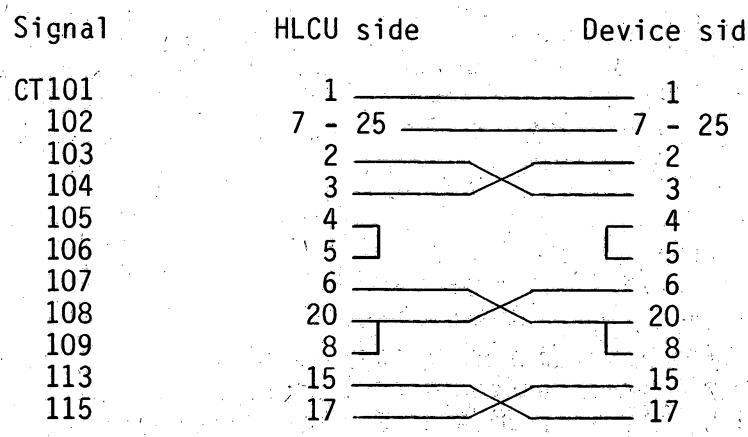
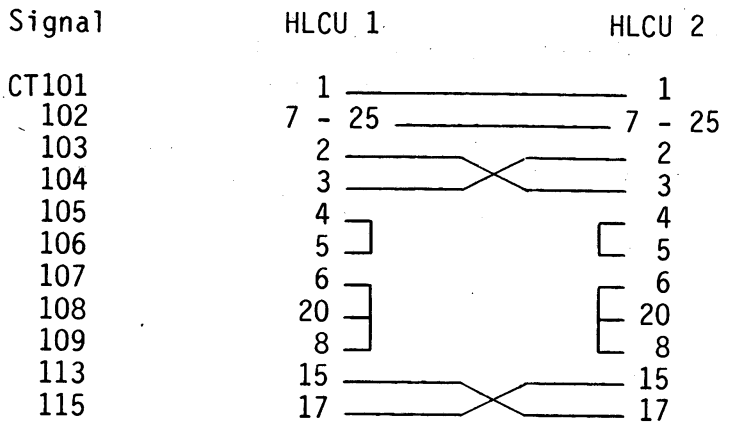


Figure 23.2 INTERFACE WIRING CU-TERMINAL (LOCAL)

For local connection of two systems, wiring could be made according:

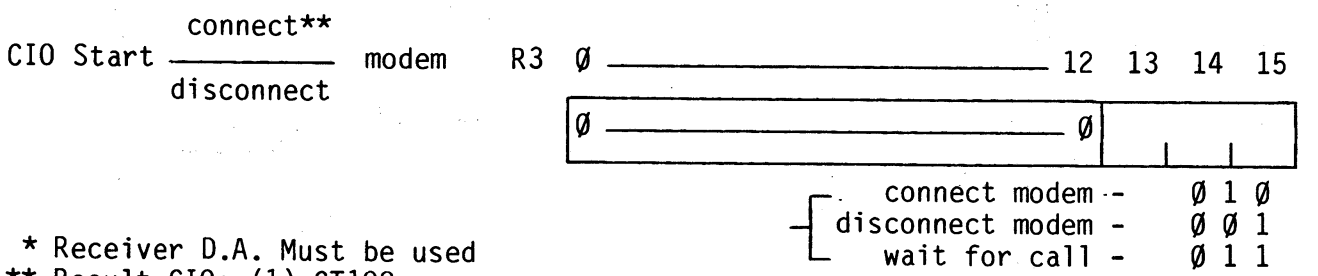


Note: U-link setting in this case: both in LOCAL.

Figure 23.3 INTERFACE WIRING CU-CU (LOCAL)

23.5 HARDWARE-SOFTWARE INTERFACE DETAILS

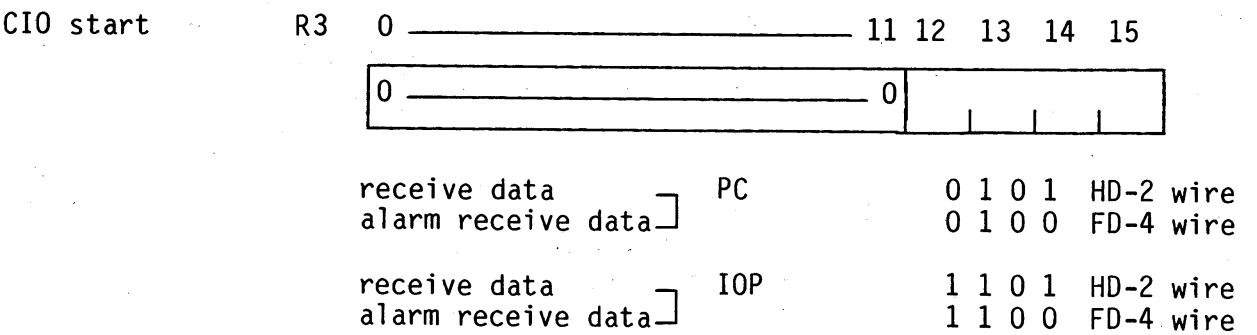
General



* Receiver D.A. Must be used
** Result CIO: (1) CT108
(2) after 100ms - 90 to WST (check on CT107)

Result : - wait for call: ┌modem not ready - go to WST after CT125 rec.
└modem ready - to to WST. (modems CT107 forced active)

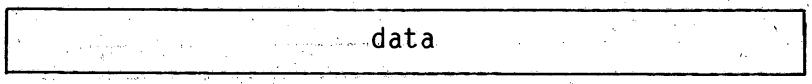
Reception



- receive data
  (1) data exchange per 16 bits (HD-2 wire)
  (2) FCS computation/zero deletion/idle, flag, abort det.
  (3) 20 sec. delay, check on DATA or STATUS exchange
- alarm receive data. See rec. data (FD-4 wire)
  and
  direct check on CT109 carrier

- CIO halt/EOR. results: (1) FCS checked/end flag
  (2) go to WST

- INR (F = Ø) R3 Ø ——— 15



SST

R3 see table:

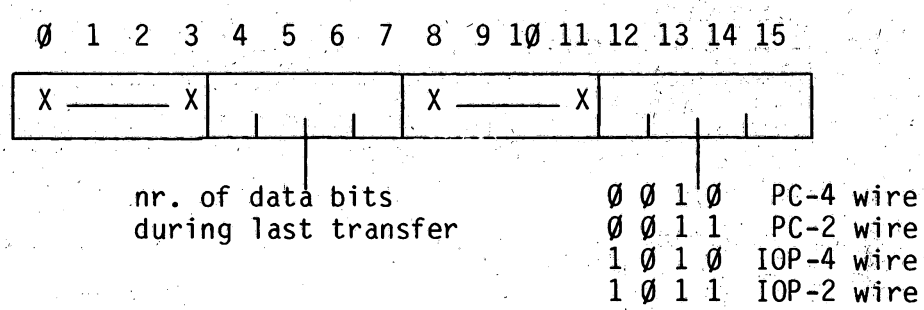
Receiver status

bit:
9 - CT125
10 - CT109 drops
15 - no-op

14 - throughput error
13 - CRC error
12 - incorrect length (only MC)
2 (- idle ones
(- abort ones
4-7 - binary code = last word specification

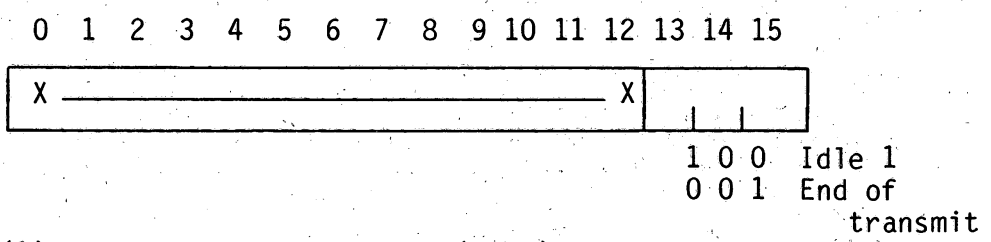
Transmission

CIO start



Result: CT105 ┌4 wire: active
└2 wire: active if no CT109

CIO start release



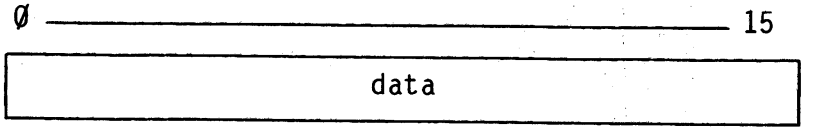
Result: ┌Idle 1 — (1) idle on line (slow)
(2) go to WST recognized at reception
└End of transmit —— (1) CT1Ø5 cleared
(2) go to WST (fast)

Note: Idle and abort at reception side are only recognized after at least 1 char transfer —— go to WST.

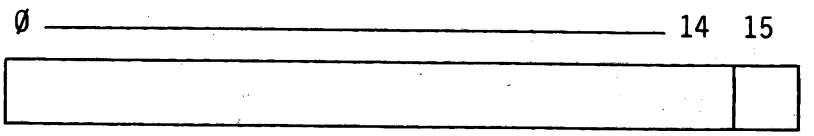
CIO halt (/EOR) normal end of exchange.

Result: (1) FCS, ending flags transferred
(2) go to WST

OTR (F = Ø) R3



OTR 1 (F = 1)



idle transm = 0
abort transm = 1

Result: (1) control char. transmit
(2) go to WST

SST

Transmitter status

BIO bit 15 - no-op: CT107 drops.
14 - throughput error
└ abort transmitted

23.6 SHORT DESCRIPTION OF TESTPROGRAM

TESTPROGRAM BHDLC

12K
Program runs under monitor BOS
- Connect loop-plug to HLCUZ, set Local Clock

Procedure:

- IPL
  RTC on

Terminal output:	Type in on keyboard:
PARMON	
Standard or change FC	C "CR"
Full/half duplex	F ''
Input device address	ØA ''
interrupt level	Ø4 ''
Output device address	ØB ''
interrupt level	Ø5 ''
PC or IOP	P ''
Leased or switched line	L ''
End of PARMON	
Print 1 for HLCU1	
Print Ø for HLCUZ	
*	Ø ''
Filecode	5 ''
*	"CR"

- The program starts after 'CR' is depressed.
- Check on running testprogram: take off the loop-plug from HLCUZ!
  An error message will be displayed on the terminal.
- Stop program: press Control Panel Interrupt button.
  type 'SP' on keyboard (= Stop Program)

Loop-plug wiring: HLCUZ	pin	CT
	2 - 3	1Ø3 - 1Ø4
	4 - 5	1Ø5 - 1Ø6
	20-6-8	1Ø8-1Ø7-1Ø9
	15 - 17	113 - 115

Note: Max. speed 7.2 kbits/sec.

Error Messages

Errors in the command message

ERR 0 : - A wrong order has been printed
        - More than one order has been printed

ERR 1 : - Too much characters have been printed
          . More than 4 in the word length or in the pattern
          . More than 2 in the bit length or bit length greater than 15

ERR 2 : - Decimal number greater than 9 or hexadecimal number greater than /F

ERR 13: - The required check does not correspond to the file code definition

Errors printed during running of a check:

ERR 3 : Status error after a CIO connect

ERR 4 : Hardware status error after a Transmission

ERR 5 : Software status error after a Transmission

ERR 6 : Hardware status error after a Reception

ERR 7 : Software status error after a Reception

ERR 8 : Error in the residual bit count after a Reception

ERR 9 : Error in the effective length after a Reception

ERR 10: The last received word is not OK (error at bit level)

ERR 11: Status error after a CIO disconnect

ERR 12: Error in the received data

Remark:

- Errors from 4 to 9 and error 11 are followed by a dump of the concerned ECB.
- Errors 10 and 12 are followed by a dump of the receiver data buffer with the indication of the first wrong data and the indication of the expected data.

ECB Description

The Event Control Block is provided to the monitor with the request; it is a seven word long table whose content is as follows:

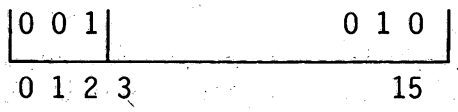
WORD 0	E	File code
WORD 1	Buffer address	
WORD 2	Nb of bits	Requested length
WORD 3	Nb of bits	Effective length
WORD 4	Status	
WORD 5	Reserved	
WORD 6	Control Word	

WORD 0 Bit 0 = Event bit
- Is managed by the monitor
- Reset at request time
- Set when the request is ended.

File Code
To be provided by the user.
The file code is defined at system generation time or by an assign request.

WORD 1 Buffer Address
To be provided by the user.
It is the first address of the user data buffer.

WORD 2 Requested Length
To be provided by the user.
It indicates in characters and bits the desired length of the frame.
Example: Requested length 17 bits.



= 2 characters and 1 bit

WORD 3 Effective Length
Is provided by the monitor on request completion and provides the user the effective length of the transmitted frame.
The effective length has the same format (character and bits) as the requested length.

WORD 4 Status
This information is given by the monitor.
It is meaningful only when the Event bit is set.

WORD 5 Reserved

WORD 6 Control word
That word contains the timer value in multiple of 100ms.
Control word equal to zero implies no time out supervision.

Status Description

The status returned in the ECB contains the result of the transmission:

Bit 0 = 0 Software status
Bit 0 = 1 Hardware status

Software Status

Bit 0 = 0
    1 = Not significant
    2 = Non connected line
    3 = Illegal Request - Line already connected
                        - Invalid order
                        - Disconnect requested on an active line
                        - Abort/Idle requested on an Input file code
4 to 7 = Irrelevant
    8 = Transmission stopped
    9 = Time out request may not be served
   10 = Time over
   11 = Abort requested with a non active line
   12 = File code table overflow
   13 = NS
   14 = NS
   15 = Line busy

Hardware Status

Bit 0 = 1
    1 = NS
    2 = Abort detected
    3 = Idle detected
4 to 7 = Number of true data bits in the last word (if 0, the length is 16 bits)
    8 = NS
    9 = Ring indicator
   10 = End of carrier detection
   11 = Command refused
   12 = Incorrect length
   13 = FCS error
   14 = Throughput error
   15 = Modem not operable

On each request a timer is set its value is:

- 100 ms For a stop request
- 200 ms For a connect or a disconnect request
- 3,5 s   For a read or write request.

Procedure	5111 991 11491 =	Procedure BHDLC	5111 991 Ø8885
		with addendum PTS8ØØØ	5111 991 11381
Listing	5111 991 08895		
Program	5111 199 69585		

```
                        IDENT    HLCUT
                      * TRX CONTINUOUSLY DATA /FC
                      *
                      * CONNECT LOOPPLUG: CT105-106 (PIN 4-5), 108-107 (20-6) AT LEAST.
                      * LOCAL CLOCK 57 (OR 7 KBITS/SEC), NRZI NOT SELECTED
                      *
                      * CHECK WITH OSCILLOSCOPE:          10 USEC/DIV.10 V/CM
                      * CT103 PIN 2
                      *      PROGRAM RUNS:
                      *      +12V='0' --I   I---I---I                    I---I   I-
                      *      -12V='1'   I---I       I---I---I---I---I---I   I---I
                      *                   0   0   1   1   1   1   1   0   1
                      *                 I----------DATA /FC-----------------I
                      *
                      *      EXECUTE PROGRAM INST-BY-INST UNTIL CIO START:
                      *
                      *       +12V='0'      I---I---I                     I---I---I
                      *       -12V='1'    --I       I---I---I---I---I---I---I       I--
                      *                     0   0   1   1   1   1   1   1   0   0
                      *                   I-----------FLAG---------------I
                      *                   LS                           MS
                      *
      000A    DAREC   EQU     /0A
      000B    DATRX   EQU     /0B
0000          RES     /40
0080  FFFF    DATA    DATA    /FFFF
0082  0000            DATA    0
0084  207F    START   HLT
0086  20BF            INH
0088  0102    BEG     LDK     A1,2
008A  41CA            CIO     A1,1,DAREC          CONNECT
008C  48CA            SST     A3,DAREC
008E  5C04            RB(4)   *-2
0090  41CB            CIO     A1,1,DATRX          START DATA OUT
0092  8220            LDKL    A2,/FCFC
0094  FCFC
0096  420B            OTR     A2,0,DATRX
0098  4CCB            SST     A4,DATRX            STATUS
009A  5C06            RB(4)   *-4                 OTR IF STATUS OK
009C  207F            HLT
                      END     START
```

```
                        IDENT    HLCUL
                        *
                        * HLCU LOOPS FRAME: FLAG - DATA /FC, /FC - FCS (=CRC) -FLAG
                        *
                        * CONNECT LOOPPLUG: CT103-104 (PIN 2-3), 105-106 (4-5), 113-115 (15-17)
                        *                    CT108-107-109 (20-6-8)
                        * CHECK CORRECT RUNNING:
                        *          1) STOP AFTER INR.(REPLACE /EC08 BY /207F)
                        *             REG A4 MUST CONTAIN /FCFC.
                        *          2) CHECK OSCILLOSCOPE PICTURE:(USE MAGNIFIER)          50 USEC/DIV
                        *             PROGRAM RUNNING:
                        *
                        *   +12V 0      00      000     0 00     0 00  0000   00   0      00
                        *   -12V  111111  111111   11111 1  11111 1  11    111  111 111111  1111
                        *        I-FLAG-II-FLAG-II-DATA--II-DATA--II----FCS-------II-FLAG-II-FLA
                        *
                        *
                        *            PROGRAM NOT RUNNING / INST BUTTON PRESSED:
                        *
                        *   +12V    00      00      00      00
                        *   -12V   1  111111  111111  111111
                        *            I-FLAG-II-FLAG-II-FLAG-I
                        *
                        *
                        * ERROR: DATA FAULT STOPS AT /BA (/BC AT HHP)
                        *        STATUS FAULT KEEPS PROGRAM IN RUN
                        * LOCAL CLOCK 57 (OR 7) KBITS/SEC, NRZI NOT SELECTED
        000A            DAREC    EQU      /0A
        000B            DATRX    EQU      /0B
        0004            INTREC   EQU      4
        0005            INTTRX   EQU      5
0000                            RES      /40
0080    FFFF            DATA     DATA     /FFFF
0082    0000                     DATA     0
0084    207F            START    HLT
                        *
                        * MAIN PROGRAM:
0086    87A0            BEG      LDKL     A15,/120
0088    0120
008A    8120                     LDKL     A1,STAR
008C    0080  R
008E    8141                     ST       A1,8
0090    0008
0092    8120                     LDKL     A1,STAT
0094    00C4  R
0096    8141                     ST       A1,/A
0098    000A
009A    0102                     LDK      A1,2
009C    20BF                     INH
009E    41CA                     CIO      A1,1,DAREC          CONNECT MODEM
00A0    4CCA                     SST      A4,DAREC            STATUS
00A2    5C04                     RB(4)    *-2
00A4    2840                     ENB
00A6    0105                     LDK      A1,5
00A8    41CA                     CIO      A1,1,DAREC          START REC
00AA    0302                     LDK      A3,2
00AC    43CB                     CIO      A3,1,DATRX          START TRX
00AE    5F02                     RB       *                   WAIT FOR INTERRUPT
                        *
                        * REC INT ROUTINE
00B0    4DCA            STAR     SST      A5,DAREC
00B2    500C                     RF(0)    *+/E
00B4    4C0A                     INR      A4,0,DAREC          DATA TO A4
00B6    EC08                     CWR      A4,A2
00B8    5002                     RF(0)    *+4                 HLT IF DATA FAULT
00BA    207F                     HLT
00BC    418A                     CIO      A1,0,DAREC          STOP REC
00BE    F03E                     RTN      A15
00C0    41CA                     CIO      A1,1,DAREC
00C2    F03E                     RTN      A15
                        *
                        * TRX INT ROUTINE
00C4    4ECB            STAT     SST      A6,DATRX
00C6    500A                     RF(0)    *+/C
00C8    8220                     LDKL     A2,/FCFC            DATA /FCFC
00CA    FCFC
00CC    420B                     OTR      A2,0,DATRX
00CE    418B                     CIO      A1,0,DATRX          STOP OUTPUT
00D0    F03E                     RTN      A15
00D2    43CB                     CIO      A3,1,DATRX
00D4    F03E                     RTN      A15
```